


Schematic: Expansion Accessory

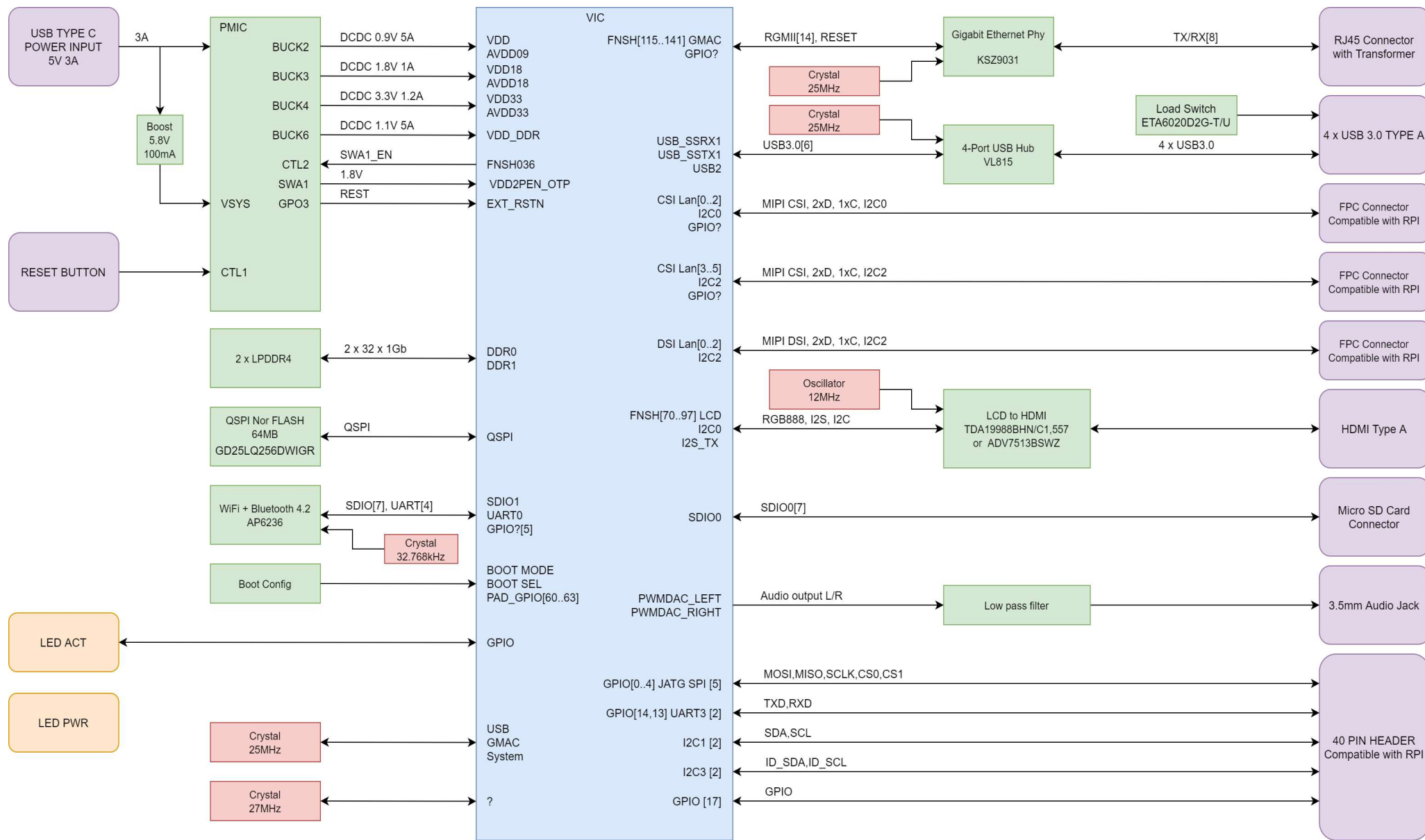
SHEET	SHEET NAME
01	Title/Revision History
02	System Block Diagram
03	Power Tree Diagram
04	PMIC
05	VIC Power
06	VIC DDR Ctrl
07	VIC ChipLink & CM
08	VIC LCD & GMII & GPIOs
09	VIC HighIF & Ctrl Other
10	LPDDR (A)
11	LPDDR (B)
12	Type C,uSD, QSIP Flash
13	USB 3.0 HUB
14	2 x USB TYPE A (A)
15	2 x USB TYPE A (B)
16	2 x CSI CONN
17	DSI, AUDIO JACK
18	HDMI FRAMER
19	WiFi, Bluetooth
20	10/100/1000 ETHERNET
21	RPI EXP CONN, LED, BUTTON

Revision History


DATE	REVISION	DESCRIPTION
Nov. 23 2020	v0.1	1. Initial release
Nov. 25 2020	v0.2	1. Add USB Hub circuit 2. Modify reset circuit of KSZ9031, removed interrupt function 3. Change LV2 output form LD03 to BUCK5
Nov. 25 2020	v0.3	1. Add Power down control and power on button
Dec. 1 2020	v0.4	1. Add reset button
Dec. 23 2020	v0.5	1. Add U74 JTAG connector for Tag-Connect cable 2. Modiy GPIO assignment for better layout
Dec. 28 2020	v0.6	1. Swap Buck2 and Buck6 of PMIC for better layout 2. Remove R67 and R76 from DNP group 3. Modify the value of C46 C215 C223 C224
Feb. 18 2021	v0.7	1. Add 100kOhm pull-up to UART3_RXD_3V3 2. Modify LED, JTAG, 3. Add boot selection button 4. Add UART3 1V8 5. Change R256 and R262 to 12.1kOhm 6. Modify Q6, Q7 schematic package 7. Add GPIO controll1 to GMAC reset pin 8. Change System Reset High voltage to 3.3V 9. Add reset IC for VIC
Feb. 22 2021	v0.8	1. Add a diode at the USB input to prevent the reverse current
Feb. 22 2021	v0.9	1. Remove Power down control and power on button 2. Modify Power LED control

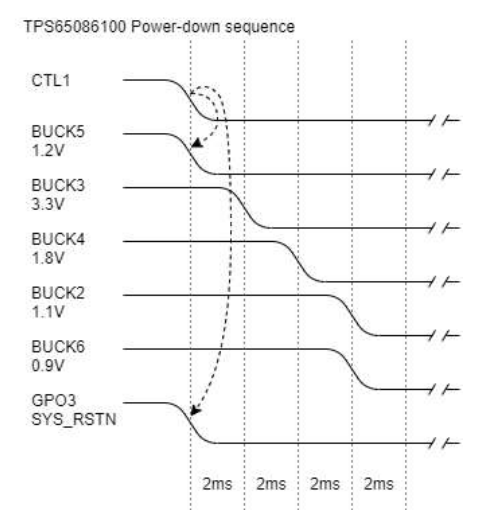
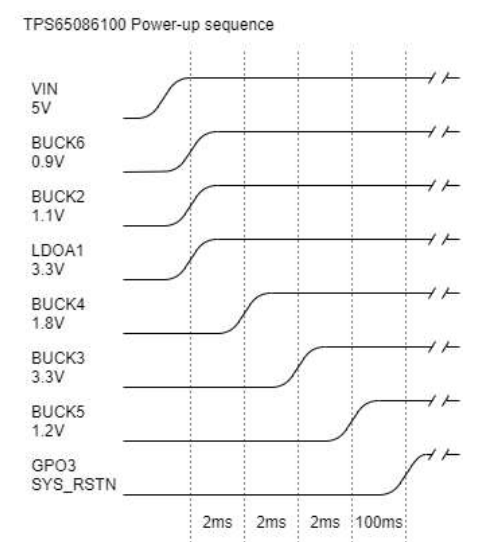
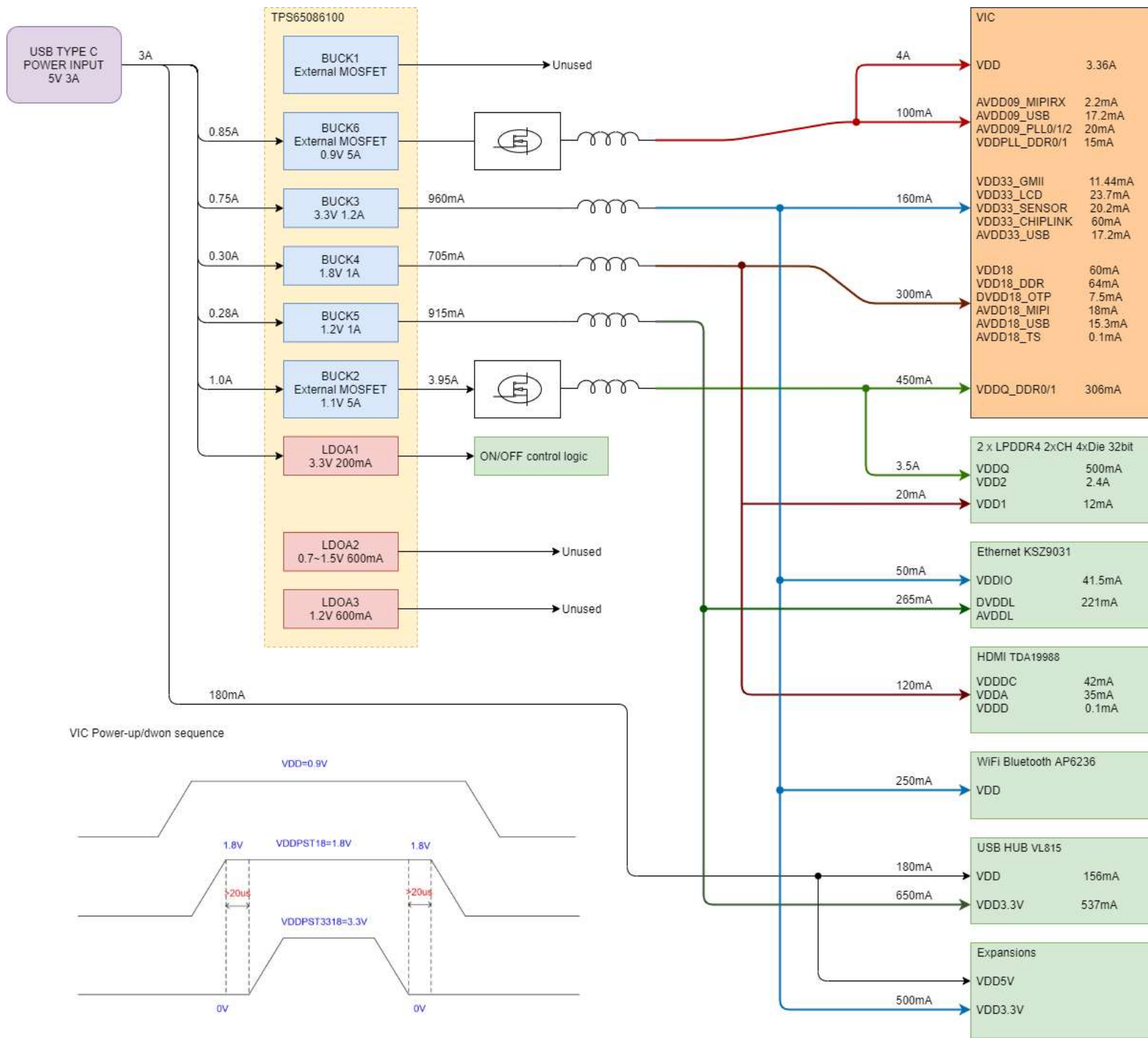
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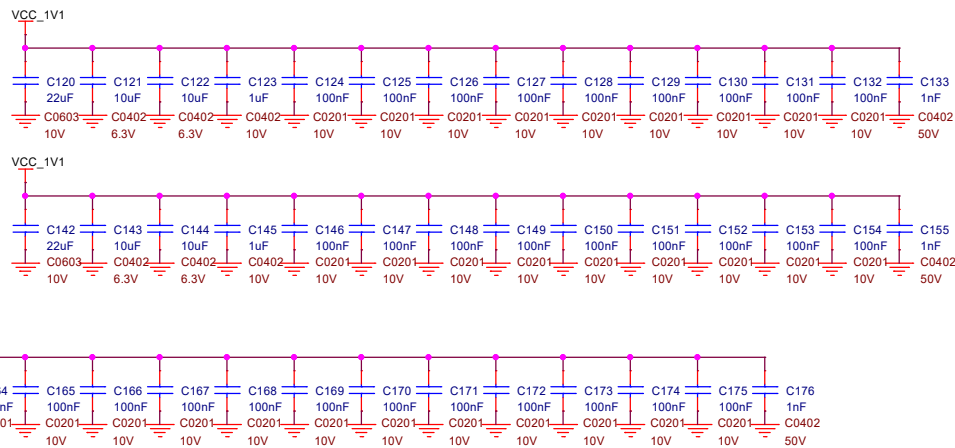
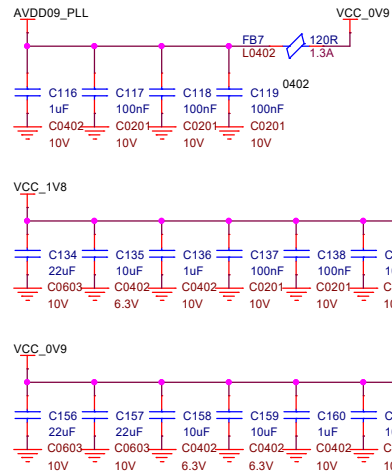
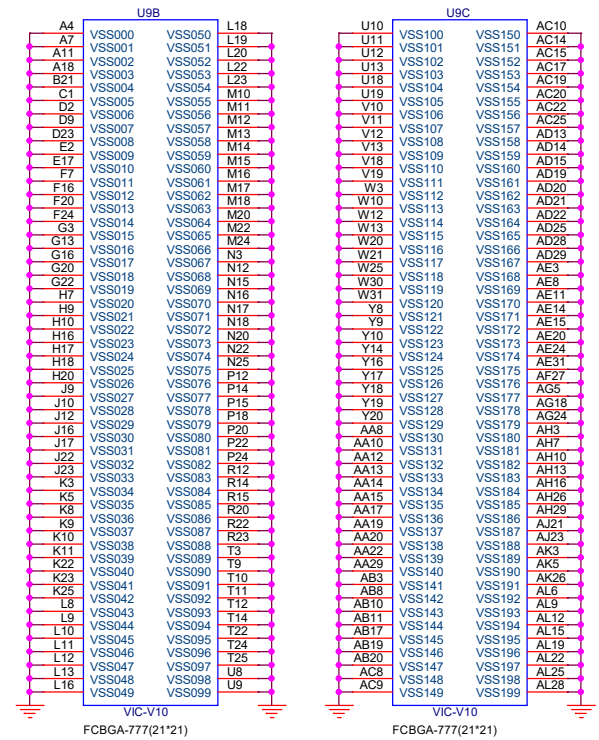
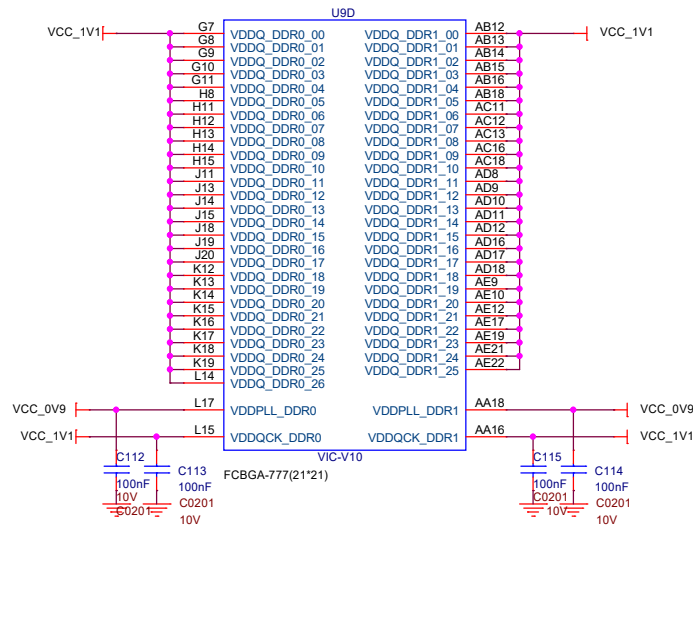
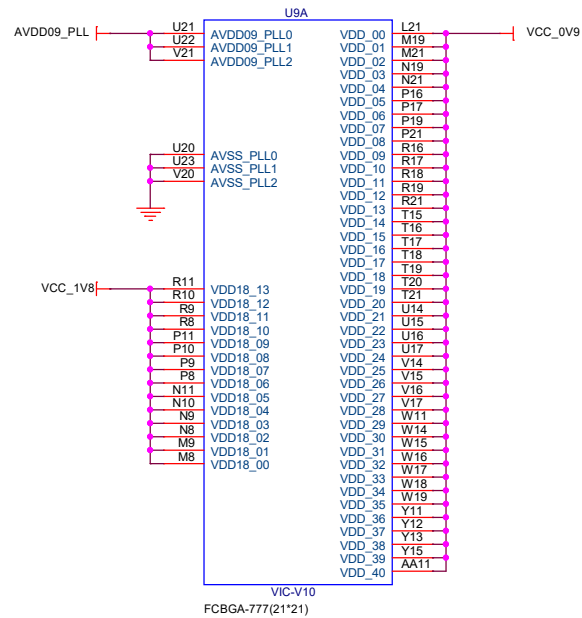
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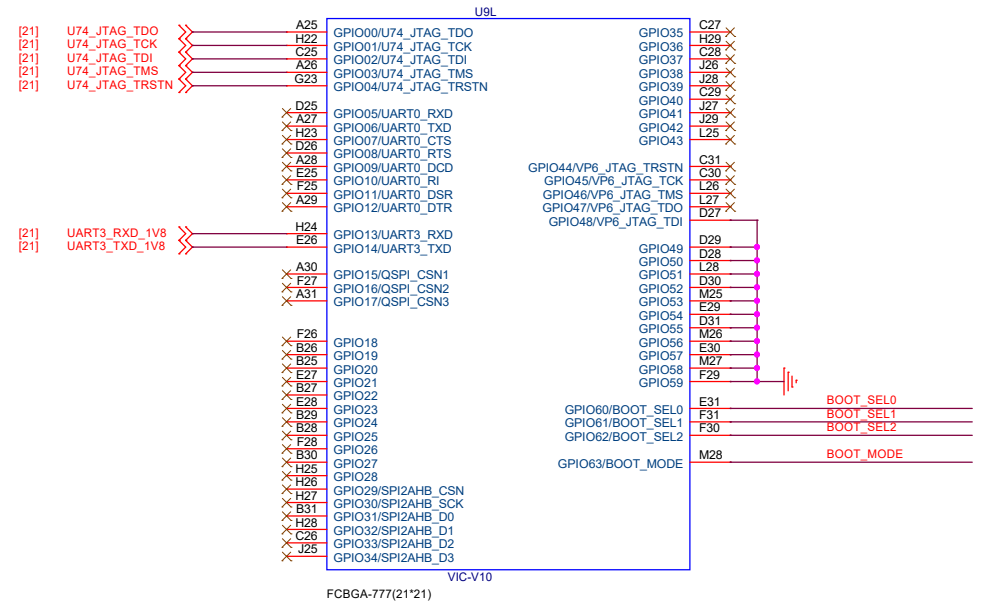
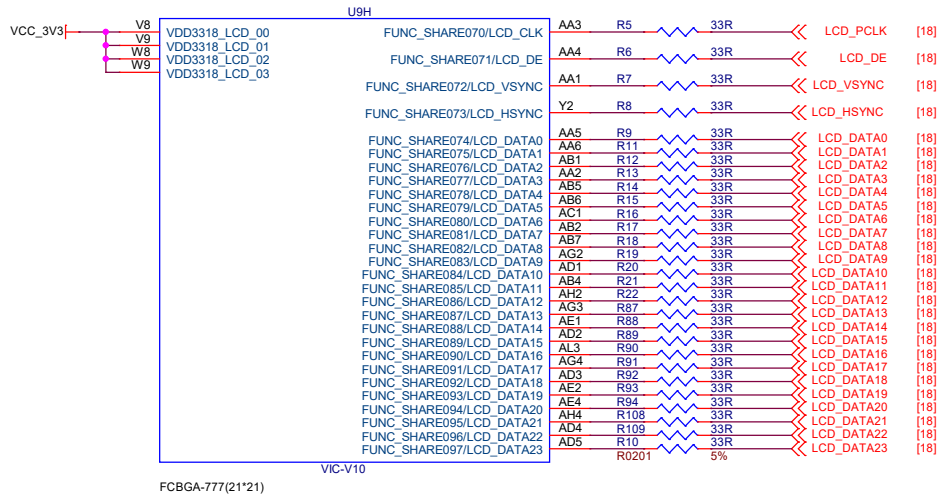


VIC Power

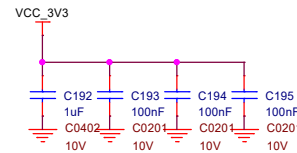
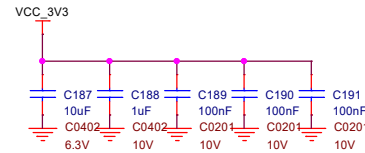
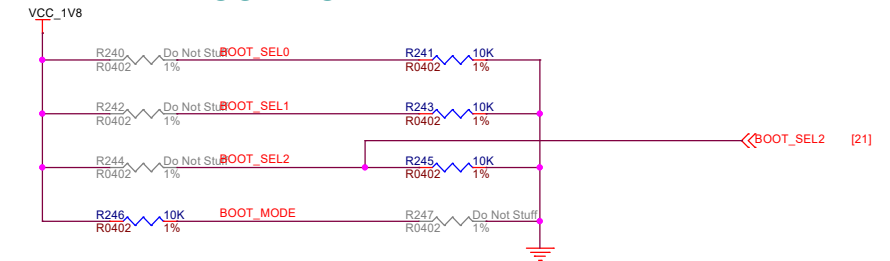
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VIC LCD&RGMII



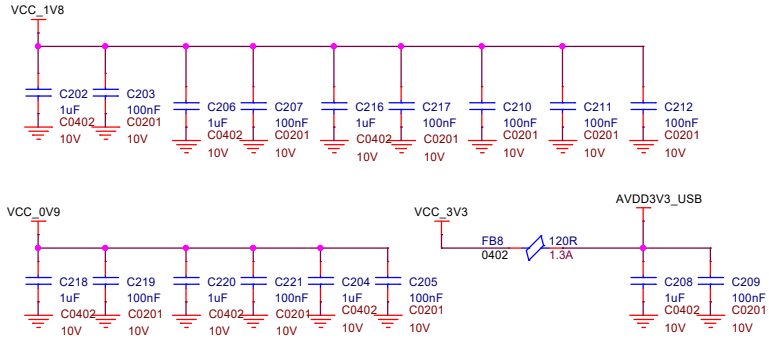
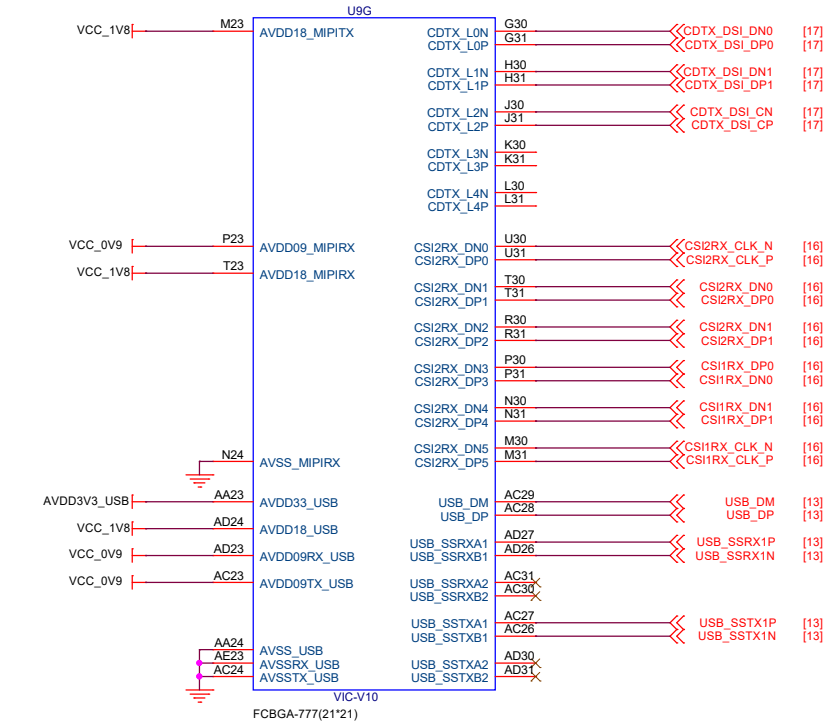
BOOT MODE



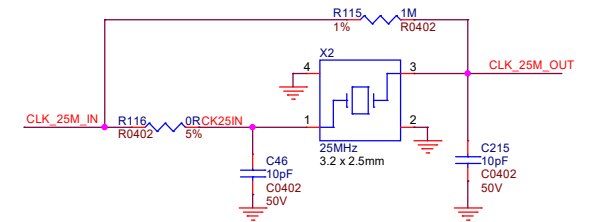
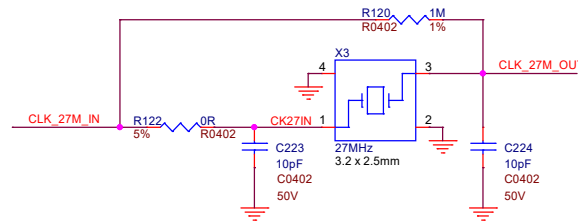
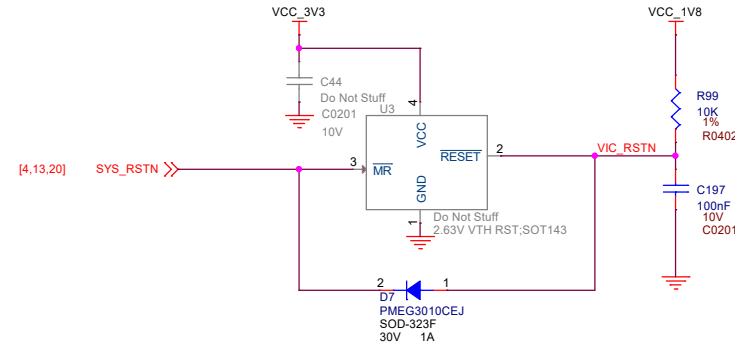
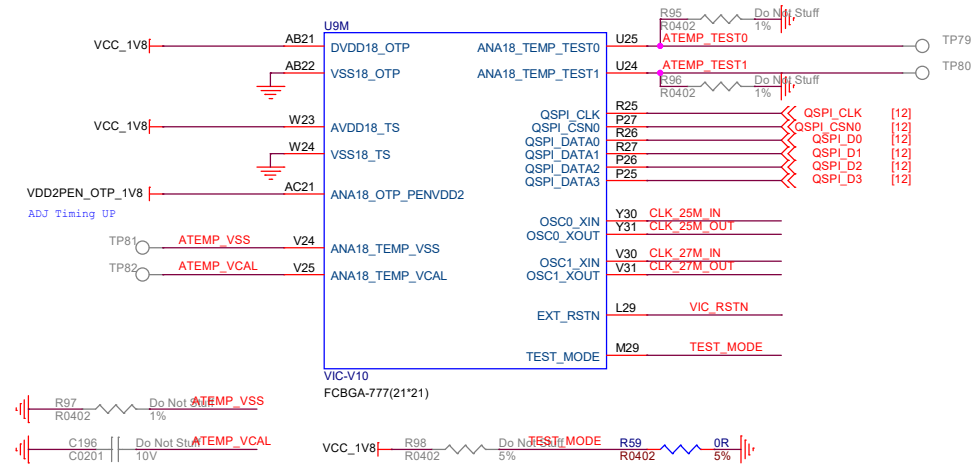
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VIC MIPI&USB

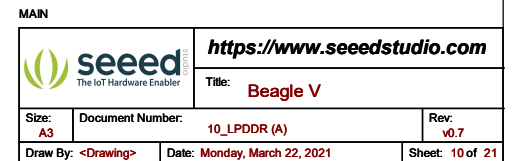


VIC Clock&

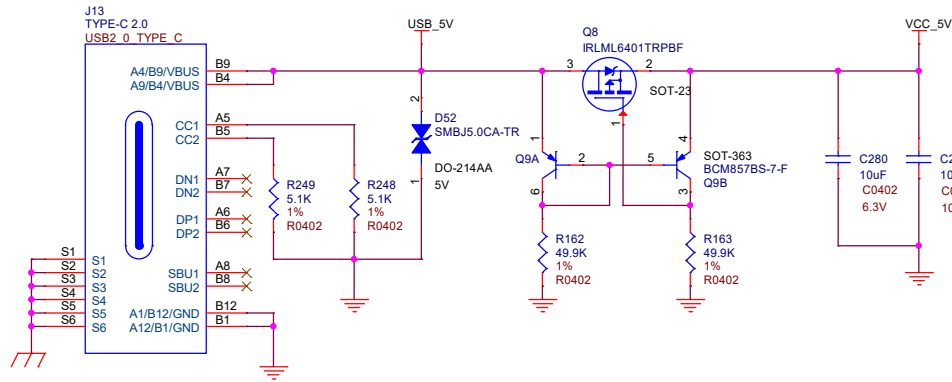


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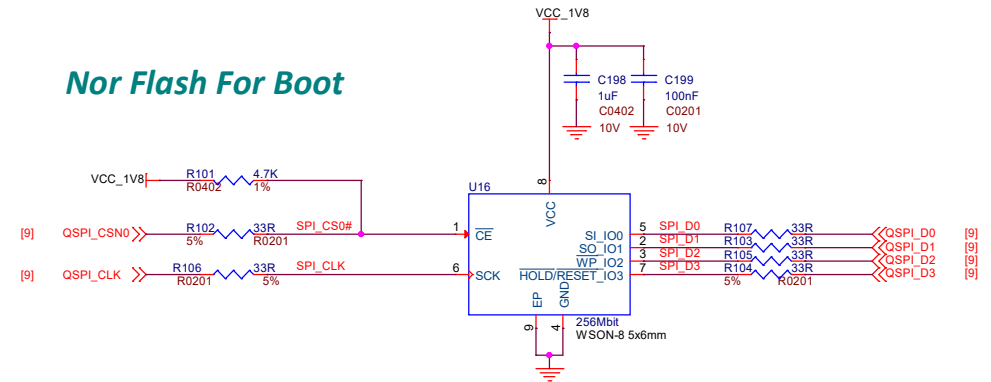
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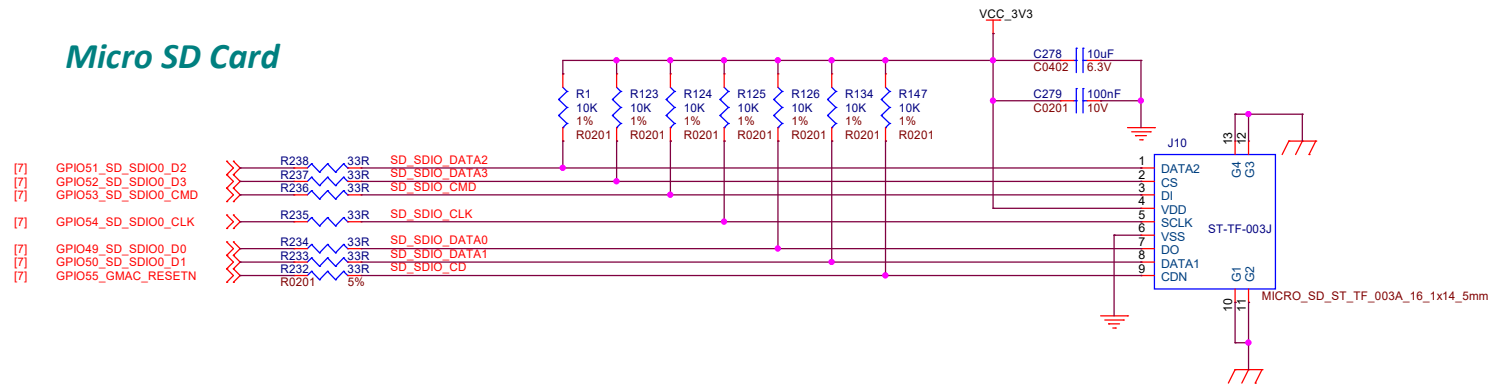
USB Tpye-C Power



Nor Flash For Boot

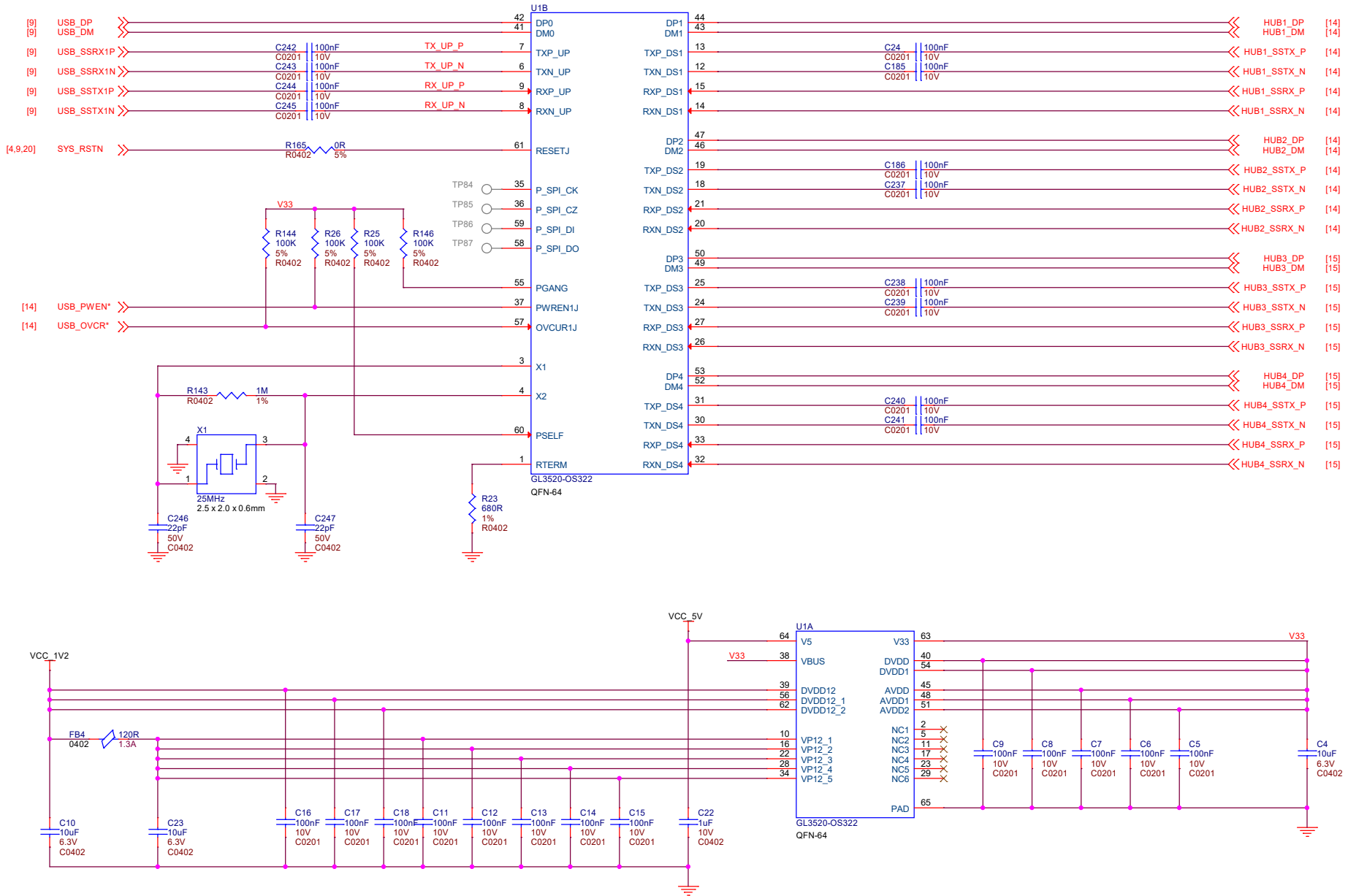


Micro SD Card



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USB 3.0 HUB
TBD



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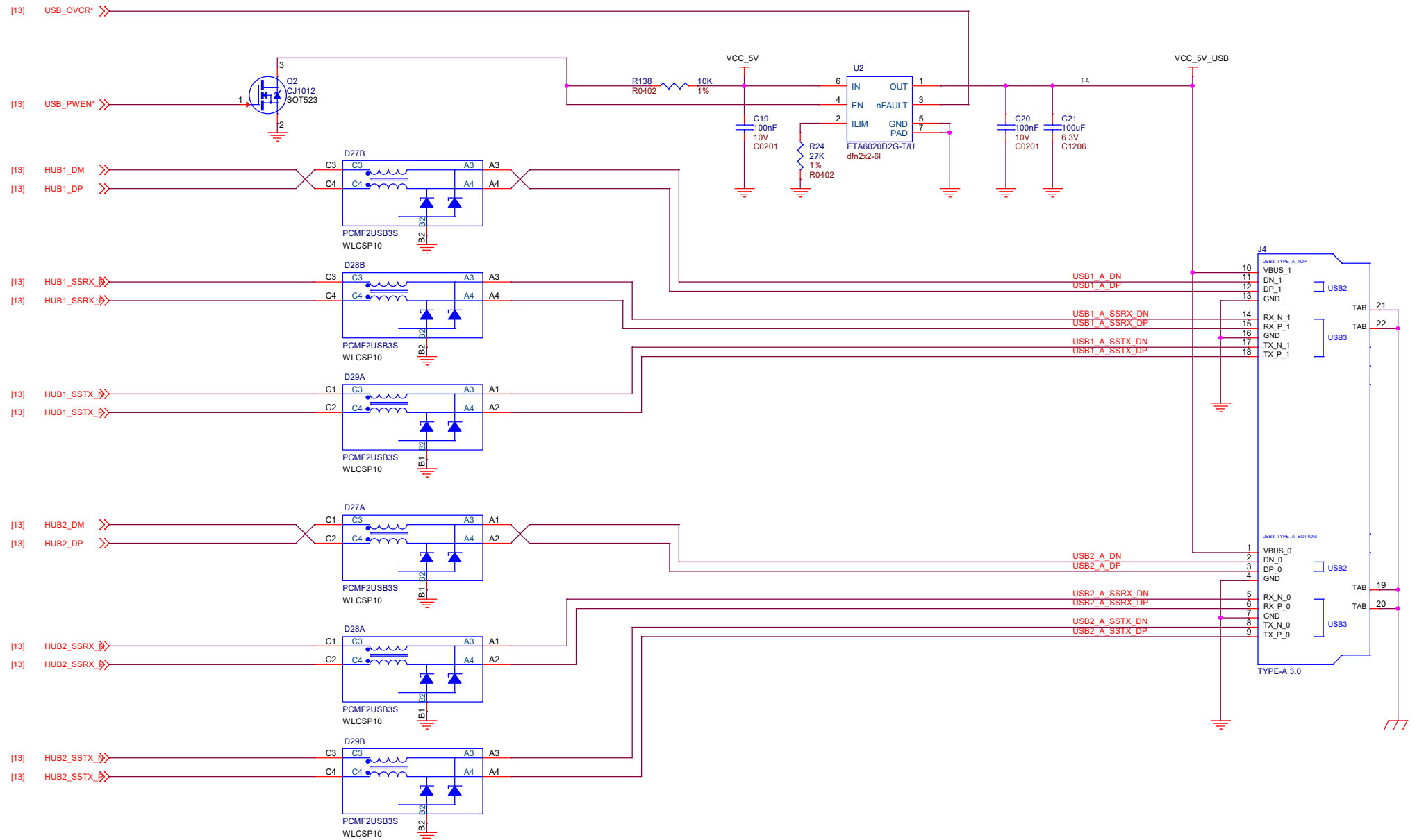
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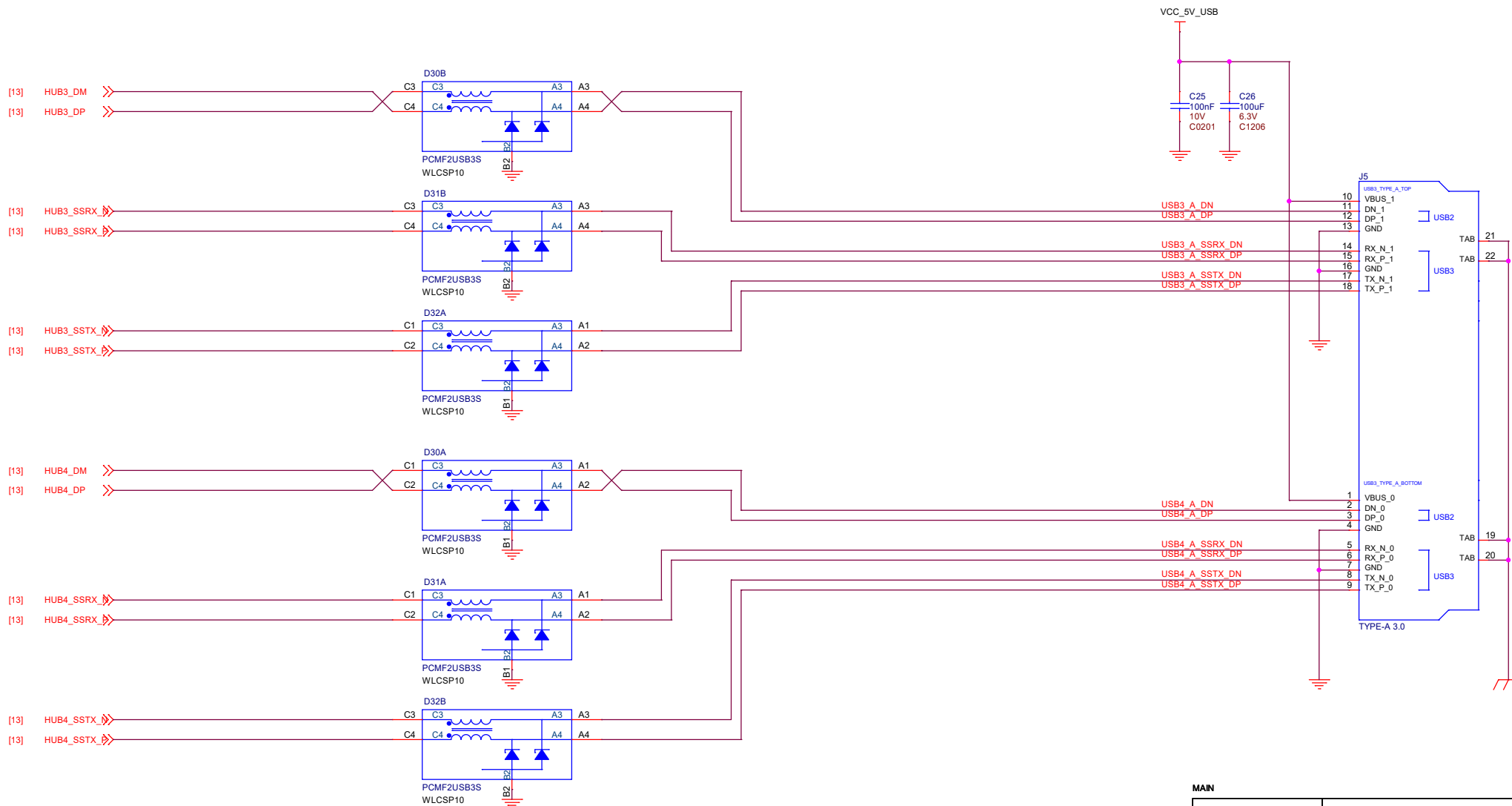
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USB 3.0 TYPE A x2



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CAMERA CONNECTOR

J1

Pin	Signal
1	CSi2RX_DN0
2	CSi2RX_DP0
3	CSi2RX_DN1
4	CSi2RX_DP1
5	CSi2RX_CLK_N
6	CSi2RX_CLK_P
7	GPIO58_CSi0_PWDN
8	GPIO62_I2C0_SCL
9	GPIO61_I2C0_SDA
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VCC_3V3

C1 100nF

C0201 10V

YL002-007 header2x15p_1d0_smd_YL002

J2

Pin	Signal
1	CSi1RX_DN0
2	CSi1RX_DP0
3	CSi1RX_DN1
4	CSi1RX_DP1
5	CSi1RX_CLK_N
6	CSi1RX_CLK_P
7	GPIO57_CSi1_PWDN
8	GPIO60_I2C2_SCL
9	GPIO59_I2C2_SDA
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VCC_3V3

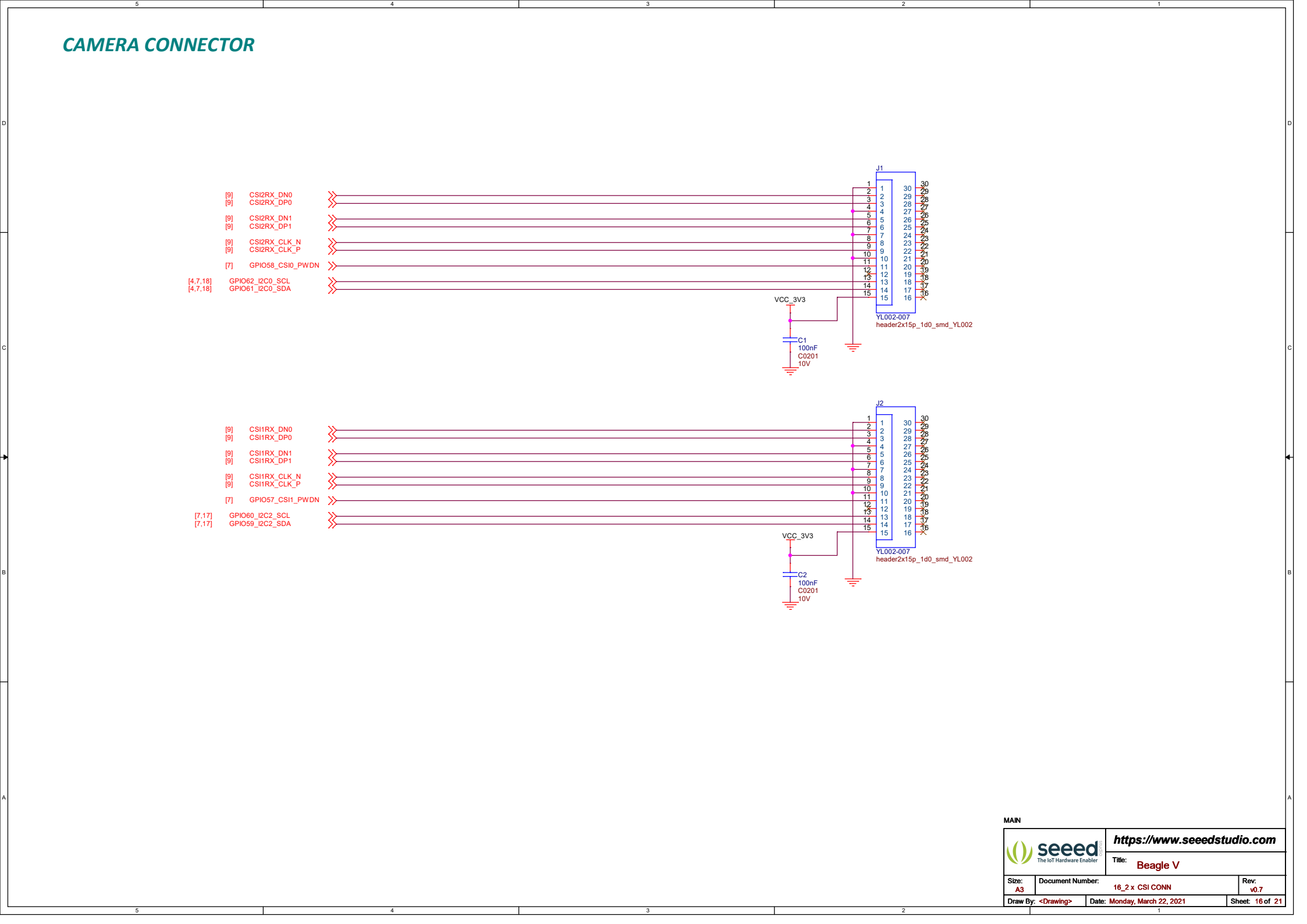
C2 100nF

C0201 10V

YL002-007 header2x15p_1d0_smd_YL002

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CAMERA CONNECTOR

J1

[9] CSI2RX_DN0
 [9] CSI2RX_DP0
 [9] CSI2RX_DN1
 [9] CSI2RX_DP1
 [9] CSI2RX_CLK_N
 [9] CSI2RX_CLK_P
 [7] GPIO58_CSI0_PWDN
 [4,7,18] GPIO62_I2C0_SCL
 [4,7,18] GPIO61_I2C0_SDA

VCC_3V3

C1 100nF
C0201 10V

YL002-007
header2x15p_1d0_smd_YL002

J2

[9] CSI1RX_DN0
 [9] CSI1RX_DP0
 [9] CSI1RX_DN1
 [9] CSI1RX_DP1
 [9] CSI1RX_CLK_N
 [9] CSI1RX_CLK_P
 [7] GPIO57_CSI1_PWDN
 [7,17] GPIO60_I2C2_SCL
 [7,17] GPIO59_I2C2_SDA

VCC_3V3

C2 100nF
C0201 10V

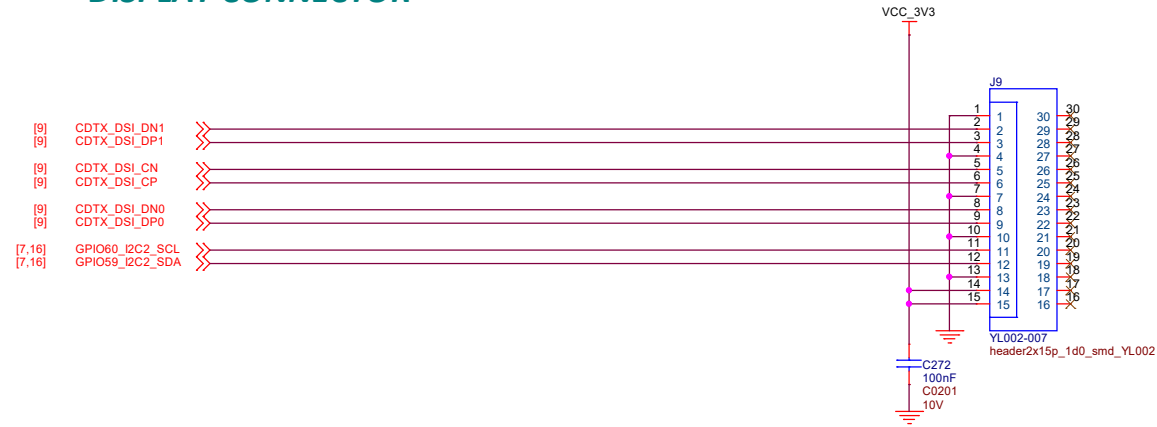
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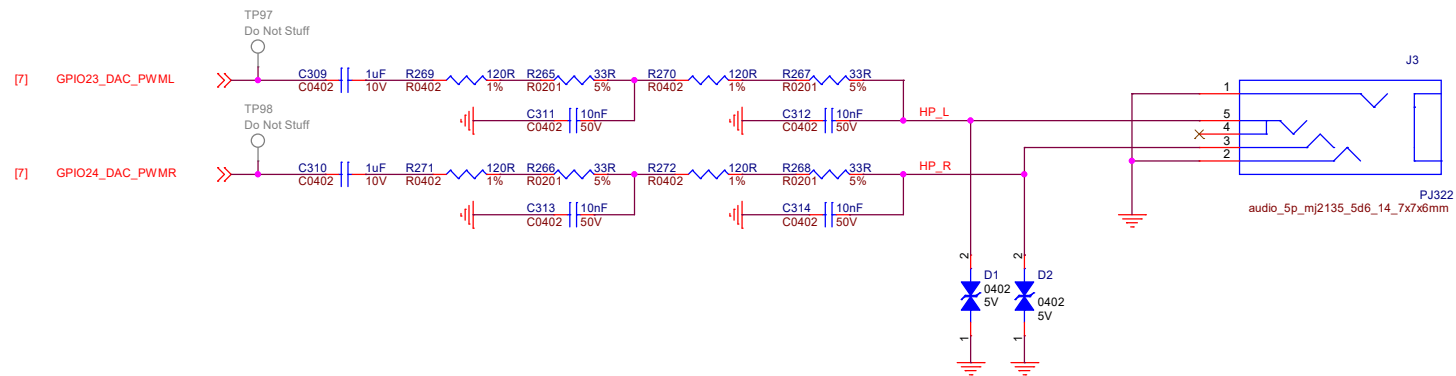
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DISPLAY CONNECTOR



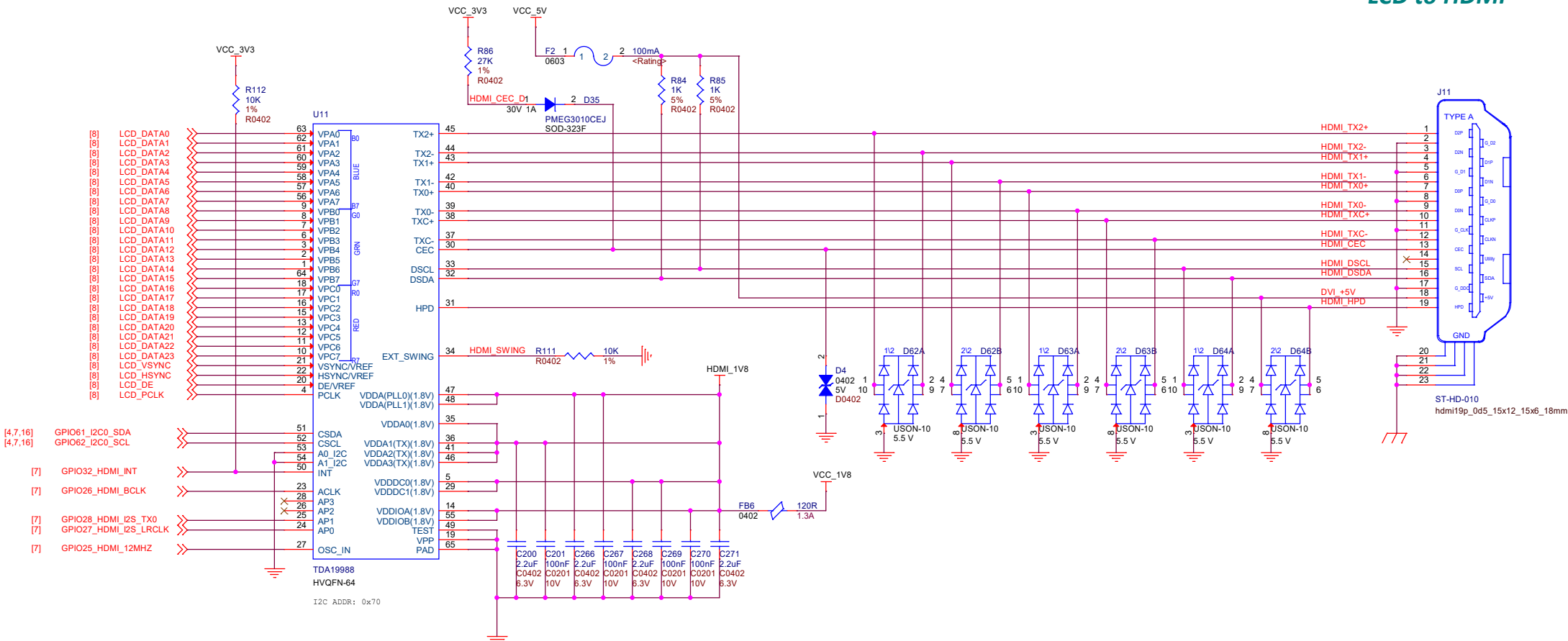
AUDIO



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LCD to HDMI



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Size:
A3

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MAIN



Title: **Beagle V**

19. WiFi, Bluetooth

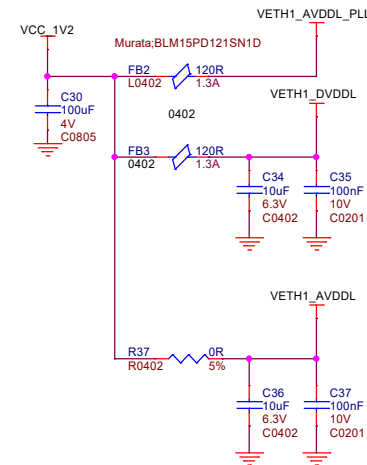
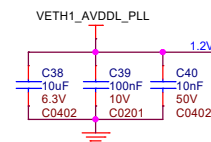
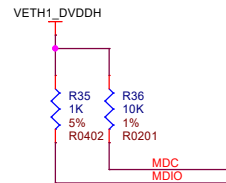
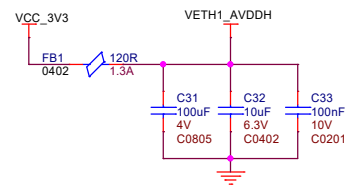
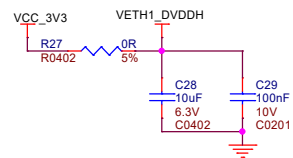
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Gigabit Ethernet



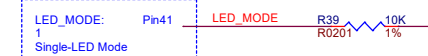
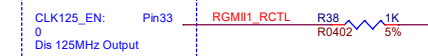
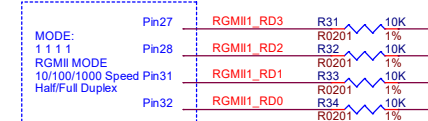
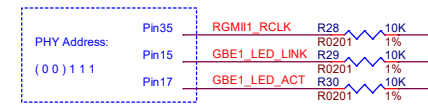
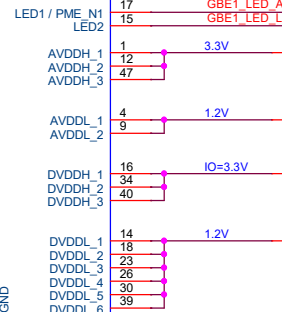
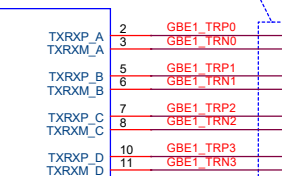
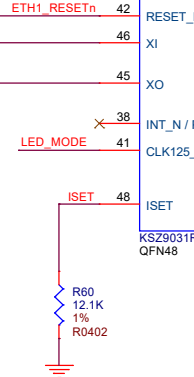
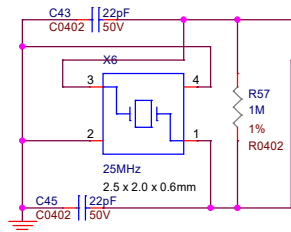
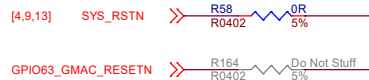
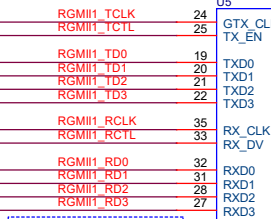
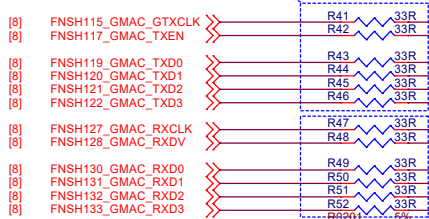
Layout Note:

The RGMII1 signals must be length-matched by TX and RX groups:

That is, the TX group should be matched within 300 Mil (7.62 mm), and the RX group should be matched within 300 Mil (7.62 mm). Total length should not exceed 1750 Mil (44.5 mm).

There is no requirement to match the TX and RX groups because their clocks are not related

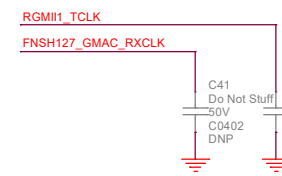
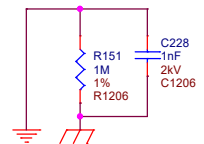
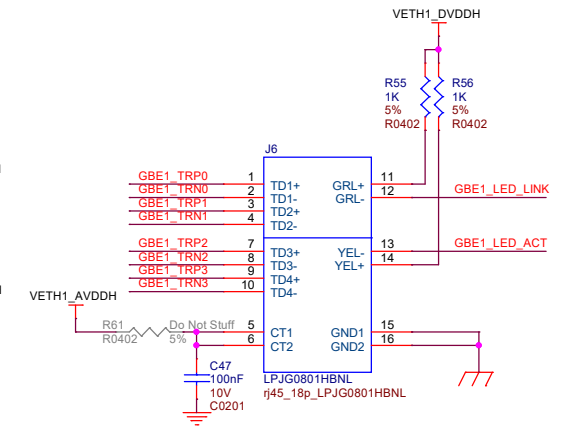
Layout Note:
Place R* Close To MPU.



Layout Note:

Max trace-length mismatch between GBE signals pairs should be no greater than ? mm.

100 ohms differential trace impedance.



MAIN



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Title: **Beagle V**

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Document Number: 20_10/100/1000 ETHERNET

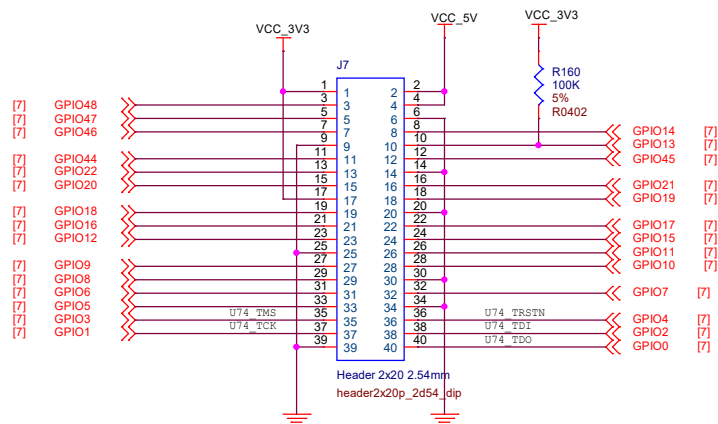
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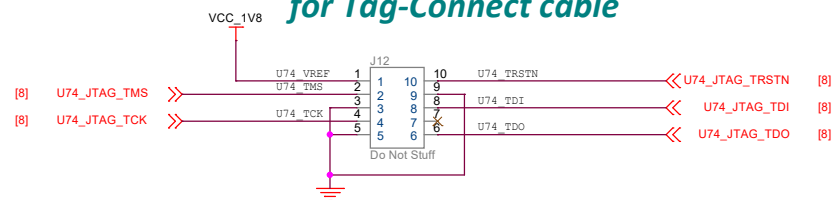
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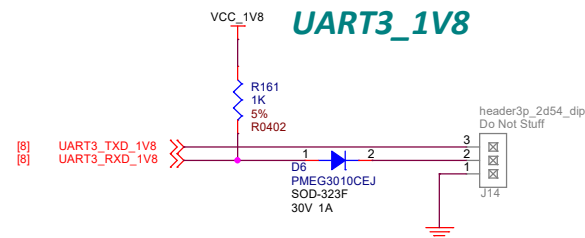
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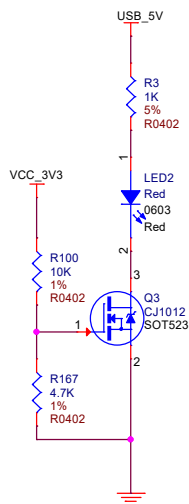
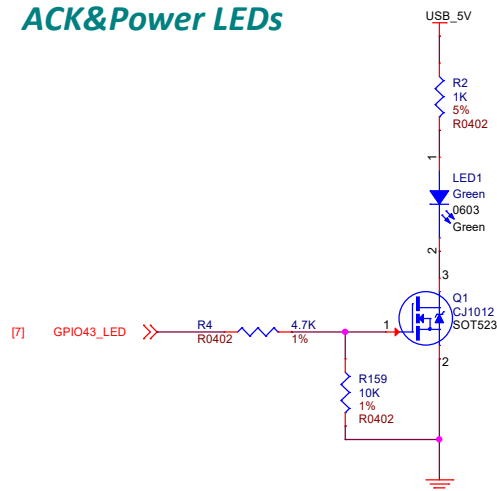
U74 JTAG 1V8 for Tag-Connect cable



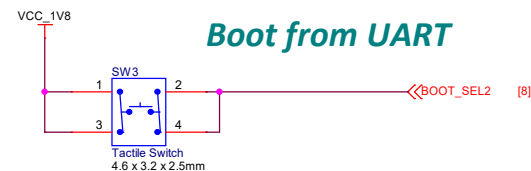
UART3_1V8



ACK&Power LEDs



Boot from UART



MAIN