CS224

Lab No. 6

Section No. 4

Your Full Name Alp Tuğrul Ağçalı

Bilkent ID 21801799

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1-)

Address is 31 bits because memory is 2GB (4Gb is 32 bits)

No.	Cache Size KB	N way cache	Word Size (no. of bits)	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Block Offset Size in bits[1]	Byte Offset Size in bits[2]	Block Replacement Policy Needed (Yes/No)
1	64	1	32	4	2^{12}	15	12	2	2	No.
2	64	2	32	4	2^{11}	16	11	2	2	Yes.
3	64	4	32	8	2^{9}	17	9	3	2	Yes.
4	64	Full	32	8	1	26	0	3	2	Yes.
9	128	1	16	4	2^{14}	14	14	2	1	No.
10	128	2	16	4	2^{13}	15	13	2	1	Yes.
11	128	4	16	16	2^{10}	16	10	4	1	Yes.
12	128	Full	16	16	1	26	0	4	1	Yes.

2-)

a.

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x24($0)	Compulsory	Hit	Hit	Hit	Hit
lw $t2, 0xAC($0)	Compulsory	Hit	Hit	Hit	Hit
lw $t3, 0xC8($0)	Compulsory	Hit	Hit	Hit	Hit

b.

Address is 32 bits because memory is 4GB.

We have 2 bit byte offset, 2 bit block offset because block size is 4 words and we have 1 set offset since we have 2 sets. So 32-2-2-1= 27. We have 27 bits as tag bits.

With V bit we have 27+1+(32*4) bit for each way. And 156*2 =312 bits in a set. 624 bits in total (there are 2 sets)

c.

2 and and 1 or gate for hits

2 equality comparator

1 4x1 mux and 1 2x1 mux to choose Word from block

3-)

a.

Instruction	**Iteration No.**				
	1	**2**	**3**	**4**	**5**
lw $t1, 0x24($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xAC($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0xC8($0)	Capacity	Capacity	Capacity	Capacity	Capacity

b.

We have 2 bit byte offset and 30 tag bits. (0 set offset because there is 1 set and 0 block offset because block size is 1 word) (N = 2 because memory size is 2 words)

30+32*1 = 62 bits for each way, 124 in a set. 124 in total since we have 1 set.

c.

2 and and 1 or gate for hits

2 equality comparator

2x1 mux to choose Word from block