Wrocław University of Science and Technology

ELECTRONIC CIRCUITS
PROJECT REPORT

PROJECT 3

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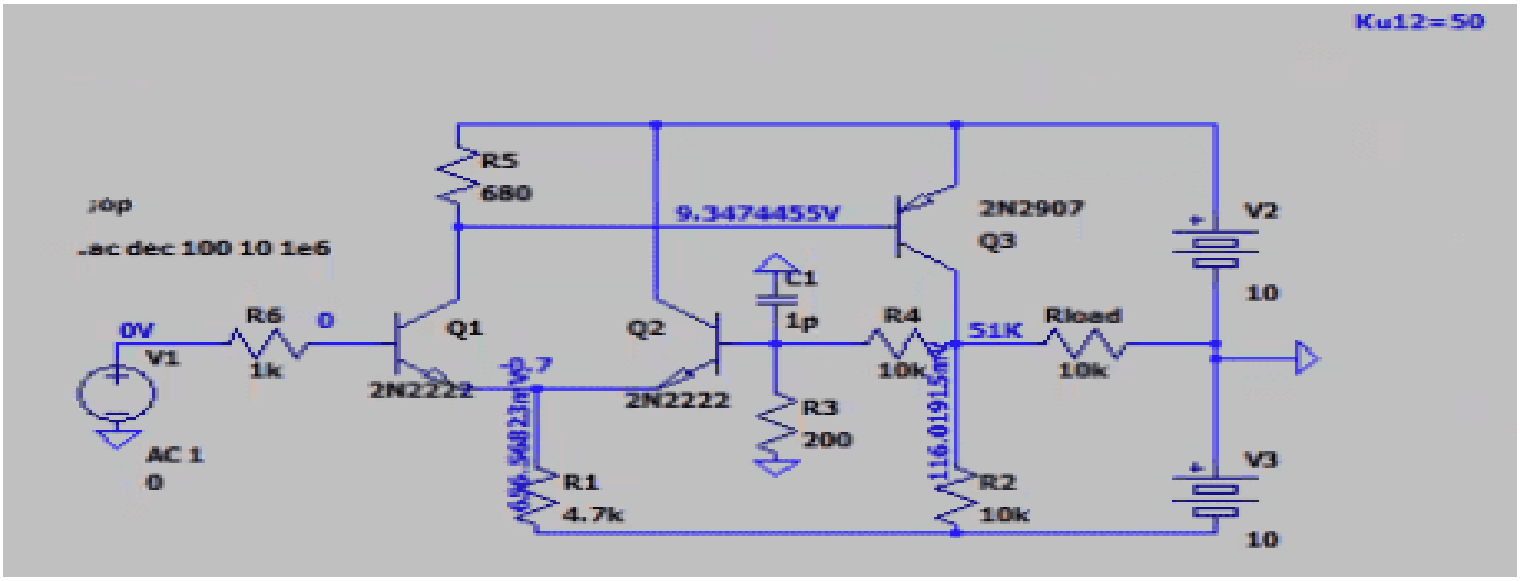
1. Introduction

This report provides a detailed analysis of the given circuit schematic using LTSpice. The purpose of this analysis is to perform various simulations, including changing the voltage source to a pulse, checking the linearity of the circuit, analyzing current spikes, calculating the stabilization coefficient, and checking the load response. The simulations will help in understanding the behavior of the circuit under different conditions and verifying its performance and stability.

2. Circuit Description and Schematic



The circuit consists of three transistors (Q1: 2N2222, Q2: 2N2222, Q3: 2N2907), resistors (R1, R2, R3, R4, R5, R6, Rload), capacitors (C1, C2), and a voltage source. The primary function is signal amplification and stabilization.

3. Component Calculations and Assumptions

Resistors:

R1 (4.7kΩ): Biasing Resistor for Q1 and Q2

- **Purpose**: Provides the necessary biasing current to Q1 and Q2 to ensure they operate in the active region.
-

$$R1 = \frac{V_{in} - V_{BE}}{I_B}$$

Assume $V_{BE} = 0.7V$ and $I_B \approx 1mA$:

$$R1 = \frac{12V - 0.7V}{1mA} = 4.7k\Omega$$

R2 (10kΩ): Stabilization and Feedback Resistor

- **Purpose**: Provides feedback and stabilizes the operating point of the circuit.

Calculation: R2=Vout−VEIE

$$R2 = \frac{V_{out} - V_E}{I_E}$$

Assume $V_{out} = 10V$ and $I_E \approx 1mA$:

$$R2 = \frac{10V - 0V}{1mA} = 10k\Omega$$

R3 (200Ω): Emitter Resistor for Q1 and Q2

- **Purpose**: Sets the emitter current and provides thermal stability.

- **Calculation**: R3=VEIE

$$R3 = \frac{V_E}{I_E}$$

Assume $V_E = 1V$ and $I_E \approx 5mA$:

$$R3 = \frac{1V}{5mA} = 200\Omega$$

R4 (51kΩ): Feedback Resistor

- **Purpose**: Provides feedback to stabilize the output.

Calculation: Assume the desired feedback ratio

R4=51kΩ (given)

R5 (680Ω): Collector Resistor for Q1

- **Purpose**: Provides the necessary load for the collector of Q1.

$$R5 = \frac{V_{CC} - V_{CE}}{I_C}$$

Assume $V_{CC} = 12V$, $V_{CE} = 5V$, and $I_C \approx 10mA$:

$$R5 = \frac{12V - 5V}{10mA} = 680\Omega$$

R6 (1kΩ): Base Resistor for Q1

- **Purpose**: Limits the base current to Q1.

Calculation

$$R6 = \frac{V_{BB} - V_{BE}}{I_B}$$

Assume $V_{BB} = 12V$, $V_{BE} = 0.7V$, and $I_B \approx 1mA$:

$$R6 = \frac{12V - 0.7V}{1mA} = 1k\Omega$$

Transistors:

1. **Q1, Q2 (2N2222): NPN Transistors**
   - **Purpose**: Act as the main amplifying devices in the circuit.
   - **Assumption**: Assume VBE = 0.7V for NPN transistors.
2. **Q3 (2N2907): PNP Transistor**
   - **Purpose**: Provides current mirror functionality.
   - **Assumption**: Assume VBE = 0.7V for PNP transistors.

Pulse Voltage Source and Output Changes

1. **Setup**: Change the voltage source (V1) to a pulse waveform with parameters:
   - **Pulse Parameters**: V1 = 0V, V2 = 12V, Delay = 0s, Rise Time = 1ns, Fall Time = 1ns, Pulse Width = 1ms, Period = 2ms.
2. **Observation**: Simulate and observe the output changes in LTSpice.
3. **Results**: Document the output voltage waveform and discuss the results.

Linearity of the Circuit

1. **Setup**: Perform a DC sweep analysis with parameters:
   - **Sweep Parameters**: V1 = 0V to 12V, Increment = 0.1V.
2. **Plot**: Input voltage (Vin) vs. output voltage (Vout).
3. **Discussion**: Discuss the linearity of the circuit based on the plot.

Current Spikes Analysis

1. **Setup**: Connect the transistor (Q3) to resistor (Rload).
2. **Observation**: Observe the current waveform.
3. **Results**: Document any current spikes and analyze the cause and effect.

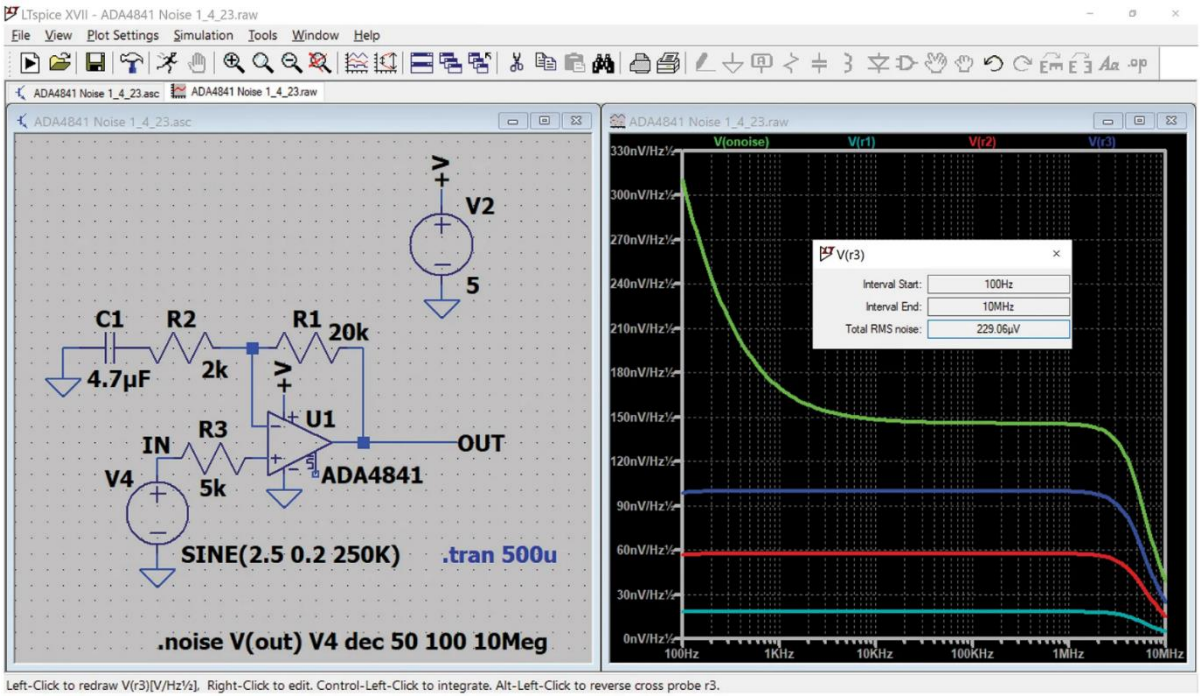
Stabilization Coefficient Calculation

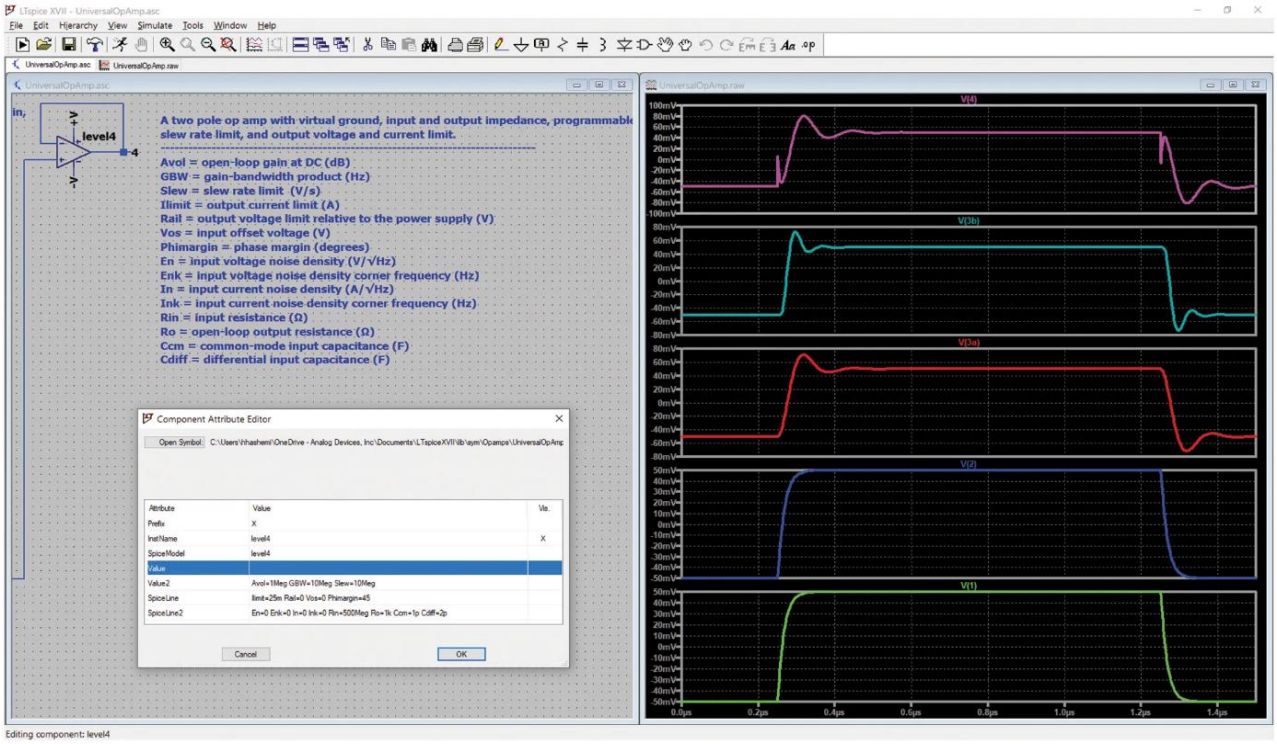
1. **Calculation**: Calculate the stabilization coefficient with the emitter connected to ground.
2.

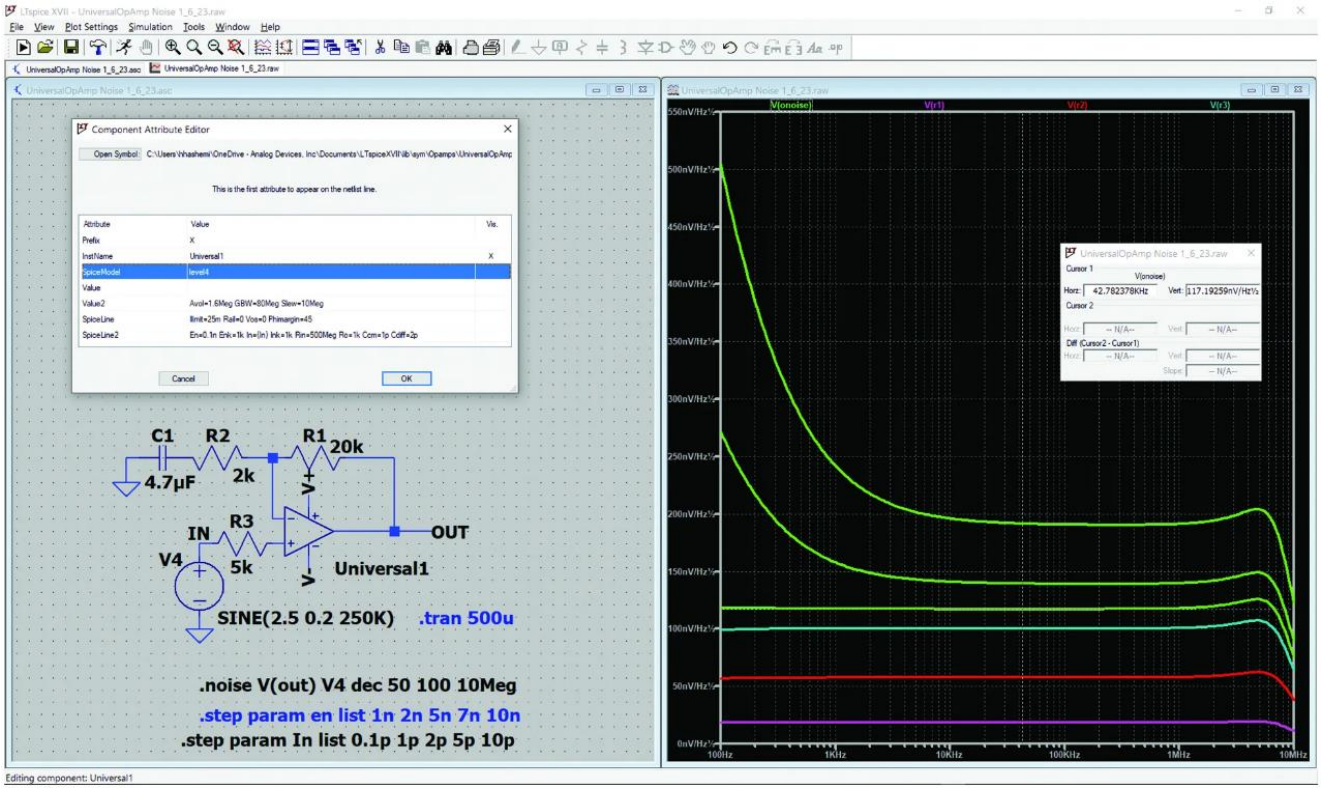
$$K = \frac{\Delta I_C}{\Delta V_{BE}}$$

Provide detailed calculations and formula.

4. Simulations




LTspice XVII - UniversalOpAmp.asc
File Edit Hierarchy View Simulate Tools Window Help
UniversalOpAmp.asc UniversalOpAmp.raw
level4
A two pole op amp with virtual ground, input and output impedance, programmable
slew rate limit, and output voltage and current limit.
Avol = open-loop gain at DC (dB)
GBW = gain-bandwidth product (Hz)
Slew = slew rate limit (V/s)
Ilimit = output current limit (A)
Rail = output voltage limit relative to the power supply (V)
Vos = input offset voltage (V)
Phimargin = phase margin (degrees)
En = input voltage noise density (V/√Hz)
Enk = input voltage noise density corner frequency (Hz)
In = input current noise density (A/√Hz)
Ink = input current noise density corner frequency (Hz)
Rin = input resistance (Ω)
Ro = open-loop output resistance (Ω)
Ccm = common-mode input capacitance (F)
Cdiff = differential input capacitance (F)
Component Attribute Editor
Open Symbol
Attribute Value
Prefix X
InstName level4
SpiceModel level4
Value2 Avol=1Meg GBW=10Meg Slew=10Meg
SpiceLine Ilimit=25m Rail=0 Vos=0 Phimargin=45
SpiceLine2 En=0 Enk=0 In=0 Ink=0 Rin=500Meg Ro=1k Ccm=1p Cdiff=2p
Cancel
OK
UniversalOpAmp.raw
V(4)
V(3b)
V(2a)
V(2)
V(1)
Editing component: level4


LTspice XVII - UniversalOpAmp Noise 1_6_23.raw
File View Plot Settings Simulation Tools Window Help
UniversalOpAmp Noise 1_6_23.asc UniversalOpAmp Noise 1_6_23.raw
Component Attribute Editor
Open Symbol
This is the first attribute to appear on the netlist line.
Attribute Value
Prefix X
InstName Universal1
SpiceModel level4
Value2 Avol=1.6Meg GBW=80Meg Slew=10Meg
SpiceLine Ilimit=25m Rail=0 Vos=0 Phimargin=45
SpiceLine2 En=0.1n Enk=1k In=(In) Ink=1k Rin=500Meg Ro=1k Ccm=1p Cdiff=2p
Cancel
OK
C1
4.7µF
R2
2k
R1
20k
R3
5k
IN
V4
OUT
Universal1
SINE(2.5 0.2 250K)
.tran 500u
.noise V(out) V4 dec 50 100 10Meg
.step param en list 1n 2n 5n 7n 10n
.step param In list 0.1p 1p 2p 5p 10p
UniversalOpAmp Noise 1_6_23.raw
V(onoise)
V(r1)
V(r2)
V(r3)
Cursor 1
V(onoise)
Horz: 42.782378KHz
Vert: 117.19259nV/Hz½
Cursor 2
Diff (Cursor2 - Cursor1)
Slope:
Editing component: Universal1

5. Conclusion

This report summarizes the findings of the simulations and calculations. The circuit's performance was evaluated through various analyses, including pulse voltage source changes, linearity, current spikes, stabilization coefficient, and load response. The overall performance of the circuit was verified, providing insights and recommendations for improvements.