

浙江大学

本科实验报告

课程名称: 计算机组成

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2020 年 3 月 17 日

Lab 3 – Integrated SOC Design

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Course: Computer Organization

Date: 2020-03-17

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1. Method and Experimental Steps

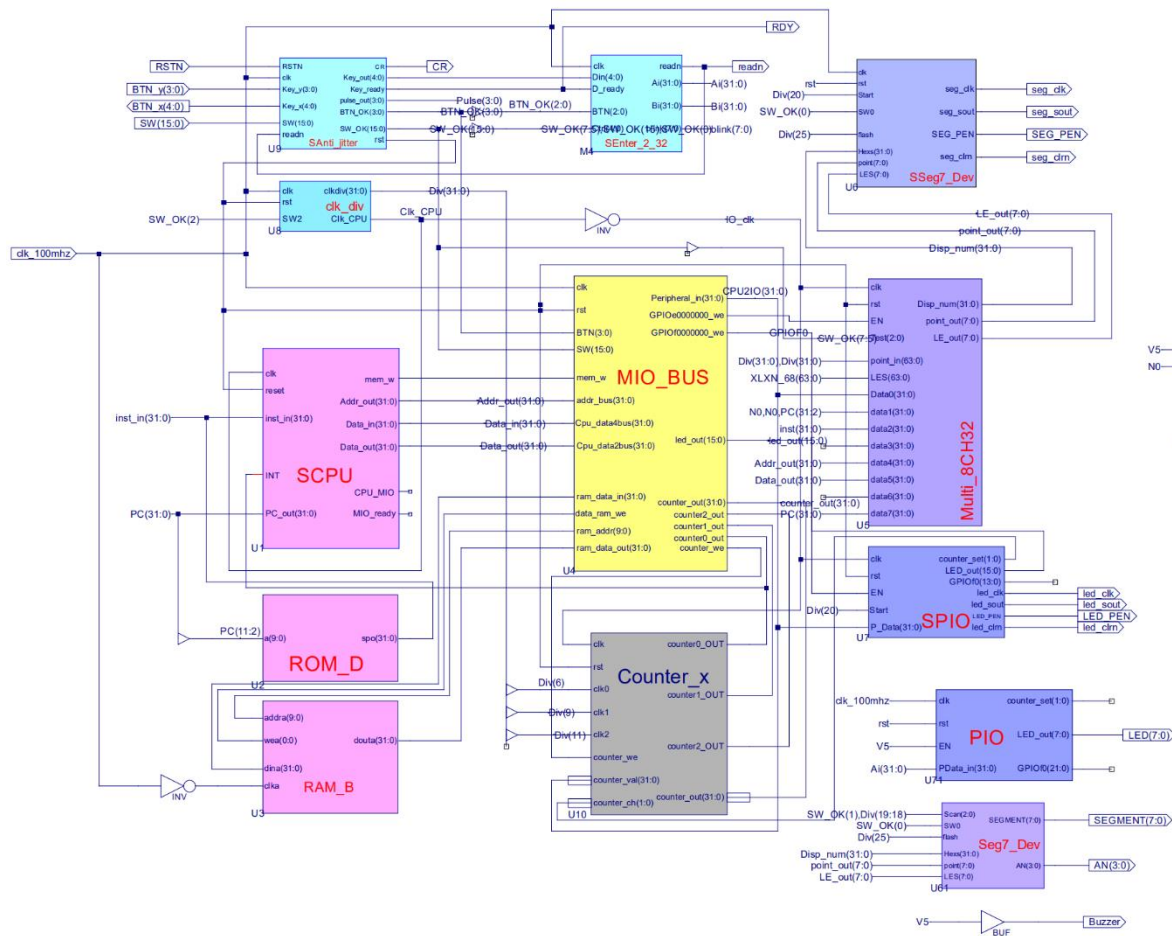


Figure 1 - topMod.sch

This depicts the completion of lab 3. In this lab, I practiced the usage of the IP core and attempted to understand the SOC system. The three new modules that were introduced into this lab are SCPU, MIO_BUS, and Counter_x. MIO_BUS handles input and output, where it takes data from the CPU and routes it to memory. SCPU can perform R-Type, I-Type and J-Type instructions. The ROM is an internal memory unit in the FPGA and stores the MIPS instructions needed for operations. For output, the Multi_8CH32 signals to the seven-segment display, similarly to what has been done in prior labs and in the Digital Logic Design course. The .ucf for this program came from the provided courseware and is linked to topMod.sch. Synthesis had minimal warnings, and implementation was successful. A programmable file has been generated and is ready for testing.

Figure 2 - TANGANNAYONGQI3180300155_03

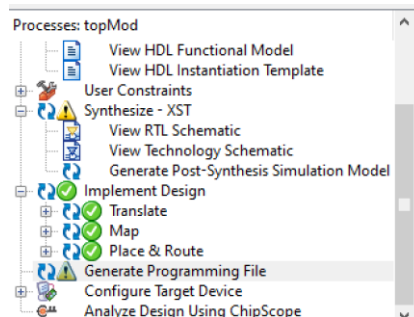


Figure 3 - .bit file generation



Figure 4 - .bit file found in directory

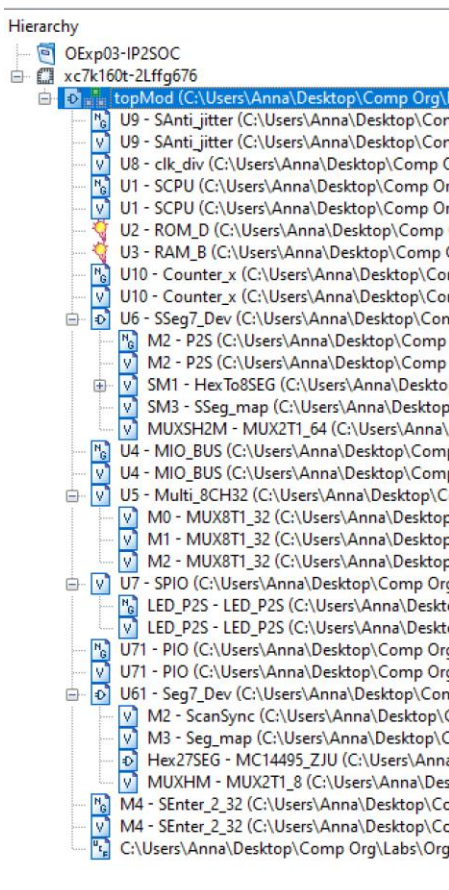


Figure 5 - file hierarchy

All modules and .ucf that were used for lab 3 came from courseware and lab 2. No modification was done.

2. Simulations and Observations

There was no specification in the given instructions whether a simulation was needed. I have decided to forgo the simulation since this lab is just a modification of the first two labs.

3. Conclusion

For this week's lab, I struggled more with understanding the general concepts rather than technically implementing it onto the ISE. I was able to make the connection as to how the new modules would work in conjunction with the rest of components, but I would still like to see a comparison or a gradual functionality progression. This is not possible now, because I have not been able to implement the testing file onto the SWORD board. In my Digital Logic Course from last semester, we explored the concept of using interrupt signals to process inputs, and how a BUS works. I look forward to re-exploring these concepts and designing an ALU in the next experiments.

4. Source Code

All modules and components were either retrieved from lab 1, lab 2 or directly taken from the given files. No modification in code was performed.