

Lab 1- Design of Multiplexer and Application of SWORD Board Displays (MINI REPORT)

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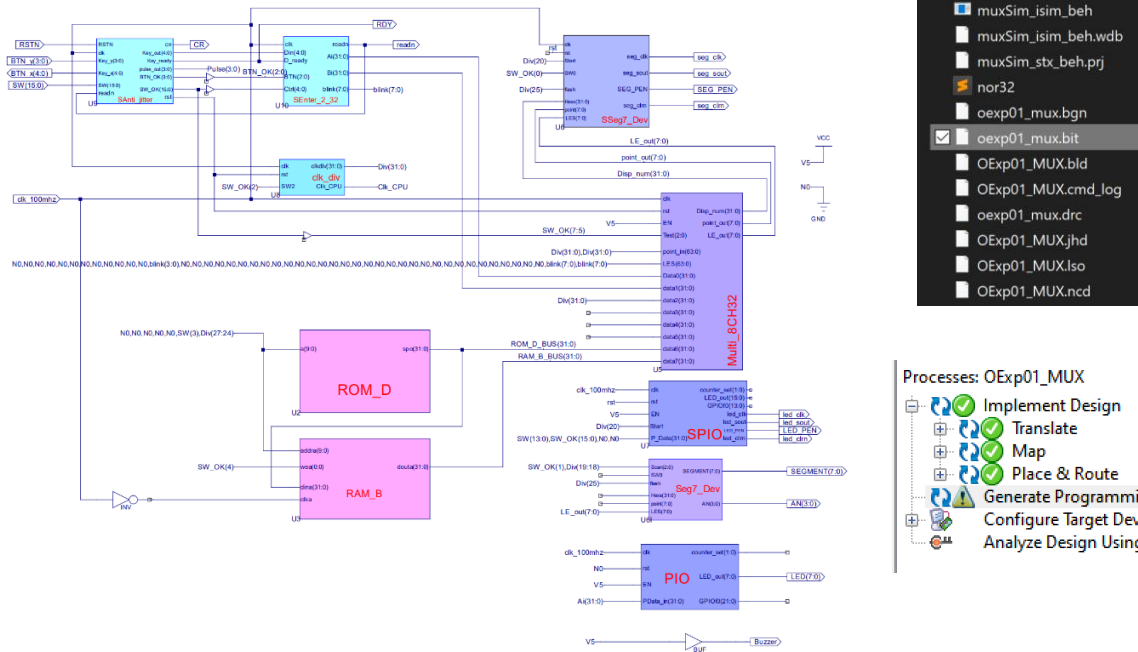
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Course: Computer Organization

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This depicts the completion of lab 1. All modules in the schematic above were sourced from course material, except for ROM_D and RAM_B. These two components were generated by the IP CORE generator, and settings referenced from the slides were used. The ucf provided in the courseware was used and is linked to the top module of this project. There were minimal warning messages with the synthesis process, but implementation was successful with zero errors and zero warnings. A programmable file has been generated and is ready for testing on the SWORD board.



The picture above shows a simulation of the 8 to 32-bit signal multiplexer. As shown, it is functioning correctly and is consistent with its outputs.