Quiz 3

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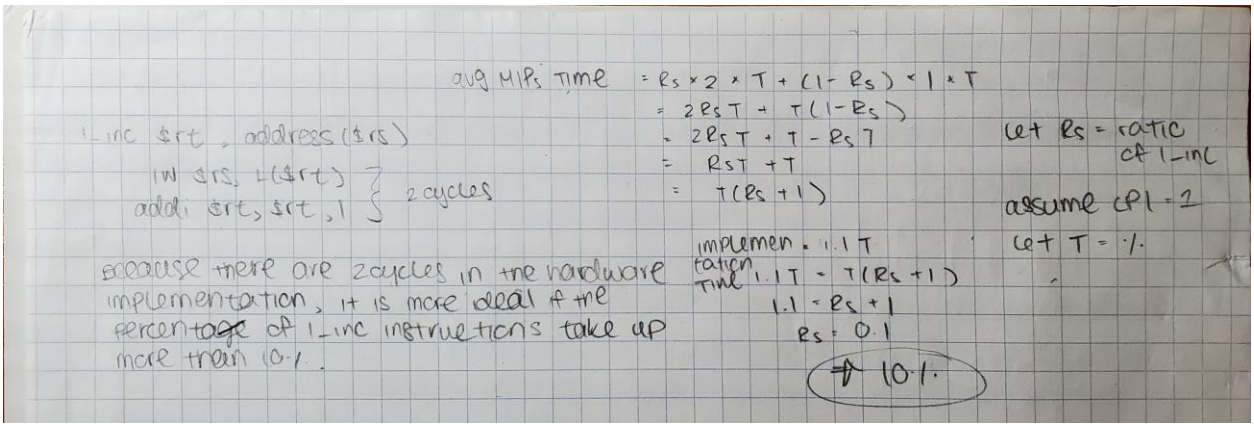
1) C (ROM)
2) B
3) False, CPU consists of controller and datapath
4) True
5) C (60%)

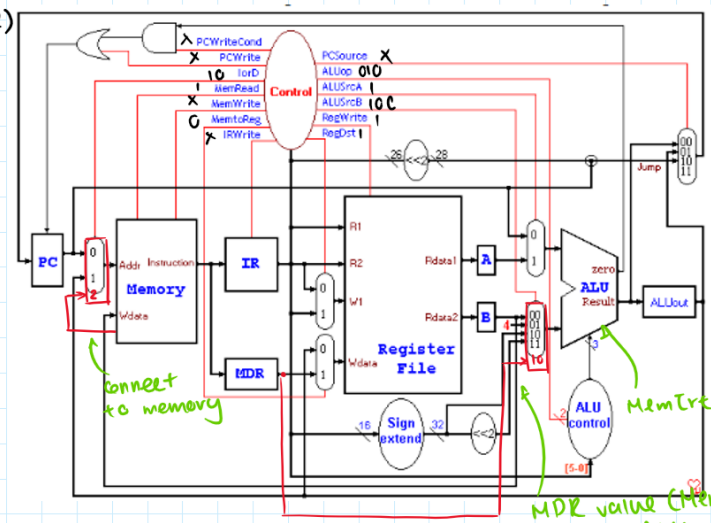
6)



10%

7)

2)



basically, fetch the instruction from IR and read the registers.

using the memory address, read the value of reg B.

add the value to reg A.

write back to destination.

1) instruction Format

ADDM rd rs rt

Field	op	rs	rt	rd	shamt	func
BITS	[31:26]	[25:21]	[25:21]	[20:16]	[10:6]	[5:0]

Not used

3)

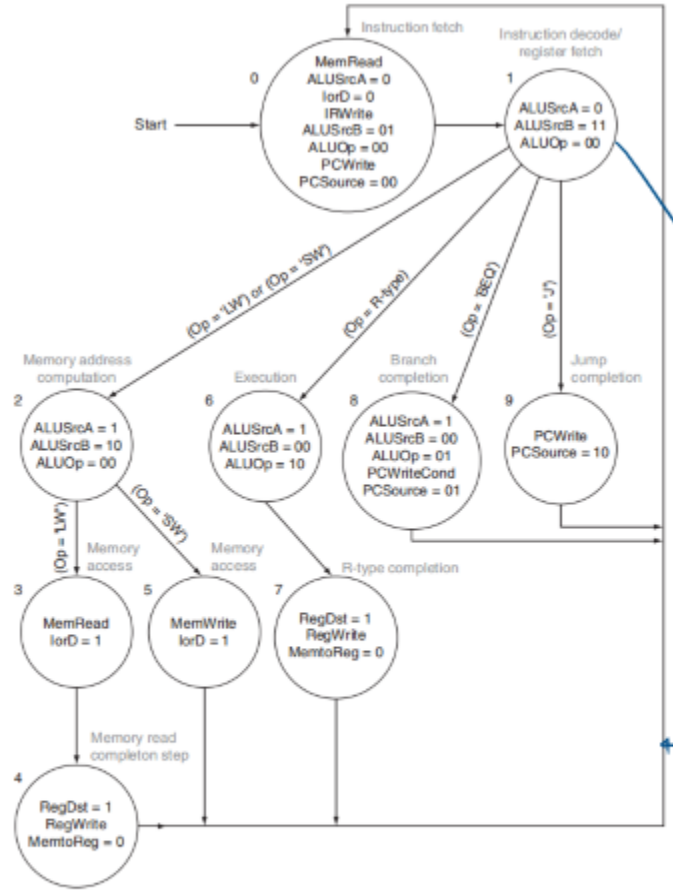


FIGURE 5.38 The complete finite state machine control for the datapath shown in Figure 5.28. The labels on the arcs are conditions that are tested to determine which state is the next state; when the next state is unconditional, no label is given. The labels inside the nodes indicate the output signals asserted during that state; we always specify the setting of a multiplexor control signal if the correct operation requires it. Hence, in some states a multiplexor control will be set to 0.