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*****
/

/*
* helloworld.c: simple test application
*
* This application configures UART 16550 to baud rate 9600.
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
*
* -----
* | UART TYPE   BAUD RATE                                |
* -----
*   uartns550   9600
*   uartlite    Configurable only in HW design
*   ps7_uart    115200 (configured by bootrom/bsp)
*/

#include <stdio.h>
#include <stdlib.h>
#include "xaxidma.h"
#include "xparameters.h"
#include "platform.h"
#include <xtime_l.h>
#define INP_SIZE 8
#define MATSIZE 8
float Find_input_A[8][8];
float Find_input_B[8][8];
float Find_outputps[8][8];
float Find_output1[8][8];
float Find_output2[8][8];
float Find_output3[8][8];
float Find_output4[8][8];
float Find_output5[8][8];

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void input()
{
    printf("What is going on\n");
    for (int i=0;i<INP_SIZE;i++)
    {
        for(int j=0; j<INP_SIZE; j++)
        {
            Find_input_A[i][j]= (rand()%20);
            Find_input_B[i][j]= (rand()%20);
        }
    }
}

void PS()
{
    float Find_outputs[INP_SIZE][INP_SIZE];
    XTime time_PS_start , time_PS_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_PS_start);
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            float res=0;
            for(int index=0; index<MATSIZE; index++)
            {
                res+=Find_input_A[i][index]*Find_input_B[index][j];
            }
            Find_outputs[i][j]=res;
        }
    }
    XTime_GetTime(&time_PS_end);
    printf("\n-----PS FPGA EXECUTION TIME-----\n");
    float time_PS = 0;
    time_PS = (float)1.0 *
(time_PS_end - time_PS_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for
PS in Micro-Seconds : %f\n" , time_PS);
    for(int row=0; row<MATSIZE; row++)
    {
        for( int col=0; col<MATSIZE; col++)
        {
            printf("Input A %f, Input B
%f\n",Find_input_A[row][col],Find_input_B[row][col]);
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)

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        {
            printf("Output %f\n",Find_outputtps[row][col]);
        }
    }
}

int Find_ACP1()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_0_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
    // for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
    // {
    //     printf("Input %f \n ",DMA_input[i]);
    // }
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);
    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);

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        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
        }
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
        }
        XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
        for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
        {
            printf("Output  :
%f\n",Find_output_DMA[i]);
        }
        index=0;
        for(int row=0; row<MATSIZE; row++)
        {
            for(int col=0; col<MATSIZE; col++)
            {
                Find_output1[row][col]=Find_out
tput_DMA[index];

                index++;
            }
        }

        return 0;
    }
int Find_ACP2()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_1_DEVICE_ID);

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status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
if(status != XST_SUCCESS)
{
    printf("ACP DMA Init Failed\t\n");
    return XST_FAILURE;
}
XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
//    for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
//    {
//        printf("Input %f \n ",DMA_input[i]);
//    }
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);
    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

    while(status!=0x00000002)
    {

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        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    }
    XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
        for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
        {
            printf("Output  :
%f\n",Find_output_DMA[i]);
        }
        index=0;
        for(int row=0; row<MATSIZE; row++)
        {
            for(int col=0; col<MATSIZE; col++)
            {
                Find_output2[row][col]=Find_ou
tput_DMA[index];

                index++;
            }
        }

        return 0;
    }
int Find_ACP3()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_2_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
        XTime_SetTime(0);
        XTime_GetTime(&time_ACP_start);
        int index=0;
        for(int row=0; row<MATSIZE; row++)
        {

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        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
    // for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
    // {
    //     printf("Input %f \n ",DMA_input[i]);
    // }

    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);

    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    }
    XTime_GetTime(&time_ACP_end);
    printf("\n-----ACP FPGA EXECUTION TIME----
-----\n");

    float time_ACPFPGA = 0;
    time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
    for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
    {

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                                                                    printf("Output  :
%f\n",Find_output_DMA[i]);
    }
    index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            Find_output3[row][col]=Find_ou
tput_DMA[index];

            index++;
        }
    }

    return 0;
}
int Find_ACP4()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_3_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
}

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    }
//      for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
//      {
//          printf("Input %f \n ",DMA_input[i]);
//      }

    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);

    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    }
    XTime_GetTime(&time_ACP_end);
    printf("\n-----ACP FPGA EXECUTION TIME----
-----\n");

    float time_ACPFPGA = 0;
    time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
    for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
    {
        printf("Output  :
%f\n",Find_output_DMA[i]);
    }
    index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            Find_output4[row][col]=Find_out
tput_DMA[index];

            index++;
        }
    }
}

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        return 0;
    }
}
int Find_ACP5()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_4_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
        XTime_SetTime(0);
        XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
    // for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
    // {
    //     printf("Input %f \n ",DMA_input[i]);
    // }
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);
    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    while(status!=0x00000002)

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        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
        }
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
        }
        XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
        for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
        {
            printf("Output :
%f\n",Find_output_DMA[i]);
        }
        index=0;
        for(int row=0; row<MATSIZE; row++)
        {
            for(int col=0; col<MATSIZE; col++)
            {
                Find_output5[row][col]=Find_ou
tput_DMA[index];

                index++;
            }
        }

        return 0;
    }
int compare1()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output1[i][j]!=Find_outputs[i][j])
            {
                return 0;
            }
        }
    }
}

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    }
    return 1;
}
int compare2()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output2[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}
int compare3()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output3[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}
int compare4()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output4[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}
int compare5()
{
    for(int i=0; i<MATSIZE; i++)

```

```

{
    for(int j=0; j<MATSIZE; j++)
    {
        if(Find_output5[i][j]!=Find_outputs[i][j])
        {
            return 0;
        }
    }
}
return 1;
}
int main()
{
    init_platform();
    input();
    PS();
    Find_ACP1();
    Find_ACP2();
    Find_ACP3();
    Find_ACP4();
    Find_ACP5();
    int ans=compare1();
    int ans1=compare2();
    int ans2=compare3();
    int ans3=compare4();
    int ans4=compare5();
    if(ans==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all\n");
    }
    if(ans1==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all");
    }
    if(ans2==1)
    {
        printf("You are great\n");
    }
    else
    {

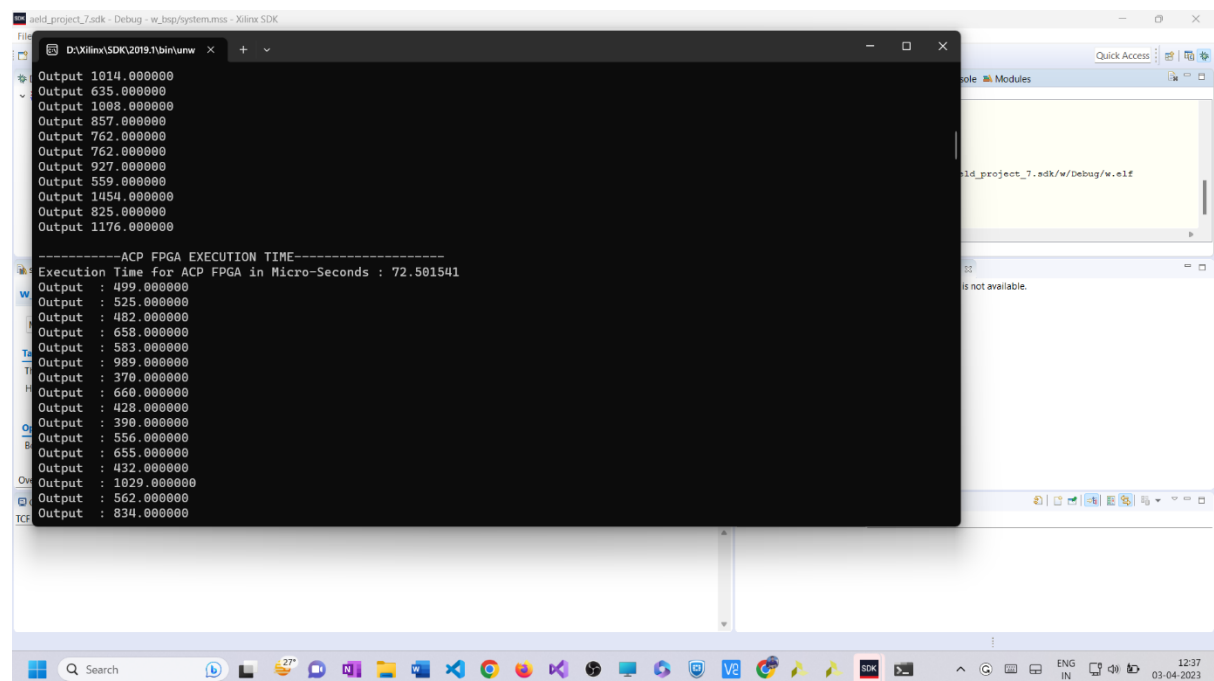
```

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        printf("No good at all\n");
    }
    if(ans3==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all\n");
    }
    if(ans4==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all");
    }
    cleanup_platform();
    return 0;
}

```

Jtagterminal:-



```
aeid_project_7_sdk - Debug - w_bsp/system.mss - Xilinx SDK
D:\Xilinx\SDK2019.1\bin\unw
Output : 590.000000
Output : 1014.000000
Output : 635.000000
Output : 1008.000000
Output : 857.000000
Output : 762.000000
Output : 762.000000
Output : 927.000000
Output : 559.000000
Output : 1454.000000
Output : 825.000000
Output : 1176.000000

-----ACP FPGA EXECUTION TIME-----
Execution Time for ACP FPGA in Micro-Seconds : 9.593846
Output : 499.000000
Output : 525.000000
Output : 482.000000
Output : 658.000000
Output : 583.000000
Output : 989.000000
Output : 370.000000
Output : 660.000000
Output : 428.000000
Output : 390.000000
Output : 556.000000
Output : 655.000000
Output : 432.000000
Output : 1029.000000
Output : 562.000000
```

```
aeid_project_7_sdk - Debug - w_bsp/system.mss - Xilinx SDK
D:\Xilinx\SDK2019.1\bin\unw
Output : 635.000000
Output : 1008.000000
Output : 857.000000
Output : 762.000000
Output : 762.000000
Output : 927.000000
Output : 559.000000
Output : 1454.000000
Output : 825.000000
Output : 1176.000000

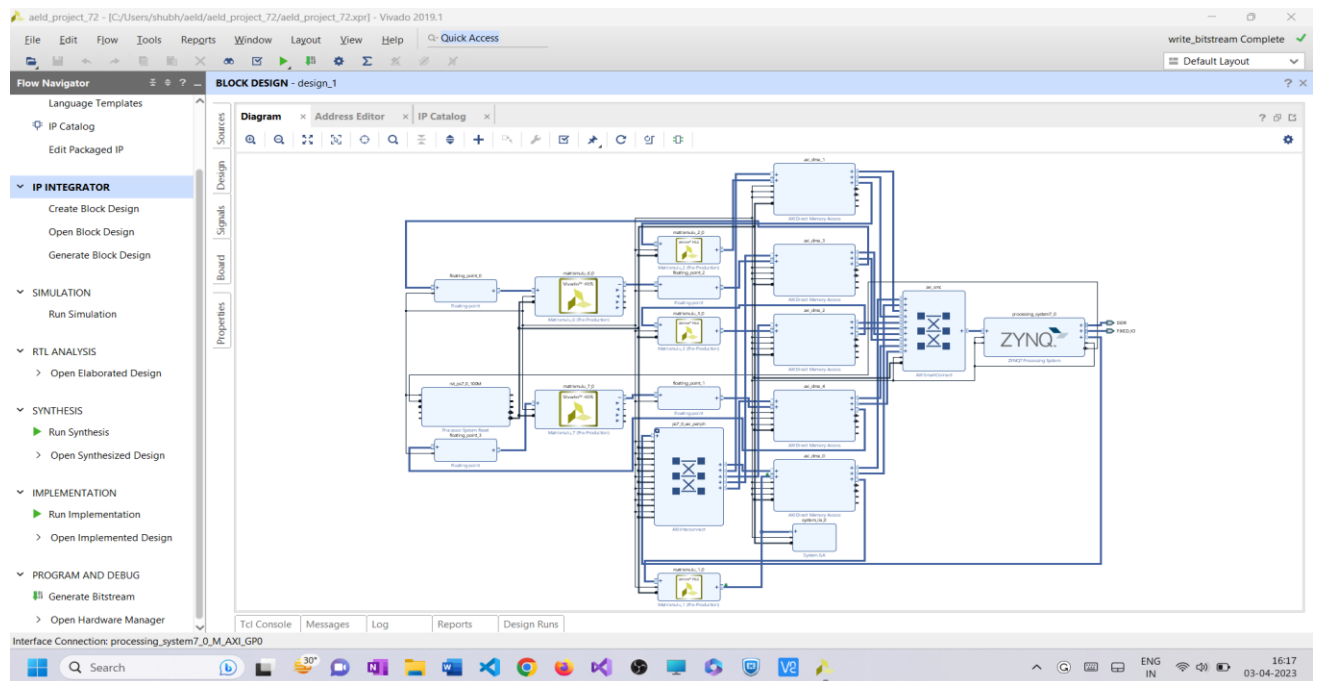
-----ACP FPGA EXECUTION TIME-----
Execution Time for ACP FPGA in Micro-Seconds : 9.406154
Output : 499.000000
Output : 525.000000
Output : 482.000000
Output : 658.000000
Output : 583.000000
Output : 989.000000
Output : 370.000000
Output : 660.000000
Output : 428.000000
Output : 390.000000
Output : 556.000000
Output : 655.000000
Output : 432.000000
Output : 1029.000000
Output : 562.000000
Output : 834.000000
Output : 526.000000
```



```
aeid_project_7_sdk - Debug - w_hsp/system.mss - Xilinx SDK
D:\Xilinx\SDK2019.1\bin\unw
Output : 673.000000
Output : 654.000000
Output : 566.000000
Output : 773.000000
Output : 590.000000
Output : 1014.000000
Output : 635.000000
Output : 1008.000000
Output : 857.000000
Output : 762.000000
Output : 762.000000
Output : 927.000000
Output : 559.000000
Output : 1454.000000
Output : 825.000000
Output : 1176.000000
-----ACP FPGA EXECUTION TIME-----
Execution Time for ACP FPGA in Micro-Seconds : 9.507692
Output : 499.000000
Output : 525.000000
Output : 482.000000
Output : 658.000000
Output : 583.000000
Output : 989.000000
Output : 370.000000
Output : 660.000000
Output : 428.000000
Output : 390.000000
Output : 556.000000
```

```
aeid_project_7_sdk - Debug - w_hsp/system.mss - Xilinx SDK
D:\Xilinx\SDK2019.1\bin\unw
Output : 566.000000
Output : 773.000000
Output : 590.000000
Output : 1014.000000
Output : 635.000000
Output : 1008.000000
Output : 857.000000
Output : 762.000000
Output : 762.000000
Output : 927.000000
Output : 559.000000
Output : 1454.000000
Output : 825.000000
Output : 1176.000000
-----ACP FPGA EXECUTION TIME-----
Execution Time for ACP FPGA in Micro-Seconds : 9.541538
Output : 499.000000
Output : 525.000000
Output : 482.000000
Output : 658.000000
Output : 583.000000
Output : 989.000000
Output : 370.000000
Output : 660.000000
Output : 428.000000
Output : 390.000000
Output : 556.000000
Output : 655.000000
Output : 432.000000
```

Block Diagram:-



Code: -

```
/*
 *
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 */
```

```

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*
*****
/

/*
 * helloworld.c: simple test application
 *
 * This application configures UART 16550 to baud rate 9600.
 * PS7 UART (Zynq) is not initialized by this application, since
 * bootrom/bsp configures it to baud rate 115200
 *
 * -----
 * | UART TYPE   BAUD RATE                                |
 * -----
 *   uartns550   9600
 *   uartlite    Configurable only in HW design
 *   ps7_uart    115200 (configured by bootrom/bsp)
 */

#include <stdio.h>
#include <stdlib.h>
#include "xaxidma.h"
#include "xparameters.h"
#include "platform.h"
#include<xtime_l.h>
#define INP_SIZE 8
#define MATSIZE 8
float Find_input_A[8][8];
float Find_input_B[8][8];
float Find_outputps[8][8];
float Find_output1[8][8];
float Find_output2[8][8];
float Find_output3[8][8];
float Find_output4[8][8];
float Find_output5[8][8];
void input()
{
    printf("What is going on\n");
    for (int i=0;i<INP_SIZE;i++)
    {
        for(int j=0; j<INP_SIZE; j++)
        {
            Find_input_A[i][j]= (rand()%20);
            Find_input_B[i][j]= (rand()%20);
        }
    }
}

```

```

    }
}

void PS()
{
    float Find_outputps[INP_SIZE][INP_SIZE];
    XTime time_PS_start , time_PS_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_PS_start);
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            float res=0;
            for(int index=0; index<MATSIZE; index++)
            {
                res+=Find_input_A[i][index]*Find_input_B[index][j];
            }
            Find_outputps[i][j]=res;
        }
    }
    XTime_GetTime(&time_PS_end);
    printf("\n-----PS FPGA EXECUTION TIME-----\n");
    float time_PS = 0;
    time_PS = (float)1.0 *
(time_PS_end - time_PS_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for
PS in Micro-Seconds : %f\n" , time_PS);
    for(int row=0; row<MATSIZE; row++)
    {
        for( int col=0; col<MATSIZE; col++)
        {
            printf("Input A %f, Input B
%f\n",Find_input_A[row][col],Find_input_B[row][col]);
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            printf("Output %f\n",Find_outputps[row][col]);
        }
    }
}

int Find_ACP1()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];

```

```

int status;
XAxisDma_Config *DMA_confptracp; //DMA configuration pointer
XAxisDma AxisDMAacp; // DMA instance pointer
DMA_confptracp = XAxisDma_LookupConfig(XPAR_AXI_DMA_0_DEVICE_ID);
status = XAxisDma_CfgInitialize(&AxisDMAacp, DMA_confptracp);
if(status != XST_SUCCESS)
{
    printf("ACP DMA Init Failed\t\n");
    return XST_FAILURE;
}
XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
//    for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
//    {
//        printf("Input %f \n ",DMA_input[i]);
//    }
    status = XAxisDma_SimpleTransfer(&AxisDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);
    status = XAxisDma_SimpleTransfer(&AxisDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxisDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    while(status!=0x00000002)
    {
        status = XAxisDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxisDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

```

```

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
        }
        XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
        for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
        {
            printf("Output  :
%f\n",Find_output_DMA[i]);
        }
        index=0;
        for(int row=0; row<MATSIZE; row++)
        {
            for(int col=0; col<MATSIZE; col++)
            {
                Find_output1[row][col]=Find_ou
tput_DMA[index];

                index++;
            }
        }

        return 0;
    }
int Find_ACP2()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_1_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);

```

```

    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
//    for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
//    {
//        printf("Input %f \n ",DMA_input[i]);
//    }
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);
    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    }
    XTime_GetTime(&time_ACP_end);
    printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

    float time_ACPFPGA = 0;
    time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);

```

```

        printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
        for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
        {
            printf("Output  :
%f\n",Find_output_DMA[i]);
        }
        index=0;
        for(int row=0; row<MATSIZE; row++)
        {
            for(int col=0; col<MATSIZE; col++)
            {
                Find_output2[row][col]=Find_ou
tput_DMA[index];

                index++;
            }
        }

        return 0;
}
int Find_ACP3()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_2_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)

```



```

        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
    // for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
    // {
    //     printf("Input %f \n ",DMA_input[i]);
    // }

    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);

    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    }
    XTime_GetTime(&time_ACP_end);
    printf("\n-----ACP FPGA EXECUTION TIME----
-----\n");

    float time_ACPFPGA = 0;
    time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
    for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
    {
        printf("Output :
%f\n",Find_output_DMA[i]);
    }
    index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {

```

```

Find_output3[row][col]=Find_output3[row][col]+Find_output2[row][col];
tput_DMA[index];
index++;
    }
}

return 0;
}

int Find_ACP4()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_3_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
    // for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
    // {
    //     printf("Input %f \n ",DMA_input[i]);
    // }
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
    (UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_DMA);
}

```

```

        status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
        }
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
        }
        XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
        for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
        {
            printf("Output :
%f\n",Find_output_DMA[i]);
        }
        index=0;
        for(int row=0; row<MATSIZE; row++)
        {
            for(int col=0; col<MATSIZE; col++)
            {
                Find_output4[row][col]=Find_ou
tput_DMA[index];

                index++;
            }
        }

        return 0;
    }
int Find_ACP5()
{
    float DMA_input[INP_SIZE*INP_SIZE*2];
    float Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer

```

```

XAxiDma AxiDMAacp; // DMA instance pointer
DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_4_DEVICE_ID);
status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
if(status != XST_SUCCESS)
{
    printf("ACP DMA Init Failed\t\n");
    return XST_FAILURE;
}
XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
//    for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
//    {
//        printf("Input %f \n ",DMA_input[i]);
//    }
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_D
MA);
    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    while(status!=0x00000002)

```

```

        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
        }
        XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
        for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
        {
            printf("Output  :
%f\n",Find_output_DMA[i]);
        }
        index=0;
        for(int row=0; row<MATSIZE; row++)
        {
            for(int col=0; col<MATSIZE; col++)
            {
                Find_output5[row][col]=Find_ou
tput_DMA[index];

                index++;
            }
        }

        return 0;
    }
int compare1()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output1[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}
int compare2()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)

```

```

        {
            if(Find_output2[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}
int compare3()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output3[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}
int compare4()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output4[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}
int compare5()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output5[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
}

```

```

    }
    return 1;
}
int main()
{
    init_platform();
    input();
    PS();
    Find_ACP1();
    Find_ACP2();
    Find_ACP3();
    Find_ACP4();
    Find_ACP5();
    int ans=compare1();
    int ans1=compare2();
    int ans2=compare3();
    int ans3=compare4();
    int ans4=compare5();
    if(ans==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all\n");
    }
    if(ans1==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all");
    }
    if(ans2==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all\n");
    }
    if(ans3==1)
    {
        printf("You are great\n");
    }
    else
    {

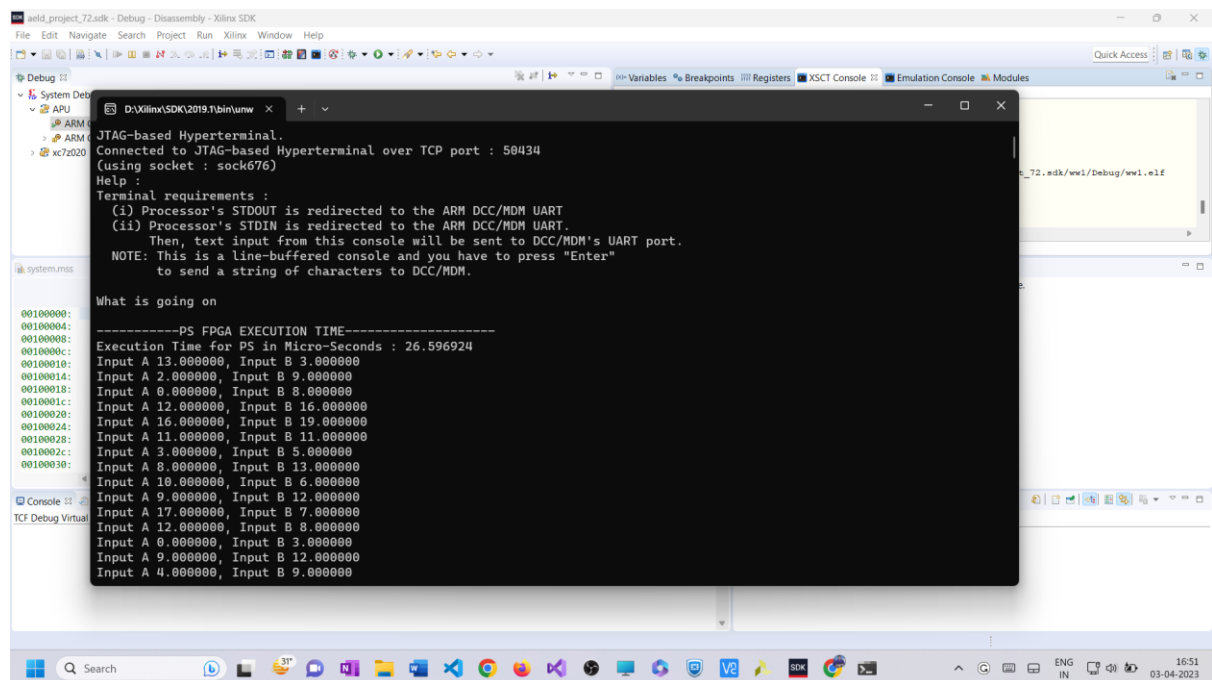
```

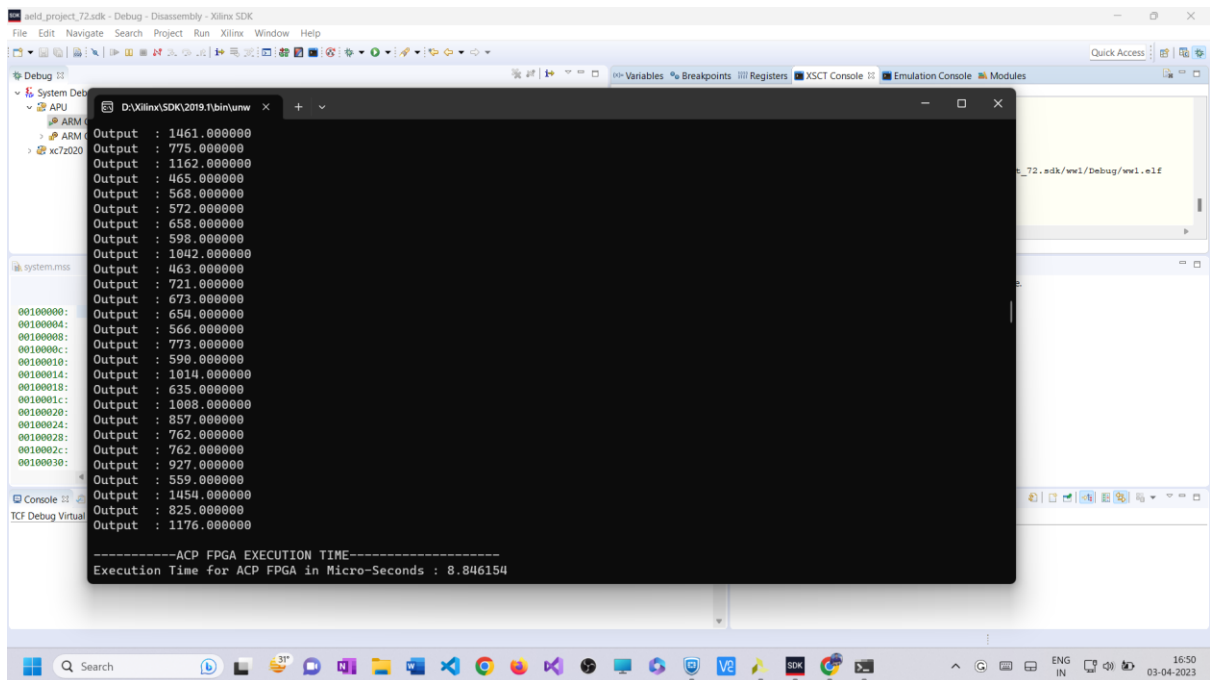
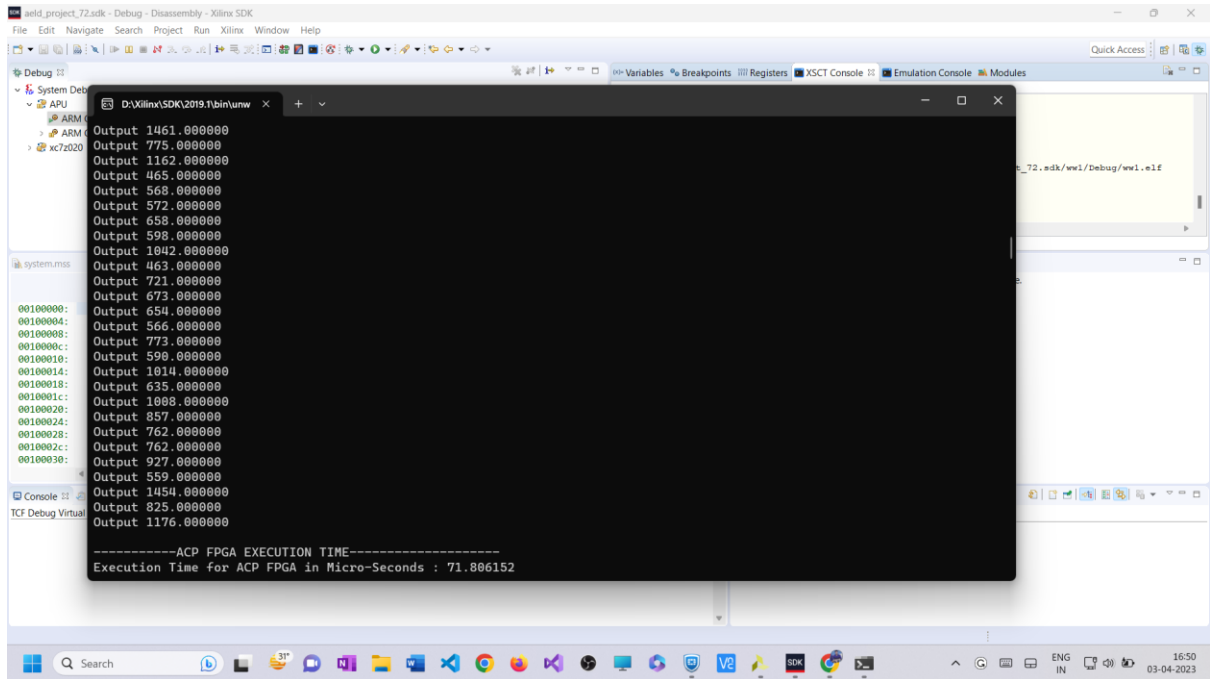
```

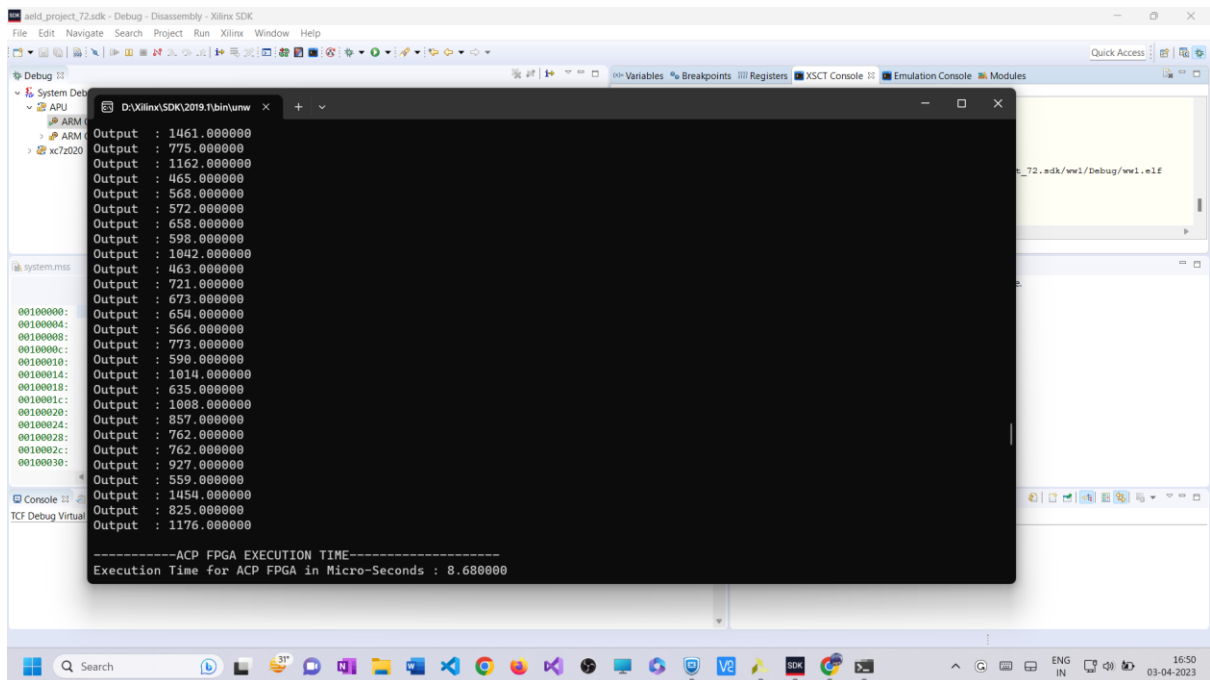
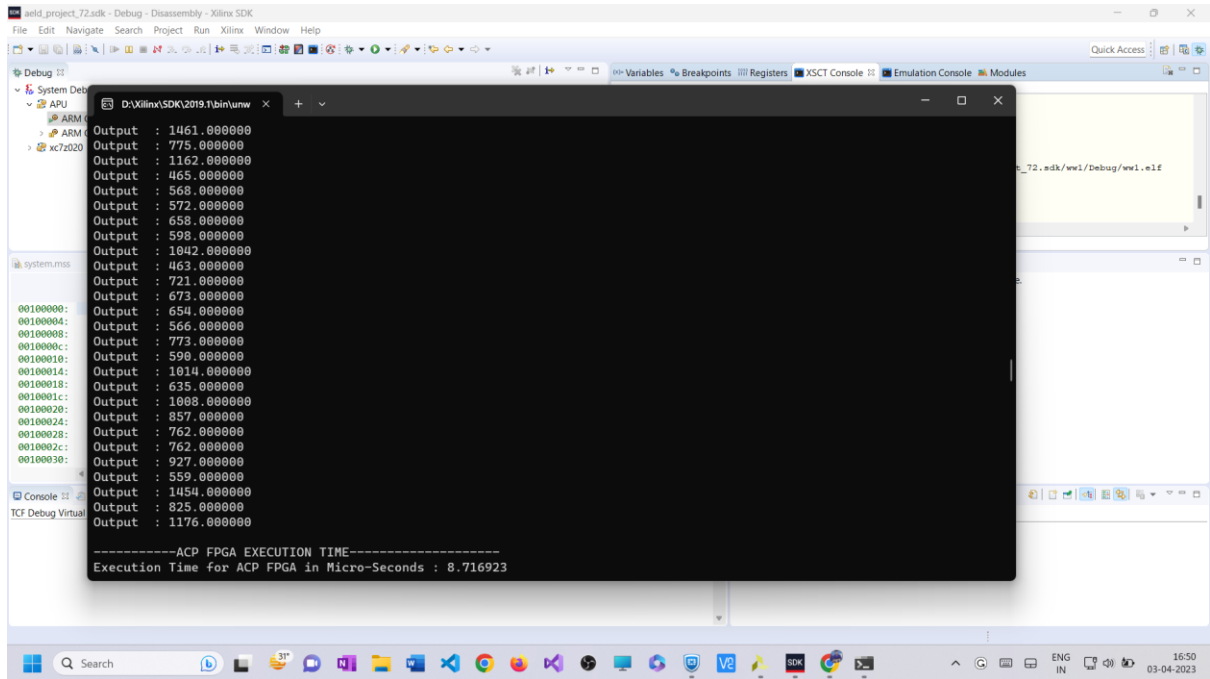
        printf("No good at all\n");
    }
    if(ans4==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all");
    }
    cleanup_platform();
    return 0;
}

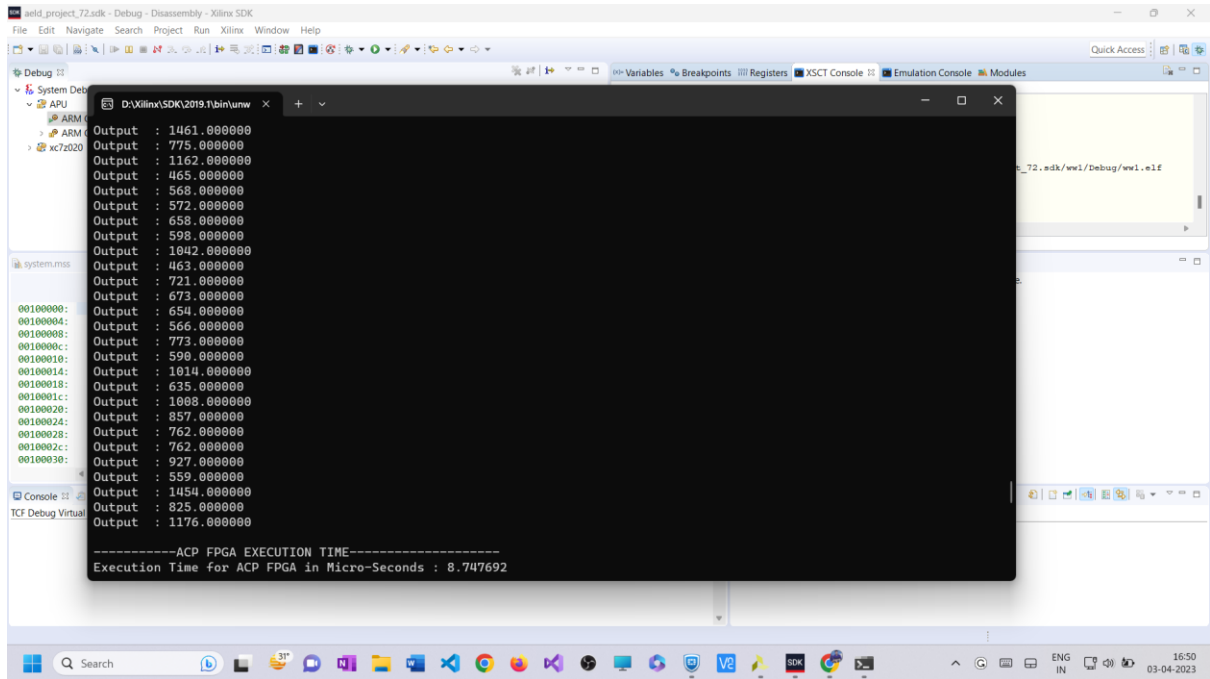
```

Jtagterminal:-

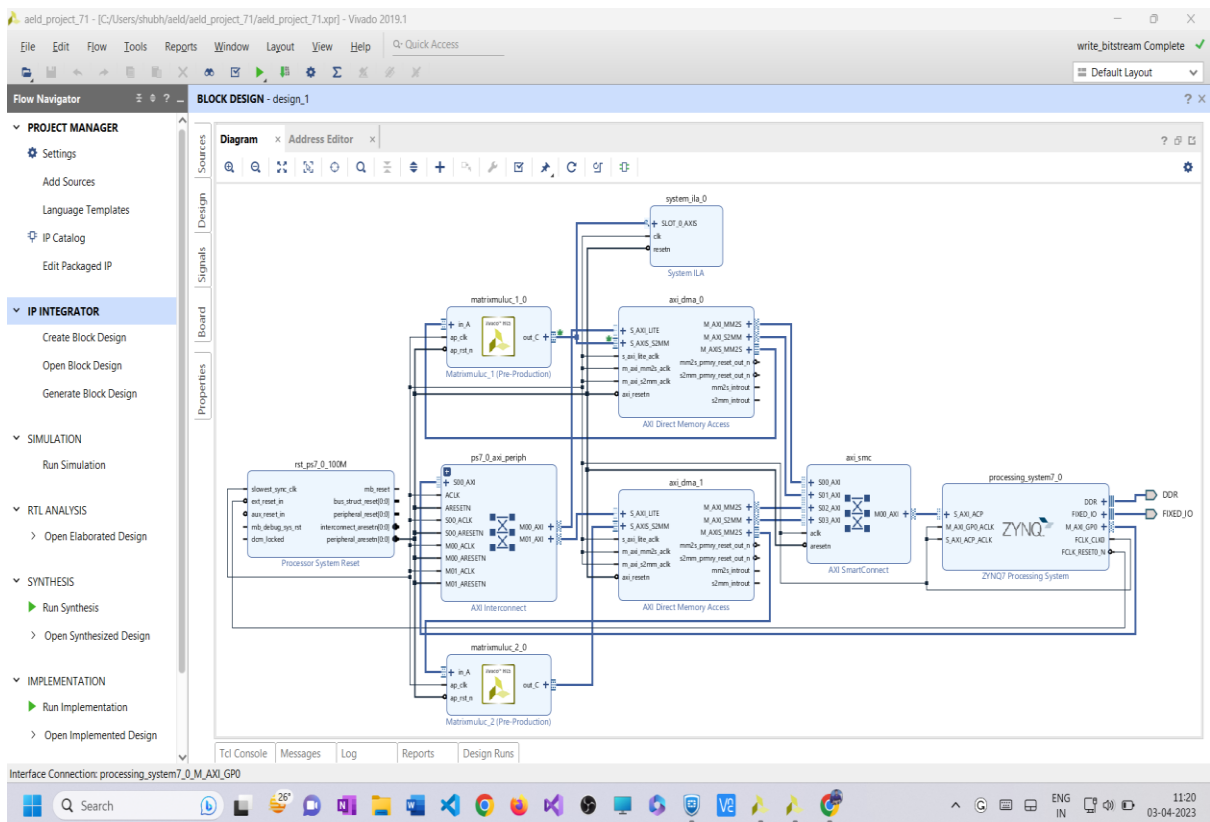








Block Diagram:-



Code:-

```
/******
*
*
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*****
/

/*
* helloworld.c: simple test application
*
* This application configures UART 16550 to baud rate 9600.
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
*
* -----
* | UART TYPE   BAUD RATE |
* -----
*/
```

```

*   uartns550    9600
*   uartlite     Configurable only in HW design
*   ps7_uart     115200 (configured by bootrom/bsp)
*/

#include <stdio.h>
#include <stdlib.h>
#include "xaxidma.h"
#include "xparameters.h"
#include "platform.h"
#include<xtime_l.h>
#include<complex.h>
#define INP_SIZE 32
#define MATSIZE 32
float complex Find_input_A[32][32];
float complex Find_input_B[32][32];
float complex Find_outputps[32][32];
float complex Find_output1[32][32];
float complex Find_output2[32][32];
void input()
{
    for (int i=0;i<INP_SIZE;i++)
    {
        for(int j=0; j<INP_SIZE; j++)
        {
            Find_input_A[i][j]= (rand()%20)+I*(rand()%20);
            Find_input_B[i][j]= (rand()%20)+I*(rand()%20);
        }
    }
}
void PS()
{
    float complex Find_outputps[INP_SIZE][INP_SIZE];
    XTime time_PS_start , time_PS_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_PS_start);
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            float complex res=0;
            for(int index=0; index<MATSIZE; index++)
            {
                res+=Find_input_A[i][index]*Find_input_B[index][j];
            }
            Find_outputps[i][j]=res;
        }
    }
}

```

```

XTime_GetTime(&time_PS_end);
for(int row=0; row<MATSIZE; row++)
{
    for( int col=0; col<MATSIZE; col++)
    {
        printf("Input A %lf %lf, Input B %lf
%lf\n",creal(Find_input_A[row][col]),cimag(Find_input_A[row][col]),creal(Find_
input_B[row][col]),cimag(Find_input_B[row][col]));
    }
}
for(int row=0; row<MATSIZE; row++)
{
    for(int col=0; col<MATSIZE; col++)
    {
        printf("Output %lf
%lf\n",creal(Find_outputps[row][col]),cimag(Find_outputps[row][col]));
    }
}
printf("\n-----PS FPGA EXECUTION TIME-----\n");
float time_PS = 0;
time_PS = (float)1.0 * (time_PS_end
- time_PS_start) / (COUNTS_PER_SECOND/1000000);
printf("Execution Time for PS in
Micro-Seconds : %f\n" , time_PS);
}
int Find_ACP1()
{
    printf("on first one\n");
    float complex DMA_input[INP_SIZE*INP_SIZE*2];
    float complex Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_0_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)

```

```

        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];
            index++;
        }
    }
    // for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
    // {
    //     printf("Input %f \n ",DMA_input[i]);
    // }

    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*2*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO_DMA);

    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*2*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    }
    XTime_GetTime(&time_ACP_end);
    printf("\n-----ACP FPGA EXECUTION TIME----
-----\n");

    float time_ACPFPGA = 0;
    time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
    // for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
    // {

```

```

//                                printf("Output  : %lf
%lf\n",creal(Find_output_DMA[i]),cimag(Find_output_DMA[i]));
//                                }
                                printf("H4\n");
                                index=0;
                                for(int row=0; row<MATSIZE; row++)
                                    {
                                        for(int col=0; col<MATSIZE; col++)
                                        {
                                            Find_output1[row][col]=Find_ou
tput_DMA[index];

                                            index++;
                                        }
                                    }

                                return 0;
}
int Find_ACP2()
{
    printf("on second one\n");
    float complex DMA_input[INP_SIZE*INP_SIZE*2];
    float complex Find_output_DMA[INP_SIZE*INP_SIZE];
    int status;
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_1_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }
    XTime time_ACP_start , time_ACP_end;
        XTime_SetTime(0);
        XTime_GetTime(&time_ACP_start);
    int index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_A[row][col];
            index++;
        }
    }
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            DMA_input[index]=Find_input_B[row][col];

```



```

        index++;
    }
}
//      for(int i=0; i<INP_SIZE*INP_SIZE*2; i++)
//      {
//          printf("Input %f \n ",DMA_input[i]);
//      }
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output_DMA,(sizeof(float)*2*INP_SIZE*INP_SIZE),XAXIDMA_DEVICE_TO
_DMA);
    status = XAxiDma_SimpleTransfer(&AxiDMAacp, (UINTPTR)DMA_input,
(sizeof(float)*2*INP_SIZE*INP_SIZE*2),XAXIDMA_DMA_TO_DEVICE);
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
    }
    status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

    while(status!=0x00000002)
    {
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
    }
    XTime_GetTime(&time_ACP_end);
    printf("\n-----ACP FPGA EXECUTION TIME----
-----\n");

    float time_ACPFPGA = 0;
    time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for ACP FPGA in
Micro-Seconds : %f\n" , time_ACPFPGA);
//      for(int i = 0 ; i<INP_SIZE*INP_SIZE; i++)
//      {
//          printf("Output : %lf
%lf\n",creal(Find_output_DMA[i]),cimag(Find_output_DMA[i]));
//      }
    index=0;
    for(int row=0; row<MATSIZE; row++)
    {
        for(int col=0; col<MATSIZE; col++)
        {
            Find_output2[row][col]=Find_ou
tput_DMA[index];

            index++;

```

```

    }
}

return 0;
}

int compare1()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output1[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}

int compare2()
{
    for(int i=0; i<MATSIZE; i++)
    {
        for(int j=0; j<MATSIZE; j++)
        {
            if(Find_output2[i][j]!=Find_outputps[i][j])
            {
                return 0;
            }
        }
    }
    return 1;
}

int main()
{
    init_platform();
    input();
    PS();
    Find_ACP1();
    Find_ACP2();
    int ans=compare1();
    int ans1=compare2();
    if(ans==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all\n");
    }
}

```

```

    }
    if(ans1==1)
    {
        printf("You are great\n");
    }
    else
    {
        printf("No good at all");
    }
    cleanup_platform();
    return 0;
}

```

Jtagterminal:-

