

Roll No – MT22154

The image shows the Vivado IDE interface for a project named 'aeld_project_32'. The main window displays a Block Design for 'design_1'. The design is composed of several interconnected components: a 'Processor System Reset' block, an 'AXI DMA' block, an 'AXI SMC' block, a 'Demo Find' block, and a 'ZYNQ Processing System' block. The 'ZYNQ Processing System' block is further detailed with various internal components like 'AXI Interconnect', 'AXI SmartConnect', and 'AXI Memory Access'. The 'Tcl Console' at the bottom shows a series of commands used to exclude certain components from the design, such as 'Excluding </processing_system7_0/S_AXI_ACP/ACP_IOP> from </axi_dma_0/Data_S2M0>' and 'Excluding </processing_system7_0/S_AXI_ACP/ACP_M_AXI_GDR> from </axi_dma_0/Data_S2M0>'. The 'Flow Navigator' on the left indicates the current stage is 'BLOCK DESIGN - design_1'. The 'Project Explorer' on the left shows the project hierarchy, including 'design_1', 'External Interface', 'Interface Connect', 'Nets', 'axi_dma_0 (AXI D', 'axi_smc (AXI Sme', 'demo_find_0 (De', 'processing_system', and 'ps7_0_axi_periph'. The 'System Net' at the bottom shows the system configuration, including 'processing_system7_0_FCLK_RESETO_N'.

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*****
/

/*
 * helloworld.c: simple test application
 *
 * This application configures UART 16550 to baud rate 9600.
 * PS7 UART (Zynq) is not initialized by this application, since
 * bootrom/bsp configures it to baud rate 115200
 *
 * -----
 * | UART TYPE   BAUD RATE |
 * -----
 * | uartns550   9600      |
 * | uartlite    Configurable only in HW design
 * | ps7_uart    115200 (configured by bootrom/bsp)
 */

#include <stdio.h>
#include <stdlib.h>
#include "xaxidma.h"
#include "xparameters.h"
#include "platform.h"
#include <xtime_l.h>
#define INP_SIZE 32
int Find_input[INP_SIZE],Find_output[INP_SIZE];
int val=4;
int find_outputps[INP_SIZE];
void input()
{

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        for(int i=0;i<INP_SIZE;i++)
        {
            Find_input[i]= (rand()%20);
        }
    }
    void PS()
    {
        XTime time_PS_start,time_PS_end;
        XTime_SetTime(0);
        XTime_GetTime(&time_PS_start);
        for(int i=0; i<INP_SIZE; i++)
        {
            if(Find_input[i]==val)
            {
                find_outputps[i]=1;
            }
            else
                find_outputps[i]=0;
        }
        XTime_GetTime(&time_PS_end);
        for(int i=0; i<INP_SIZE; i++)
        {
            printf("%d ",find_outputps[i]);
        }

        printf("\n-----PS EXECUTION TIME-----\n");

        float time_processor = 0;
        time_processor = (float)1.0 * (time_PS_end -
time_PS_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for PS in Micro-Seconds : %f\n"
, time_processor);
    }
    int Find_ACP()
    {
        int status;
        XAxiDma_Config *DMA_confptracp;
        XAxiDma AxiDMAacp;
        DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_0_DEVICE_ID);
        status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
        if(status != XST_SUCCESS)
        {
            printf("ACP DMA Init Failed\t\n");
            return XST_FAILURE;
        }

        XTime time_ACP_start , time_ACP_end;
        XTime_SetTime(0);
        XTime_GetTime(&time_ACP_start);

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        // Generate random numbers

        status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output, (sizeof(int)*INP_SIZE),XAXIDMA_DEVICE_TO_DMA);
        status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_input, (sizeof(int)*INP_SIZE),XAXIDMA_DMA_TO_DEVICE);
        // We have only configure the DMA to perform these two
transactions..DMA might not have started the transactions.

        // Xil_DCacheInvalidateRange((UINTPTR)FFT_output_PLACP,
(sizeof(float complex)*FFT_Size));
        //status = checkDMAIdle(XPAR_AXI_DMA_0_BASEADDR, 0x04);
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
        }
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
        }
        XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in Micro-Seconds :
%f\n" , time_ACPFPGA);
        int j;

        for (j = 0 ; j < 10 ; j++)
        {
            printf("Input : %d , Output : %d\n " ,(int)Find_input[j],
(int)Find_output[j]);
        }

        return 0;
}

int main()
{
    init_platform();

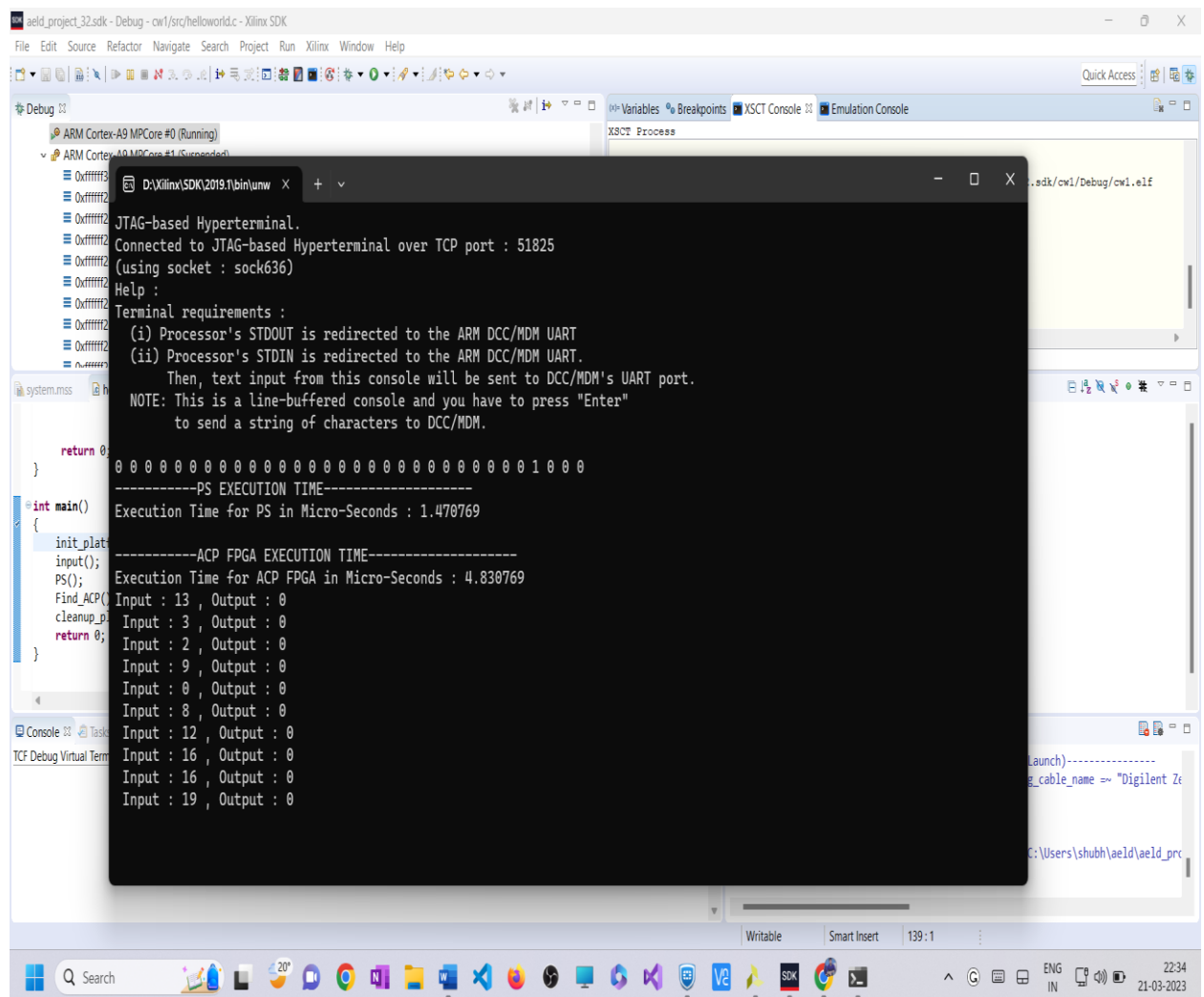
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input();
PS();
Find_ACP();
cleanup_platform();
return 0;
}

```

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[illegible]

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 * | UART TYPE   BAUD RATE |
 * -----
 *   uartns550   9600
 *   uartlite    Configurable only in HW design
 *   ps7_uart    115200 (configured by bootrom/bsp)
 */

#include <stdio.h>
#include <stdlib.h>
#include "xaxidma.h"
#include "xparameters.h"
#include "platform.h"
#include <xtime_l.h>
#define INP_SIZE 1024
int Find_input[INP_SIZE],Find_output[INP_SIZE];
int Find_outputps[INP_SIZE];
void input()
{
    for (int i=0;i<INP_SIZE;i++)
    {
        Find_input[i]= (rand()%20);
    }
}
void PS()

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{
    XTime time_PS_start,time_PS_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_PS_start);
    for(int i=0; i<INP_SIZE; i++)
    {
        Find_outputps[i]=Find_input[i]*Find_input[i];
    }
    XTime_GetTime(&time_PS_end);
    printf("\n-----PS EXECUTION TIME-----\n");

    float time_processor = 0;
    time_processor = (float)1.0 * (time_PS_end -
time_PS_start) / (COUNTS_PER_SECOND/1000000);
    printf("Execution Time for PS in Micro-Seconds :
%f\n" , time_processor);
}
int Find_ACP()
{
    int status;

    // ACP DMA Initialization
    XAxiDma_Config *DMA_confptracp; //DMA configuration pointer
    XAxiDma AxiDMAacp; // DMA instance pointer
    // Copy the DMA information (received from hardware in xparameters.h
file)
    DMA_confptracp = XAxiDma_LookupConfig(XPAR_AXI_DMA_0_DEVICE_ID);
    status = XAxiDma_CfgInitialize(&AxiDMAacp, DMA_confptracp);
    if(status != XST_SUCCESS)
    {
        printf("ACP DMA Init Failed\t\n");
        return XST_FAILURE;
    }

    XTime time_ACP_start , time_ACP_end;
    XTime_SetTime(0);
    XTime_GetTime(&time_ACP_start);
    // Generate random numbers

    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_output, (sizeof(int)*INP_SIZE),XAXIDMA_DEVICE_TO_DMA);
    status = XAxiDma_SimpleTransfer(&AxiDMAacp,
(UINTPTR)Find_input, (sizeof(int)*INP_SIZE),XAXIDMA_DMA_TO_DEVICE);
    // We have only configure the DMA to perform these two
transactions..DMA might not have started the transactions.

    // Xil_DCacheInvalidateRange((UINTPTR)FFT_output_PLACP,
(sizeof(float complex)*FFT_Size));
    //status = checkDMAIdle(XPAR_AXI_DMA_0_BASEADDR, 0x04);

```



```

        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x04) &
0x00000002;
        }
        status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;

        while(status!=0x00000002)
        {
            status = XAxiDma_ReadReg(XPAR_AXI_DMA_0_BASEADDR,0x34) &
0x00000002;
        }
        XTime_GetTime(&time_ACP_end);
        printf("\n-----ACP FPGA EXECUTION TIME-----
-----\n");

        float time_ACPFPGA = 0;
        time_ACPFPGA = (float)1.0 * (time_ACP_end -
time_ACP_start) / (COUNTS_PER_SECOND/1000000);
        printf("Execution Time for ACP FPGA in Micro-
Seconds : %f\n" , time_ACPFPGA);
        int j;

        for (j = 0 ; j < 10 ; j++)
        {
            printf("Input : %d , Output : %d\n " ,(int)Find_input[j],
(int)Find_output[j]);

            }

        return 0;
}

int main()
{
    init_platform();
    input();
    PS();
    Find_ACP();
    cleanup_platform();
    return 0;
}

```

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