Name – Aryan Gupta

Roll No -MT22154

Assignment -6 VDF

Submitted to the Dr.Sneh Saurabh

1. Show screenshot or snippet of log file to prove that you have indeed run the tool [If this is not given then your assignment will not be evaluated].

```
aryan22154@edaserver3:~/assi_6$ atalanta
Invalid command line options.
To see on-line manual, use the following commands:
        For the user's guide, type "atalanta -h g"
        For the netlist format, type "atalanta -h n"
        For the test file format, type "atalanta -h t"
        For the fault list file format, type "atalanta -h f"
        For the entire manual, type "atalanta -h a"
aryan22154@edaserver3:~/assi_6$
```

2. Run the tool and find the test patterns for the single stuck at faults in the circuit shown in Fig. 1. Report the output in the file. Make the following table:

The column “Fault Site and fault type (SA0 or SA1)” should contain all possible single stuck-at fault in the circuit. No need to show the manual computation. Just write the answers. [1+4Marks]

```
aryan22154@edaserver3:~/assi_6$ atalanta -A -l -u -v c171.bench|& tee -a log.txt
before
after
end initialazition
iLastUndetectedFault=11
iLastUndetectedFault=10
iLastUndetectedFault=9
iLastUndetectedFault=8
iLastUndetectedFault=7
iLastUndetectedFault=6
iLastUndetectedFault=5
iLastUndetectedFault=4
iLastUndetectedFault=3
iLastUndetectedFault=2
iLastUndetectedFault=1
iLastUndetectedFault=0
        ********************************************************
        *                                                      *
        *          Welcome to atalanta (version 2.0)           *
        *                                                      *
        *               Dong S. Ha (ha@vt.edu)                 *
        *            Web: http://www.ee.vt.edu/ha              *
        *  Virginia Polytechnic Institute & State University   *
        *                                                      *
        ********************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                      : c171.bench
   Number of primary inputs                 : 4
   Number of primary outputs                : 1
   Number of gates                          : 6
   Level of the circuit                     : 5

2. ATPG parameters
   Test pattern generation Mode             : DTPG + TC
   Backtrack limit                          : 10
   Initial random number generator seed     : 1680359678
```

```
        ************************************************************
        *                                                          *
        *          Welcome to atalanta (version 2.0)               *
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        *               Dong S. Ha (ha@vt.edu)                     *
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        *                                                          *
        ************************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                        : c171.bench
   Number of primary inputs                   : 4
   Number of primary outputs                  : 1
   Number of gates                            : 6
   Level of the circuit                       : 5

2. ATPG parameters
   Test pattern generation Mode               : DTPG + TC
   Backtrack limit                            : 10
   Initial random number generator seed       : 1680359678
   Test pattern compaction Mode               : NONE

3. Test pattern generation results
   Number of test patterns                    : 18
   Fault coverage                             : 91.667 %
   Number of collapsed faults                 : 12
   Number of identified redundant faults      : 1
   Number of aborted faults                   : 0
   Total number of backtrackings              : 12

4. Memory used                                : 0.000 MB

5. CPU time
   Initialization                             : 0.000 Secs
   Fault simulation                           : 0.000 Secs
   FAN                                        : 0.000 Secs
   Total                                      : 0.000 Secs
aryan22154@edaserver3:~/assi_6$
```

c171.test

File Edit View

```
* Name of circuit:  c171.bench
* Primary inputs :
  A B C D

* Primary outputs:
  Z

* Test patterns and fault free responses:

C /1
       1: 1x00 0
C /0
       1: 1x10 1
w1 /1
       1: 0010 0
C->w2 /1
       1: 1x0x 0
       2: 010x 0
w3 /0
       1: xx0x 0
       2: 0010 0
D /1
       1: 1x10 1
C->w4 /1
Z /0
       1: 1x10 1
       2: 0110 1
A /0
       1: 1010 1
B /0
       1: 0110 1
w4 /0
       1: 1x11 0
       2: 0111 0
Z /1
       1: xx11 0
       2: xx01 0
       3: xx00 0
       4: 0010 0
```

c171.ufaults

File Edit View

```
C->w4 /1
```

| Fault Sites and Type | Test Pattern | Test Pattern(Manual) |
|---|---|---|
| A/0 | 1010 | 1010 |
| B/0 | 0110 | 0110 |
| C/0 | 1x10 | 1x10 |
| C/1 | 1x00 | 1x00 |
| D/1 | 1x10 | 1x10 |
| W1/1 | 0010 | 0010 |
| W3/0 | xx0x 0010 | xx0x 0010 |
| W4/0 | 1x11 0111 | 1x11 0111 |
| Z/1 | xx11 xx01 xx00 0010 | xx11 xx01 xx00 0010 |
| C-> w2/1 | 1x0x 010x | 1x0x 010x |
| C-> w4/0 | 1x11 0111 | 1x11 0111 |
| C-> w4/1 | Redundant | Redundant |

X refers to the I don't care (can be 0 or 1).

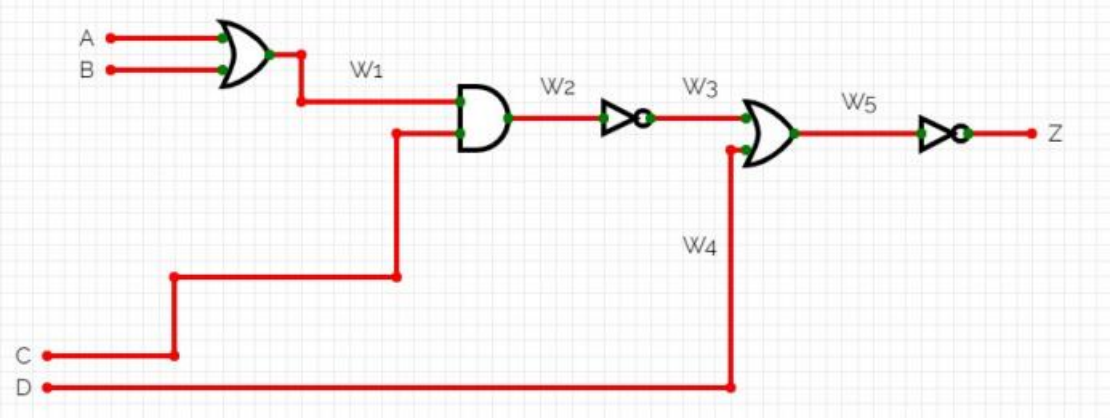
The redundant fault occurs in the AND Gate.(which of the SA1 type).

3. Modify the circuit to remove redundant fault reported by the ATPG tool preserving the Boolean function implemented by the circuit. Report the modified netlist in the "bench" format and schematic (you can draw by hand and paste the photograph). Run the ATPG tool. again, on the modified bench file. Report the output of the ATPG tool. Make the above table. again, for the modified circuit. No need to show the manual computation. Just write the answers. [1+1+1+2 Marks]

As there is only one redundant fault which occurs in the C-> w4/1. In order to reduce it we can do the is that we can remove the AND Gate that is connected.

As the C is stuck at the 1, so what ever be the value of D is, it is going to be propagated.

So the Boolean function is also be maintained.




Updated Netlist

```
aryan22154@edaserver3:~/assi_6$ atalanta -A -l -u -v c1.bench|& tee -a log.txt
before
after
end initialazition
iLastUndetectedFault=7
iLastUndetectedFault=6
iLastUndetectedFault=5
iLastUndetectedFault=4
iLastUndetectedFault=3
iLastUndetectedFault=2
iLastUndetectedFault=1
iLastUndetectedFault=0
        ************************************************************
        *                                                          *
        *          Welcome to atalanta (version 2.0)               *
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        *                                                          *
        ************************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                      : c1.bench
   Number of primary inputs                 : 4
   Number of primary outputs                : 1
   Number of gates                          : 5
   Level of the circuit                     : 5

2. ATPG parameters
   Test pattern generation Mode             : DTPG + TC
   Backtrack limit                          : 10
   Initial random number generator seed     : 1680361158
   Test pattern compaction Mode             : NONE

3. Test pattern generation results
```

```
3. Test pattern generation results
   Number of test patterns                    : 12
   Fault coverage                             : 100.000 %
   Number of collapsed faults                 : 8
   Number of identified redundant faults      : 0
   Number of aborted faults                   : 0
   Total number of backtrackings              : 8

4. Memory used                                : 0.000 MB

5. CPU time
   Initialization                             : 0.000 Secs
   Fault simulation                           : 0.000 Secs
   FAN                                        : 0.000 Secs
   Total                                      : 0.000 Secs
aryan22154@edaserver3:~/assi_6$
```

* log.txt

```
before
after
end initialazition
iLastUndetectedFault=7
iLastUndetectedFault=6
iLastUndetectedFault=5
iLastUndetectedFault=4
iLastUndetectedFault=3
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******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
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   Level of the circuit                       : 5

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   Test pattern generation Mode               : DTPG + TC
   Backtrack limit                            : 10
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   Test pattern compaction Mode               : NONE

3. Test pattern generation results
   Number of test patterns                    : 12
   Fault coverage                             : 100.000 %
   Number of collapsed faults                 : 8
   Number of identified redundant faults      : 0
   Number of aborted faults                   : 0
   Total number of backtrackings              : 8

4. Memory used                                : 0.000 MB

5. CPU time
   Initialization                             : 0.000 Secs
   Fault simulation                           : 0.000 Secs
   FAN                                        : 0.000 Secs
   Total                                      : 0.000 Secs

```

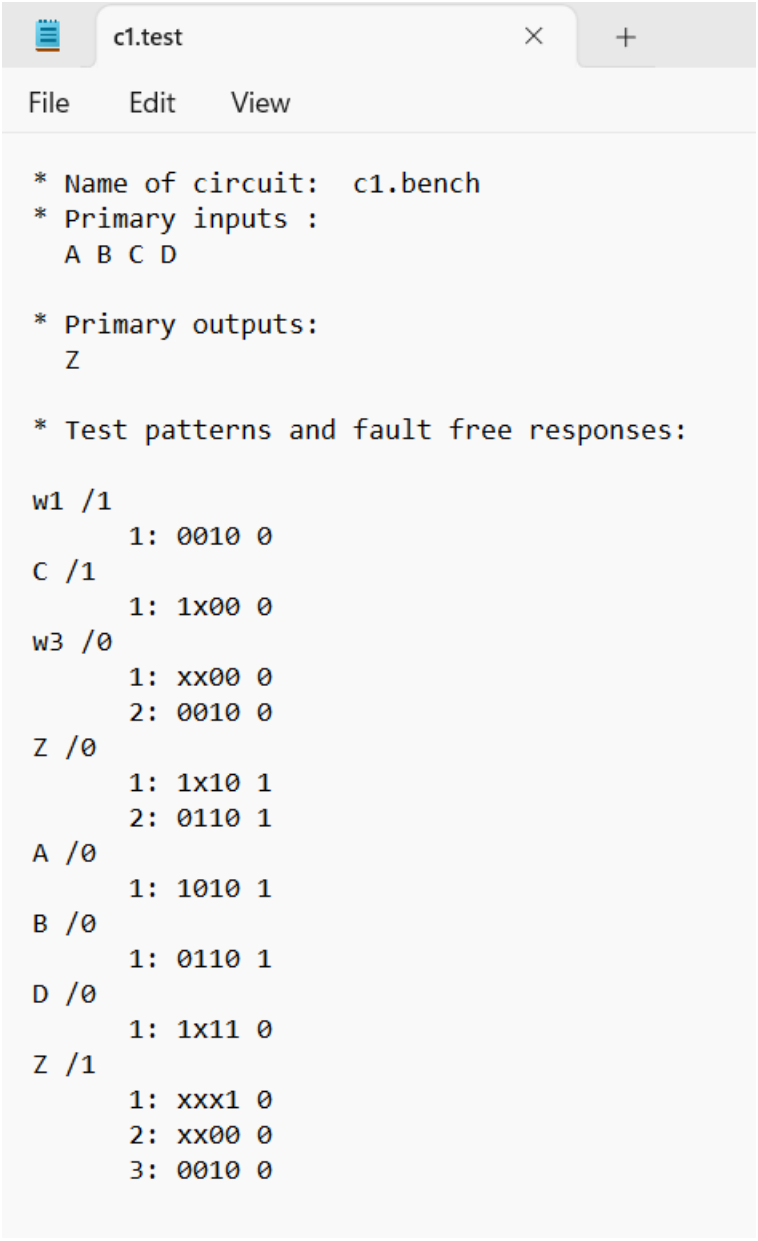


| Fault Sites and Type | Test Pattern | Test Pattern (Manual) |
|---|---|---|
| A/0 | 1010 | 1010 |
| B/0 | 0110 | 0110 |
| C/1 | 1x00 | 1x00 |
| D/0 | 1x11 | 1x11 |
| W1/1 | 0010 | 0010 |
| W3/0 | xx00  0010 | xx00  0010 |
| Z/0 | 1x10  0110 | 1x10  0110 |
| Z/1 | xxx1  xx00  0010 | xxx1  xx00  0010 |