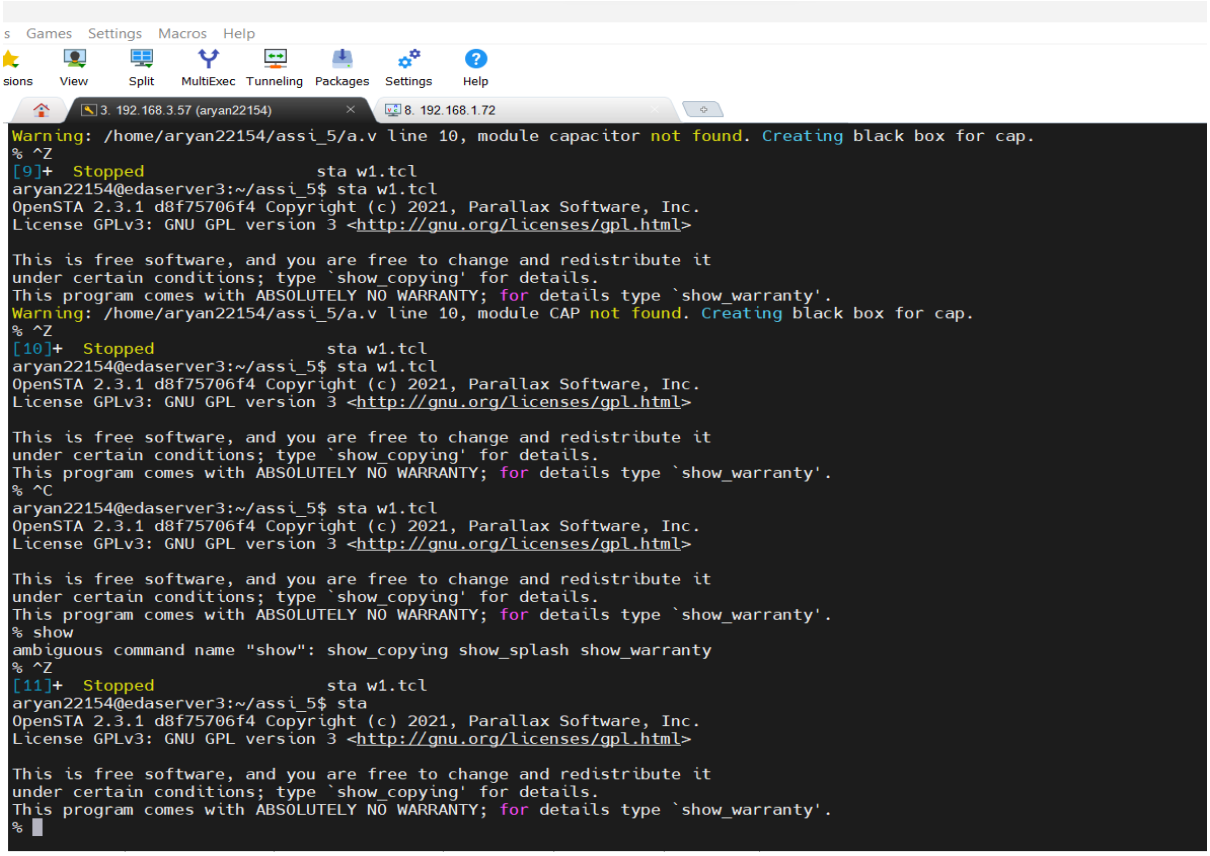
Name: - Aryan Gupta Roll No -MT22154

Assignment -5 VDF

Submitted to the: - Dr. Sneh Saurabh

Q1)-Show a screenshot or snippet of the log file to prove that you have indeed run the tool [If this is not given, then your assignment will not be evaluated].



Q2) –Write a Verilog netlist for the circuit shown above. Use instances of the minimum-sized (1X) inverter available in the library. [1 Marks]

```
module inv_c(IN,OUT);
input IN;
output OUT;
wire n1,n2,n3,n4,as,bs;
INVX1 I1(.A(IN),.Y(n1));
INVX1 I2(.A(n1),.Y(n2));
INVX1 I3(.A(n2),.Y(n3));
INVX1 I4(.A(n3),.Y(n4));
INVX1 I5(.A(n4),.Y(OUT));
// CAP cap(.OUT(out));
endmodule
```

Q3) - Specify the following constraints: input slew at port IN is 100 ps, and the output load at port OUT is one pF. Measure the delay between IN and OUT using the STA tool. Report the total delay and its value for each instance [2 Marks].

w.sdc

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```
create_clock -name CLK -period 5 -waveform {0 3}
set_input_delay 0 -clock [get_clocks "CLK"] [get_ports "IN"]
set_output_delay 0 -clock [get_clocks "CLK"] [get_ports "OUT"]
set_input_transition 0.1 [get_ports "IN"]
set_load 1 [get_ports "OUT"]
```

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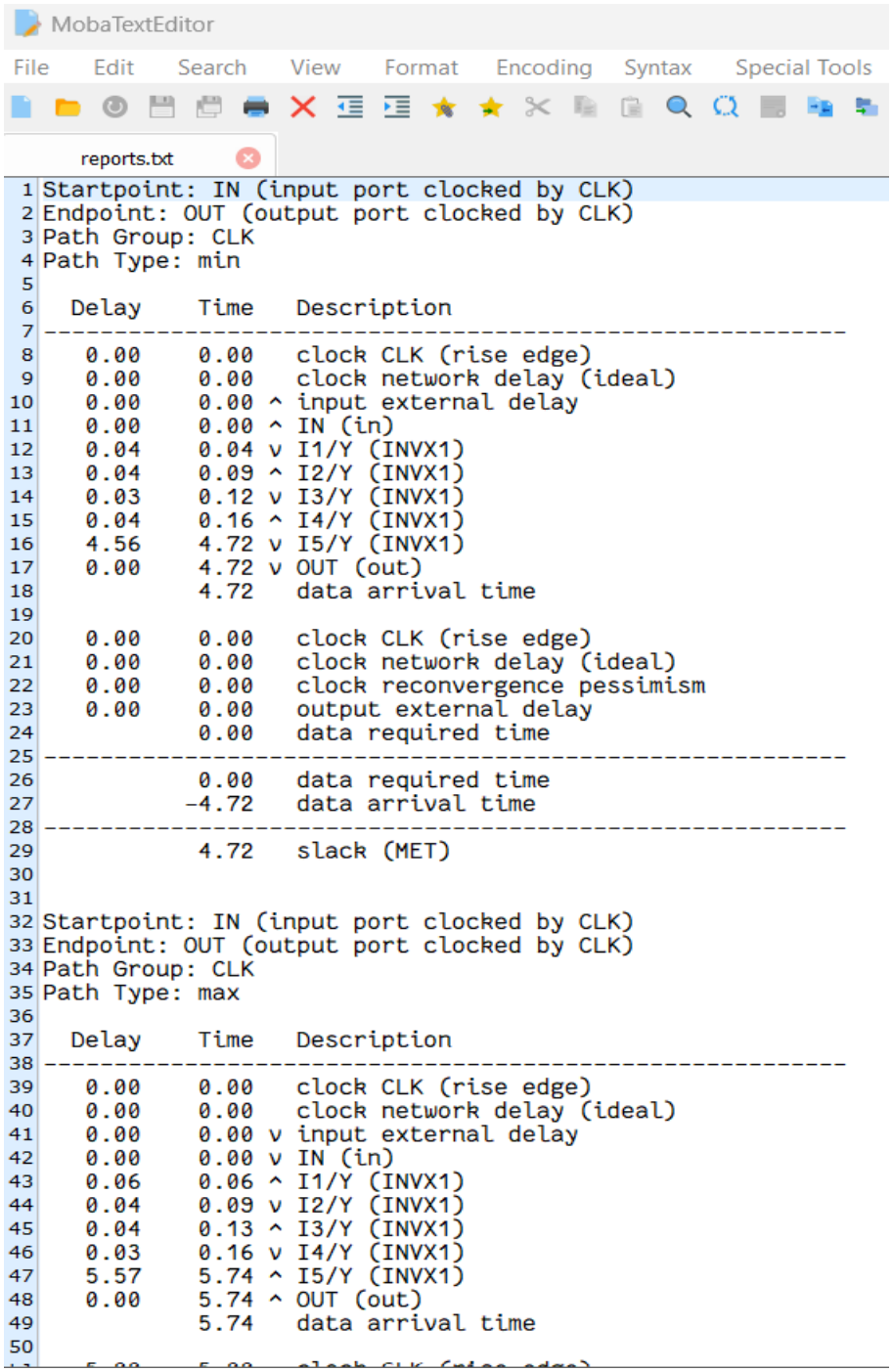
```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.04    0.04 v I1/Y (INVX1)
   0.04    0.09 ^ I2/Y (INVX1)
   0.03    0.12 v I3/Y (INVX1)
   0.04    0.16 ^ I4/Y (INVX1)
   4.56    4.72 v I5/Y (INVX1)
   0.00    4.72 v OUT (out)
           4.72   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.72   data arrival time
---------------------------------------------------------
           4.72   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.06    0.06 ^ I1/Y (INVX1)
   0.04    0.09 v I2/Y (INVX1)
   0.04    0.13 ^ I3/Y (INVX1)
   0.03    0.16 v I4/Y (INVX1)
   5.57    5.74 ^ I5/Y (INVX1)
   0.00    5.74 ^ OUT (out)
           5.74   data arrival time
```

The total delay in the above circuit is 4.72 (min) and 5.74 (max).

Q4)- Besides the inverter of size 1X, select three bigger inverters (higher drive strengths) from the

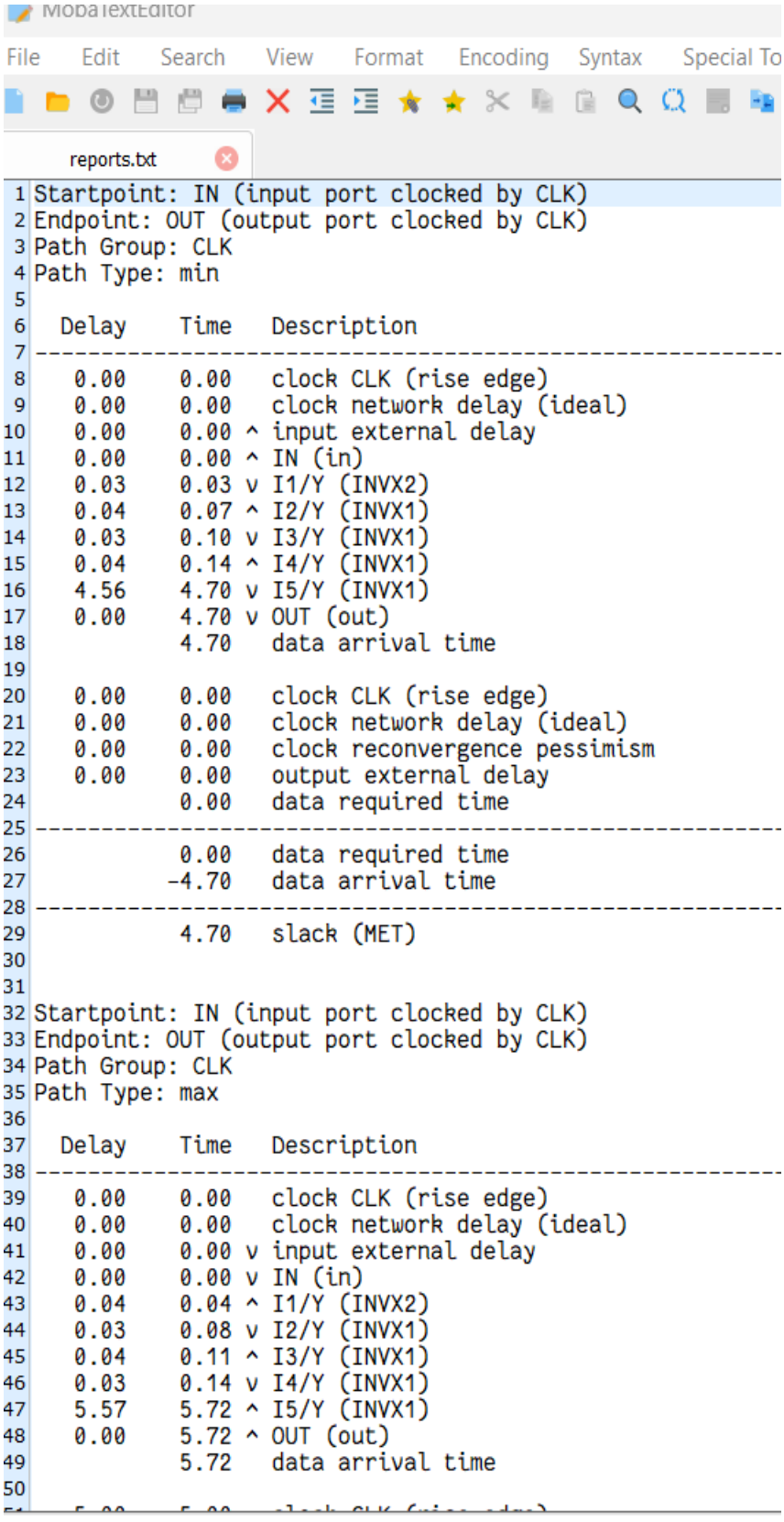
library for these experiments. Manually change instance A with these cells one by one. Observe the change in the delay of each instance of the circuit and the total path delay [total path delay means to delay from the input port to the output port]. Tabulate the information. Comment on the result. [4+1 Marks]

CASE -1 All are 1X size.



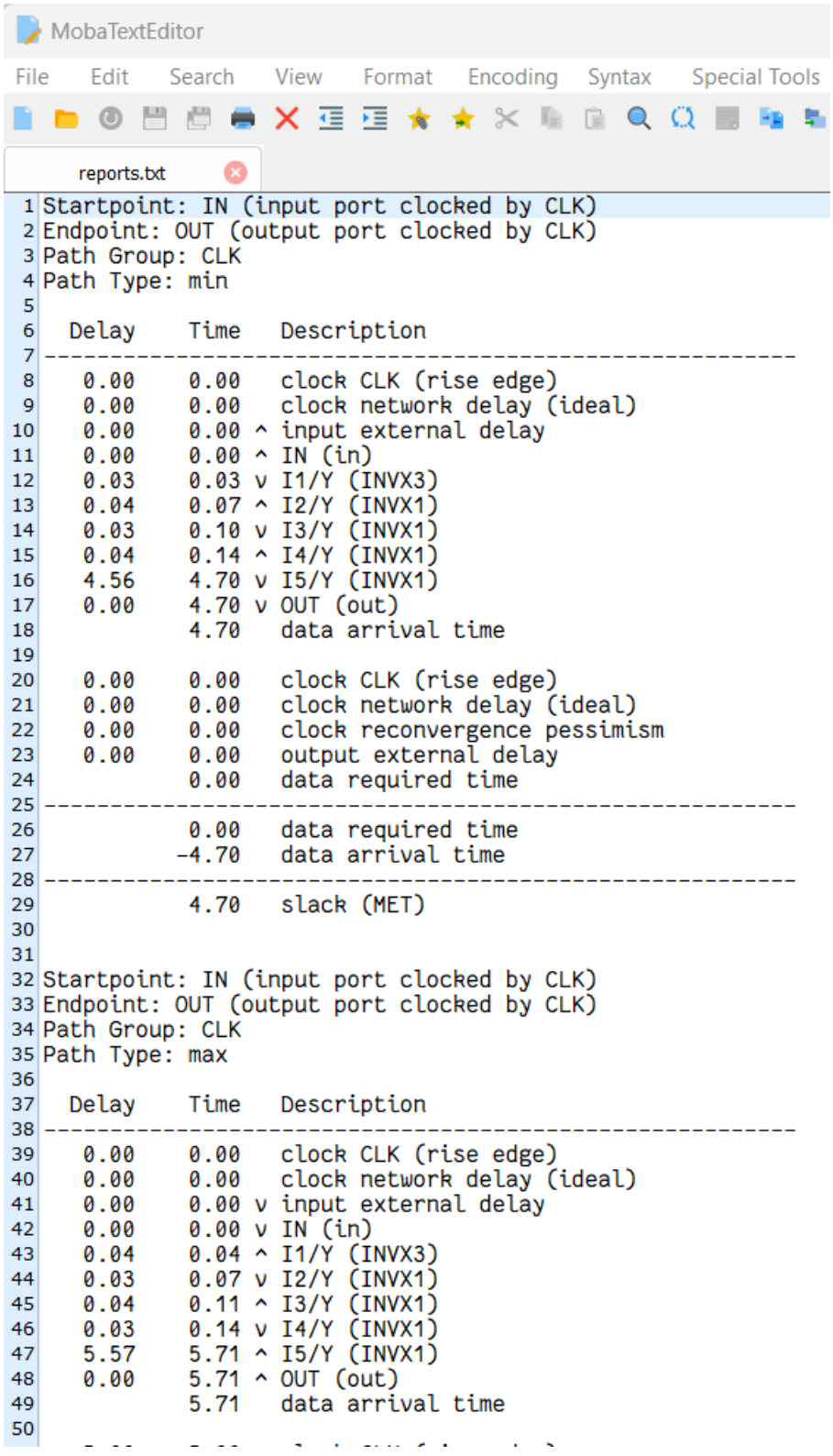

```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.04    0.04 v I1/Y (INVX1)
   0.04    0.09 ^ I2/Y (INVX1)
   0.03    0.12 v I3/Y (INVX1)
   0.04    0.16 ^ I4/Y (INVX1)
   4.56    4.72 v I5/Y (INVX1)
   0.00    4.72 v OUT (out)
           4.72   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.72   data arrival time
---------------------------------------------------------
           4.72   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.06    0.06 ^ I1/Y (INVX1)
   0.04    0.09 v I2/Y (INVX1)
   0.04    0.13 ^ I3/Y (INVX1)
   0.03    0.16 v I4/Y (INVX1)
   5.57    5.74 ^ I5/Y (INVX1)
   0.00    5.74 ^ OUT (out)
           5.74   data arrival time
```

CASE 2:- I1 of 2X size , reset are 1X




```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX2)
   0.04    0.07 ^ I2/Y (INVX1)
   0.03    0.10 v I3/Y (INVX1)
   0.04    0.14 ^ I4/Y (INVX1)
   4.56    4.70 v I5/Y (INVX1)
   0.00    4.70 v OUT (out)
           4.70   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.70   data arrival time
---------------------------------------------------------
           4.70   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX2)
   0.03    0.08 v I2/Y (INVX1)
   0.04    0.11 ^ I3/Y (INVX1)
   0.03    0.14 v I4/Y (INVX1)
   5.57    5.72 ^ I5/Y (INVX1)
   0.00    5.72 ^ OUT (out)
           5.72   data arrival time
```

Case 3:- I1 3X size and Rest are of 1X




```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX3)
   0.04    0.07 ^ I2/Y (INVX1)
   0.03    0.10 v I3/Y (INVX1)
   0.04    0.14 ^ I4/Y (INVX1)
   4.56    4.70 v I5/Y (INVX1)
   0.00    4.70 v OUT (out)
           4.70   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.70   data arrival time
---------------------------------------------------------
           4.70   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX3)
   0.03    0.07 v I2/Y (INVX1)
   0.04    0.11 ^ I3/Y (INVX1)
   0.03    0.14 v I4/Y (INVX1)
   5.57    5.71 ^ I5/Y (INVX1)
   0.00    5.71 ^ OUT (out)
           5.71   data arrival time
```

Case 4:- I1 of 4X and rest of 1X.

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```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.04    0.06 ^ I2/Y (INVX1)
   0.03    0.10 v I3/Y (INVX1)
   0.04    0.13 ^ I4/Y (INVX1)
   4.56    4.69 v I5/Y (INVX1)
   0.00    4.69 v OUT (out)
           4.69   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.69   data arrival time
---------------------------------------------------------
           4.69   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX1)
   0.04    0.10 ^ I3/Y (INVX1)
   0.03    0.14 v I4/Y (INVX1)
   5.57    5.71 ^ I5/Y (INVX1)
   0.00    5.71 ^ OUT (out)
           5.71   data arrival time

```

Inverter type	I1/1X	I1/2X	I1/3X	I1/4X
Delay	0.04	0.03	0.03	0.03
Total Delay (Min)	4.72	4.70	4.70	4.69
Total Delay (Max)	5.74	5.72	5.71	5.71

For the Table, We can observe that as we increase the size and driving strength of the inverter, the delay through the inverter also getting decreases.

As we also know, high strength lends to high leakages and high speed.

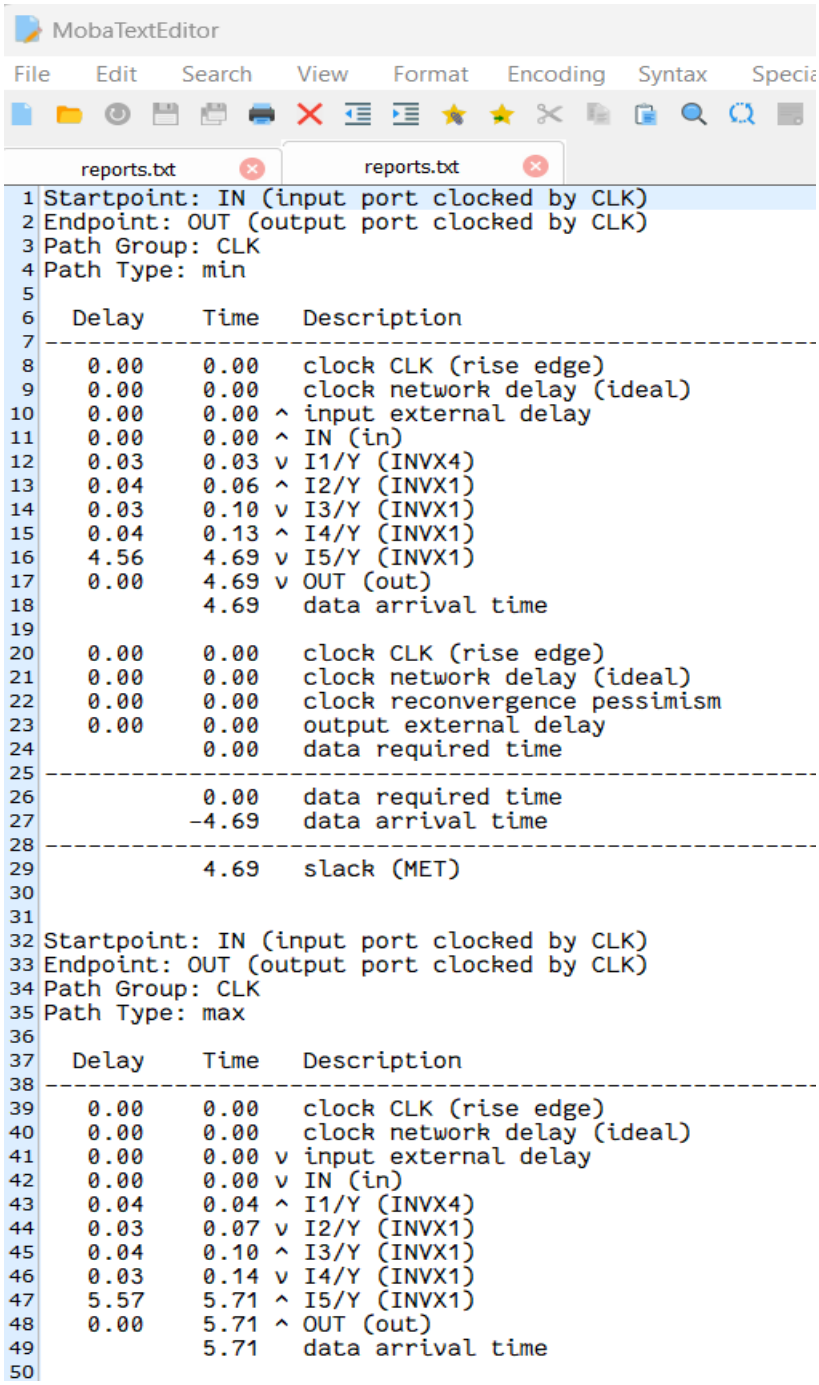
X1 means only one transistor(including pmos and a nmos) in the cells' drive stage.

X2 means two transistors in parallel in the cells's drive stage.

x4 means four transistors in parallel in cells' drive stage.

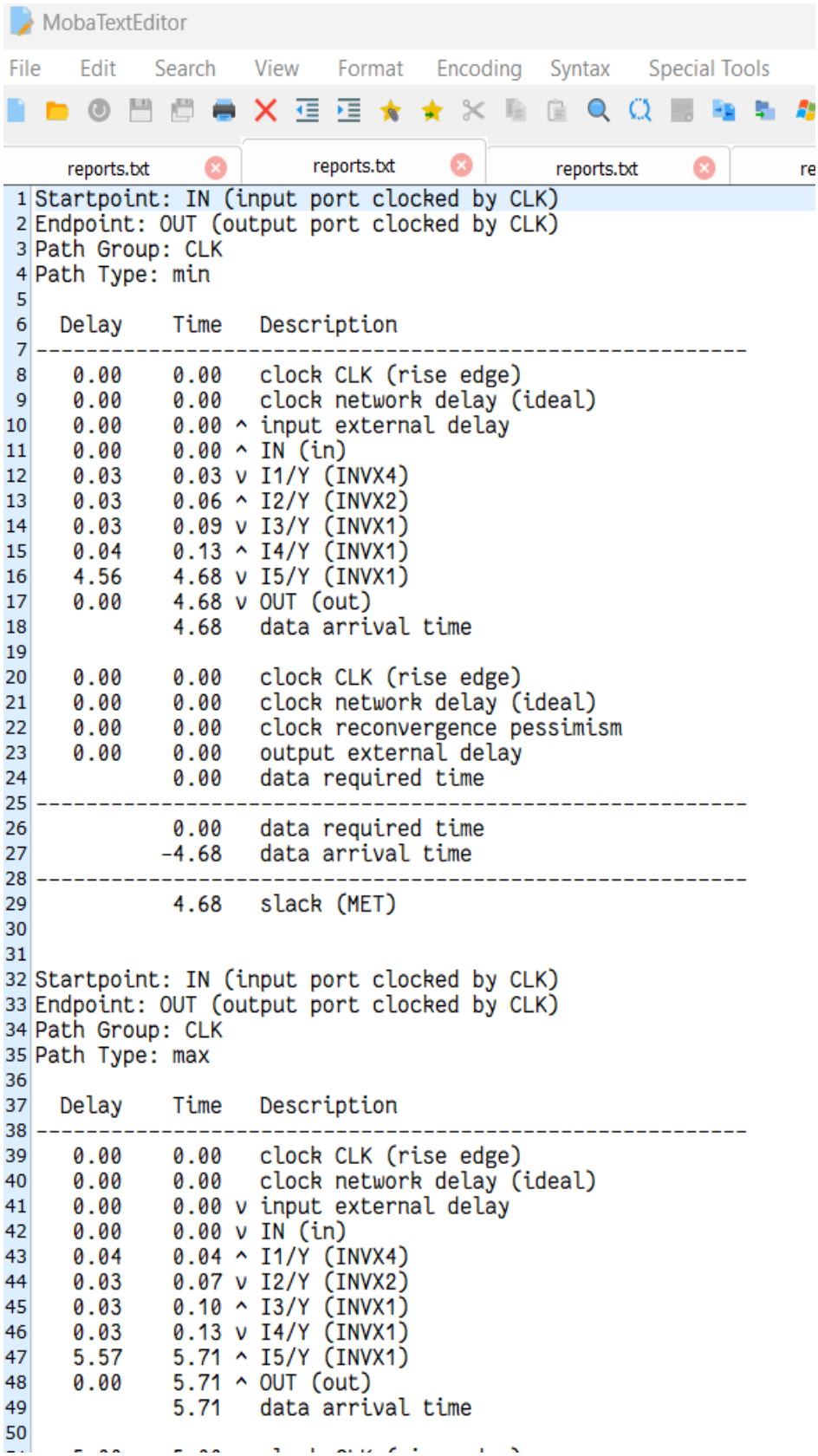
Q5)-For instance, A, fix the cell that produced the smallest total path delay in the above experiment. Next, repeat the above process for instance B and find the cell (among the cells considered in the previous experiment) that minimizes the total path delay. Tabulate the delay of each instance and the total path delay. Now, fix instance B to the cell that minimizes the total path delay. Repeat the same for instances C, D, and E in succession. [2+2+2+2 Marks]

Ans) - For the I1, the minimum path delay is set when it is X4.



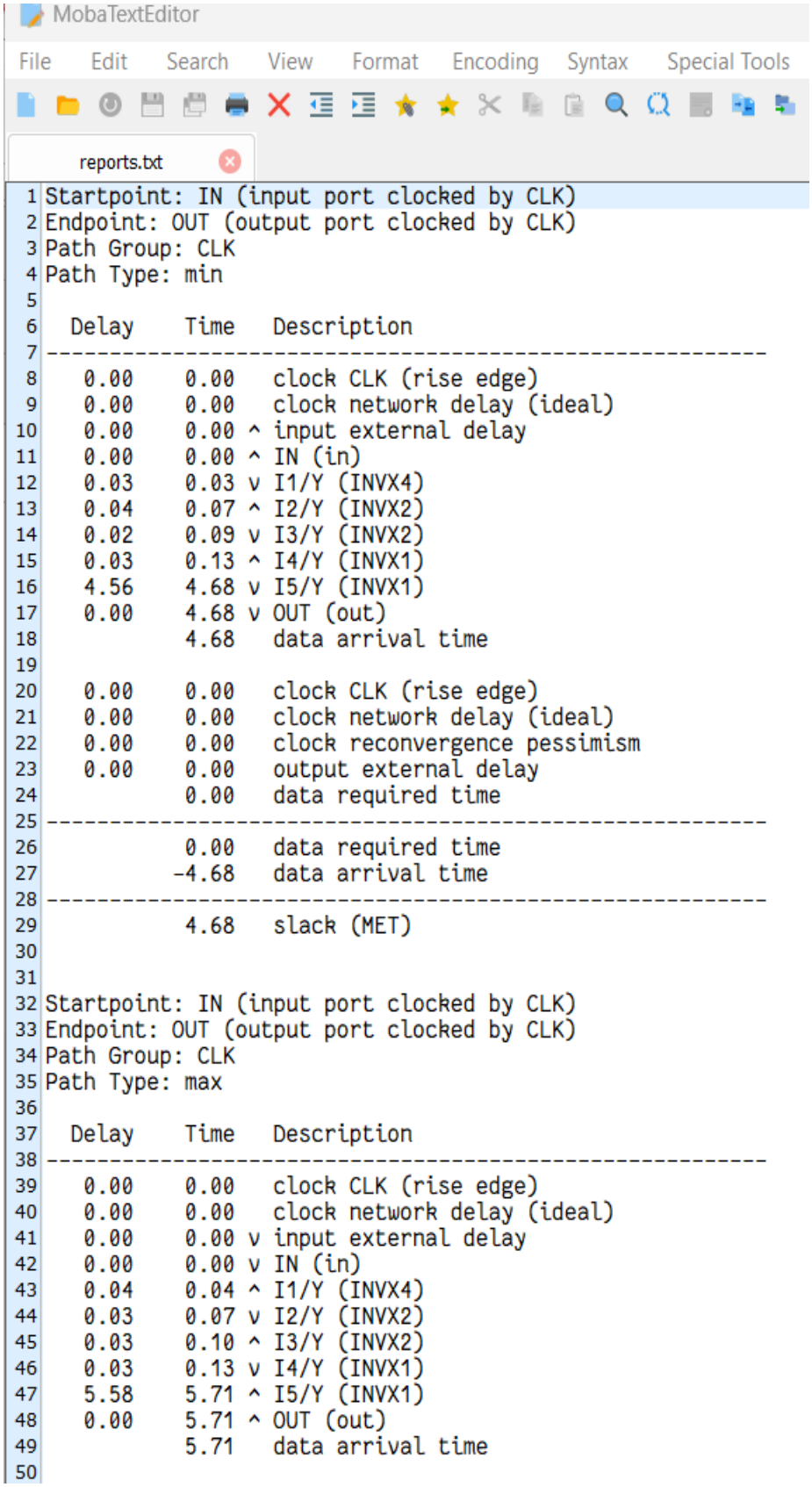

```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.04    0.06 ^ I2/Y (INVX1)
   0.03    0.10 v I3/Y (INVX1)
   0.04    0.13 ^ I4/Y (INVX1)
   4.56    4.69 v I5/Y (INVX1)
   0.00    4.69 v OUT (out)
           4.69   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.69   data arrival time
---------------------------------------------------------
           4.69   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX1)
   0.04    0.10 ^ I3/Y (INVX1)
   0.03    0.14 v I4/Y (INVX1)
   5.57    5.71 ^ I5/Y (INVX1)
   0.00    5.71 ^ OUT (out)
           5.71   data arrival time

```

Now for the I2,



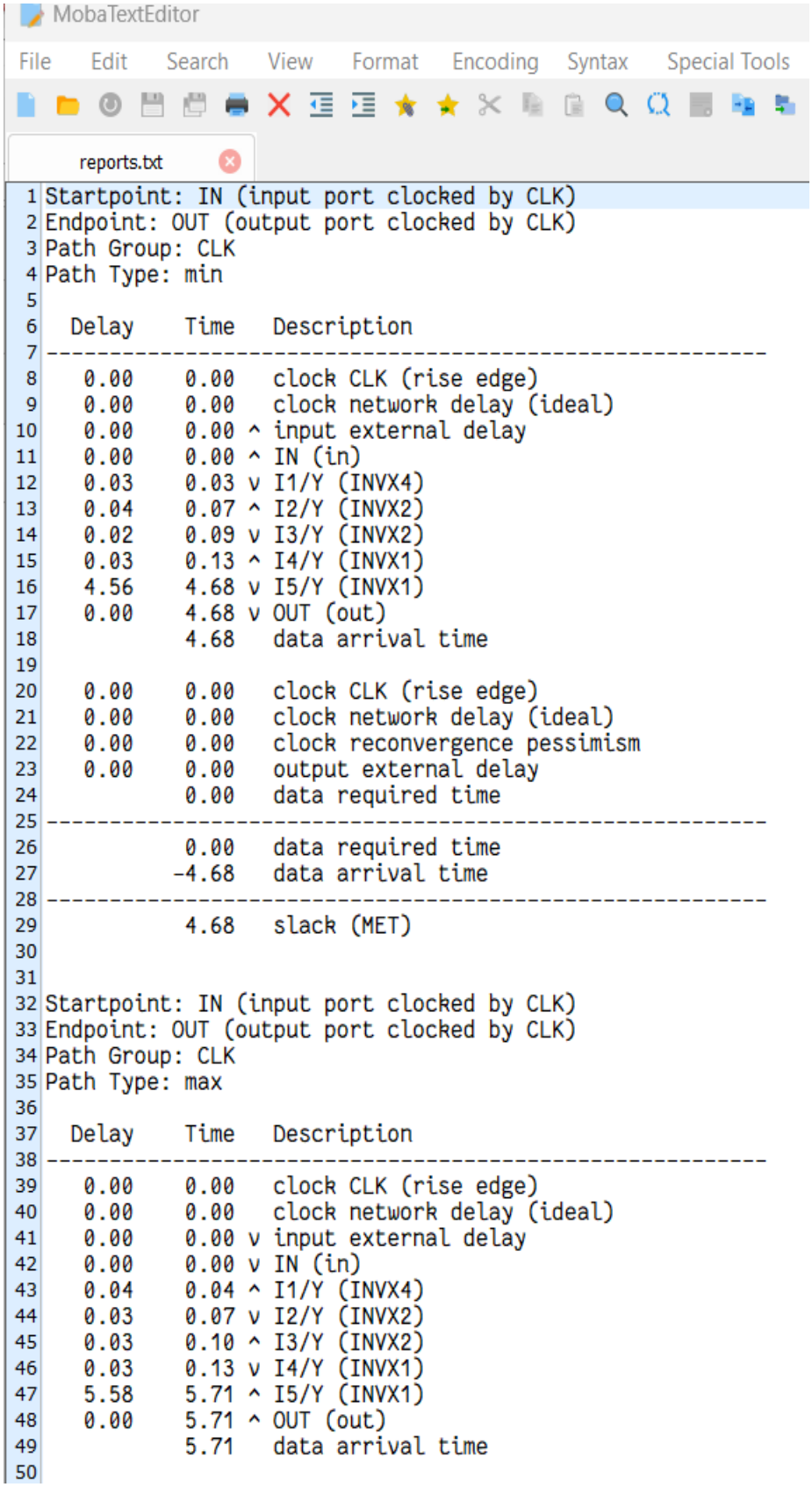

```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.03    0.06 ^ I2/Y (INVX2)
   0.03    0.09 v I3/Y (INVX1)
   0.04    0.13 ^ I4/Y (INVX1)
   4.56    4.68 v I5/Y (INVX1)
   0.00    4.68 v OUT (out)
           4.68   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.68   data arrival time
---------------------------------------------------------
           4.68   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX2)
   0.03    0.10 ^ I3/Y (INVX1)
   0.03    0.13 v I4/Y (INVX1)
   5.57    5.71 ^ I5/Y (INVX1)
   0.00    5.71 ^ OUT (out)
           5.71   data arrival time
```

Now for the I3,



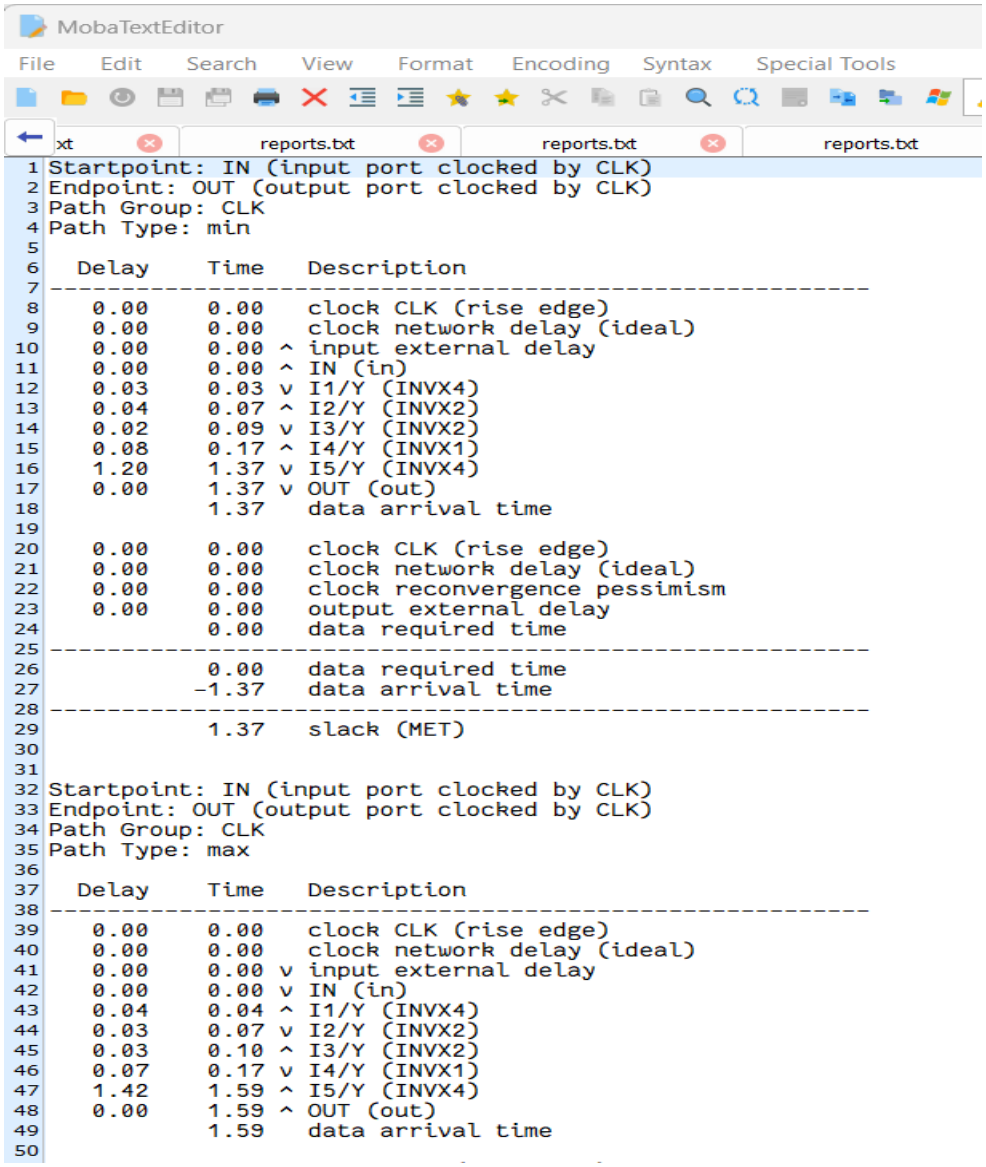

```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.04    0.07 ^ I2/Y (INVX2)
   0.02    0.09 v I3/Y (INVX2)
   0.03    0.13 ^ I4/Y (INVX1)
   4.56    4.68 v I5/Y (INVX1)
   0.00    4.68 v OUT (out)
           4.68   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.68   data arrival time
---------------------------------------------------------
           4.68   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX2)
   0.03    0.10 ^ I3/Y (INVX2)
   0.03    0.13 v I4/Y (INVX1)
   5.58    5.71 ^ I5/Y (INVX1)
   0.00    5.71 ^ OUT (out)
           5.71   data arrival time

```

Now for the I4,




```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.04    0.07 ^ I2/Y (INVX2)
   0.02    0.09 v I3/Y (INVX2)
   0.03    0.13 ^ I4/Y (INVX1)
   4.56    4.68 v I5/Y (INVX1)
   0.00    4.68 v OUT (out)
           4.68   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -4.68   data arrival time
---------------------------------------------------------
           4.68   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX2)
   0.03    0.10 ^ I3/Y (INVX2)
   0.03    0.13 v I4/Y (INVX1)
   5.58    5.71 ^ I5/Y (INVX1)
   0.00    5.71 ^ OUT (out)
           5.71   data arrival time

```

Now for I5,




```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.04    0.07 ^ I2/Y (INVX2)
   0.02    0.09 v I3/Y (INVX2)
   0.08    0.17 ^ I4/Y (INVX1)
   1.20    1.37 v I5/Y (INVX4)
   0.00    1.37 v OUT (out)
           1.37   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -1.37   data arrival time
---------------------------------------------------------
           1.37   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX2)
   0.03    0.10 ^ I3/Y (INVX2)
   0.07    0.17 v I4/Y (INVX1)
   1.42    1.59 ^ I5/Y (INVX4)
   0.00    1.59 ^ OUT (out)
           1.59   data arrival time
```

I1 at X1 – 0.04 – 4.72 , X2 – 0.03 – 4.70 , X3 – 0.03 -4.70 , X4 – 0.03 – 4.69 (set at X4)

I2 at X1 – 0.04 – 4.69, X2 – 0.03 – 4.68 , X3 – 0.03 – 4.69 , X4 – 0.03 -4.69 (set at X2)

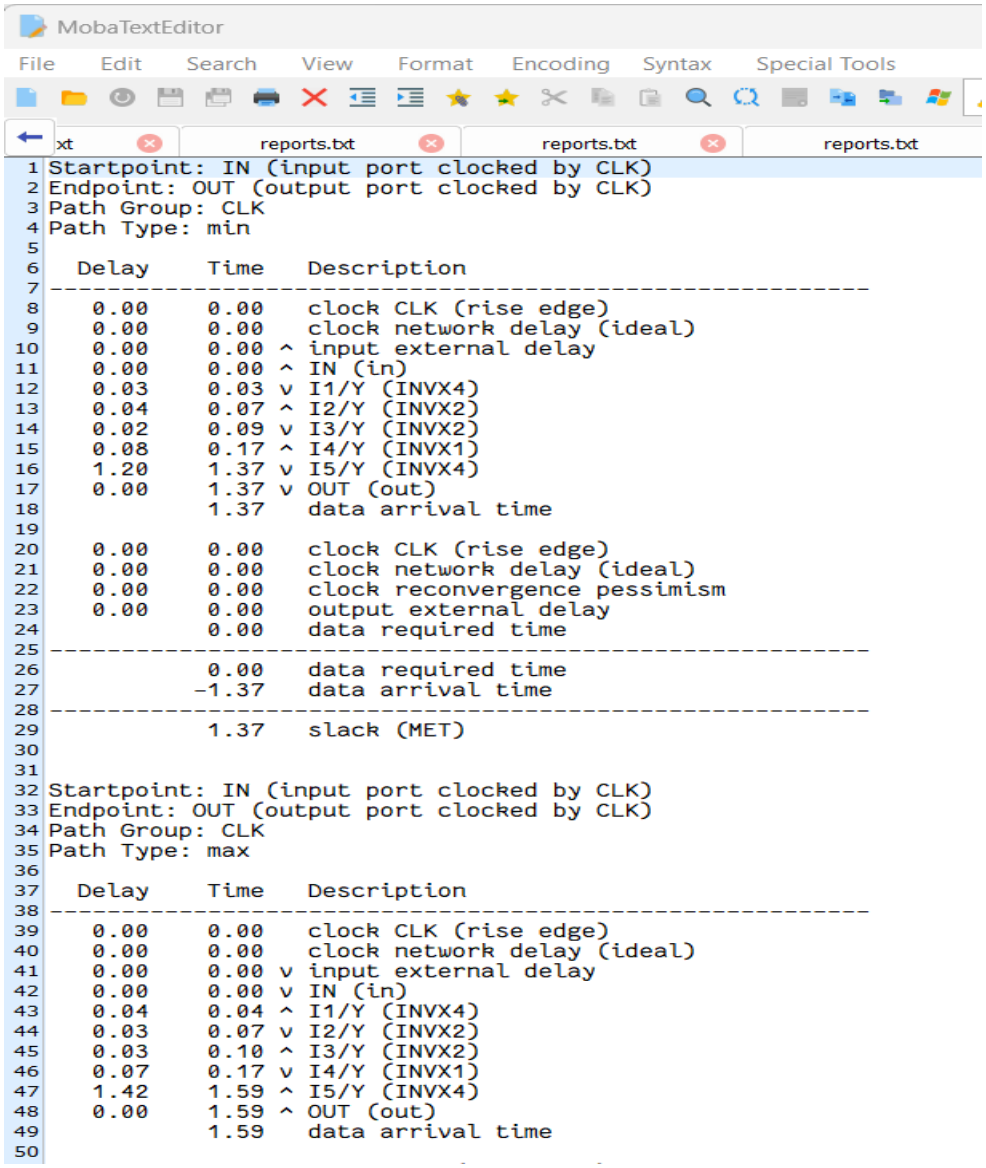
I3 at X1 – 0.03 – 4.68, X2 – 0.02-4.68, X3 – 0.02 – 4.69, X4 – 0.02 – 4.70 (set at X2)

I4 at X1 – 0.03 – 4.68, X2 – 0.03 -4.69, X3 – 0.03 – 4.70, X4 – 0.03 – 4.70 (set at X1)

I5 at X1 – 4.56 – 4.68, X2 – 2.33 -2.47, X3 – 1.55 – 1.71, X4 – 1.16 – 1.31 (set at X4)

Inverter	I1/X4	I2/X2	I3/X2	I4/X1	I5/X4
Delay	0.03	0.03	0.02	0.03	1.20
Total Delay (Min)	4.69	4.68	4.68	4.68	1.37
Total Delay (Max)	5.71	5.71	5.71	5.71	1.59

Q6) - Report the minimum total path delay and the minimum total area (add the area of all instances) obtained in the above exercise. Analyse and comment on the result. [2+3 Marks]




```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.04    0.07 ^ I2/Y (INVX2)
   0.02    0.09 v I3/Y (INVX2)
   0.08    0.17 ^ I4/Y (INVX1)
   1.20    1.37 v I5/Y (INVX4)
   0.00    1.37 v OUT (out)
           1.37   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -1.37   data arrival time
---------------------------------------------------------
           1.37   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX2)
   0.03    0.10 ^ I3/Y (INVX2)
   0.07    0.17 v I4/Y (INVX1)
   1.42    1.59 ^ I5/Y (INVX4)
   0.00    1.59 ^ OUT (out)
           1.59   data arrival time
```

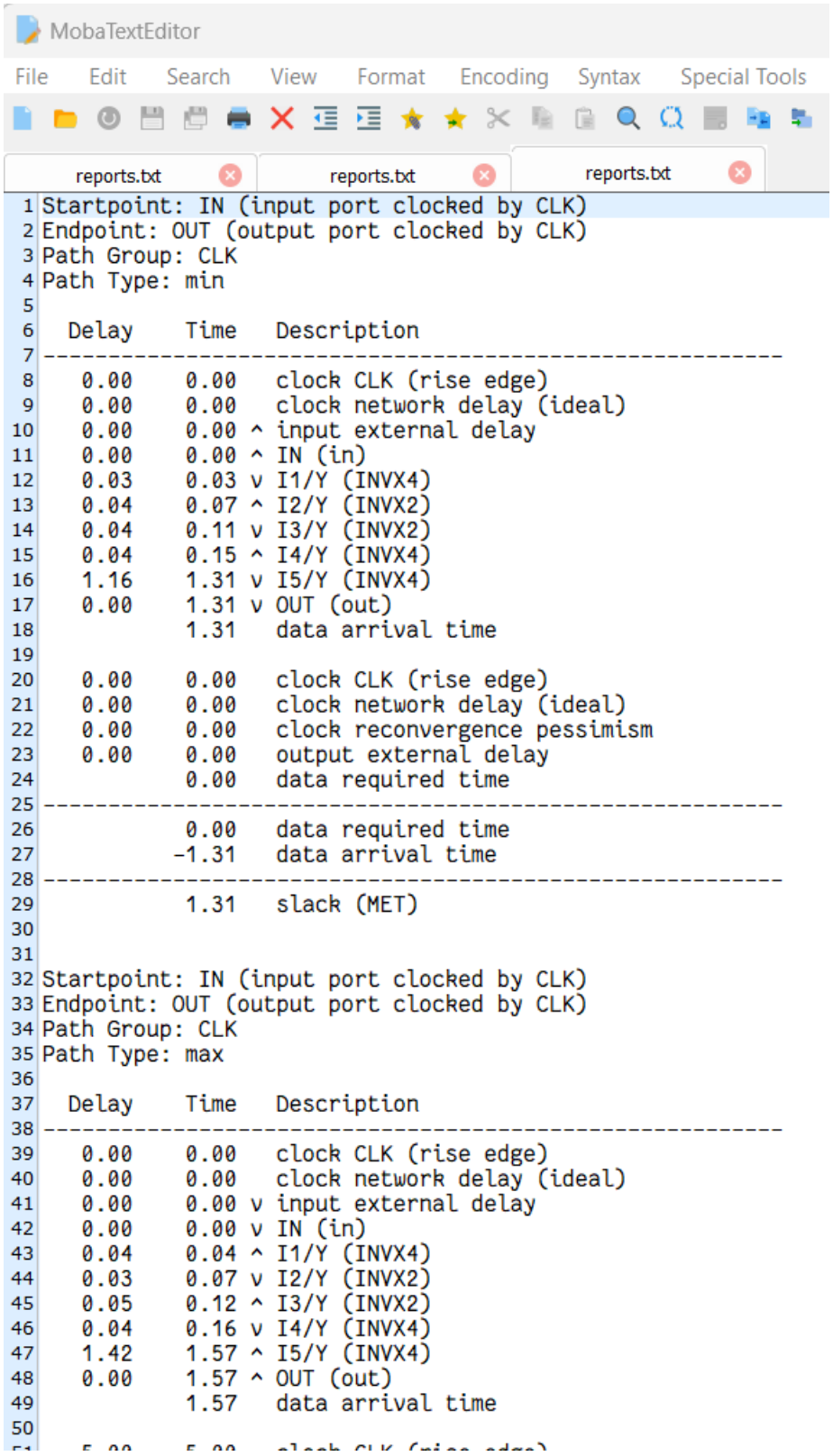
In this, the total path delay is 1.37 (min) and 1.59(max).

Suppose X1 Area-1, X2-2, X3-3, X4-4.

Total Area - 4+2+2+1+4 = 13

So, by increasing the driving strength and the sizes of inverters, the capacitor can be driven in less time. So ultimately, the delay decreases in it.

Also, the slack is also decreased because the slack is equal to the RT-AT. (By doing all this, the arrival time is get decreased.




```
Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: min

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ input external delay
   0.00    0.00 ^ IN (in)
   0.03    0.03 v I1/Y (INVX4)
   0.04    0.07 ^ I2/Y (INVX2)
   0.04    0.11 v I3/Y (INVX2)
   0.04    0.15 ^ I4/Y (INVX4)
   1.16    1.31 v I5/Y (INVX4)
   0.00    1.31 v OUT (out)
           1.31   data arrival time

   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00   clock reconvergence pessimism
   0.00    0.00   output external delay
           0.00   data required time
---------------------------------------------------------
           0.00   data required time
          -1.31   data arrival time
---------------------------------------------------------
           1.31   slack (MET)


Startpoint: IN (input port clocked by CLK)
Endpoint: OUT (output port clocked by CLK)
Path Group: CLK
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock CLK (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 v input external delay
   0.00    0.00 v IN (in)
   0.04    0.04 ^ I1/Y (INVX4)
   0.03    0.07 v I2/Y (INVX2)
   0.05    0.12 ^ I3/Y (INVX2)
   0.04    0.16 v I4/Y (INVX4)
   1.42    1.57 ^ I5/Y (INVX4)
   0.00    1.57 ^ OUT (out)
           1.57   data arrival time
```

In this, the total path Delay is 1.31(min) and 1.57(max).

Suppose X1 Area – 1, X2-2, X3-3, X4-4.

Total Area = 4+2+2+4+4 = 16

In this, the area is more but the delay is less compared to the above situation.