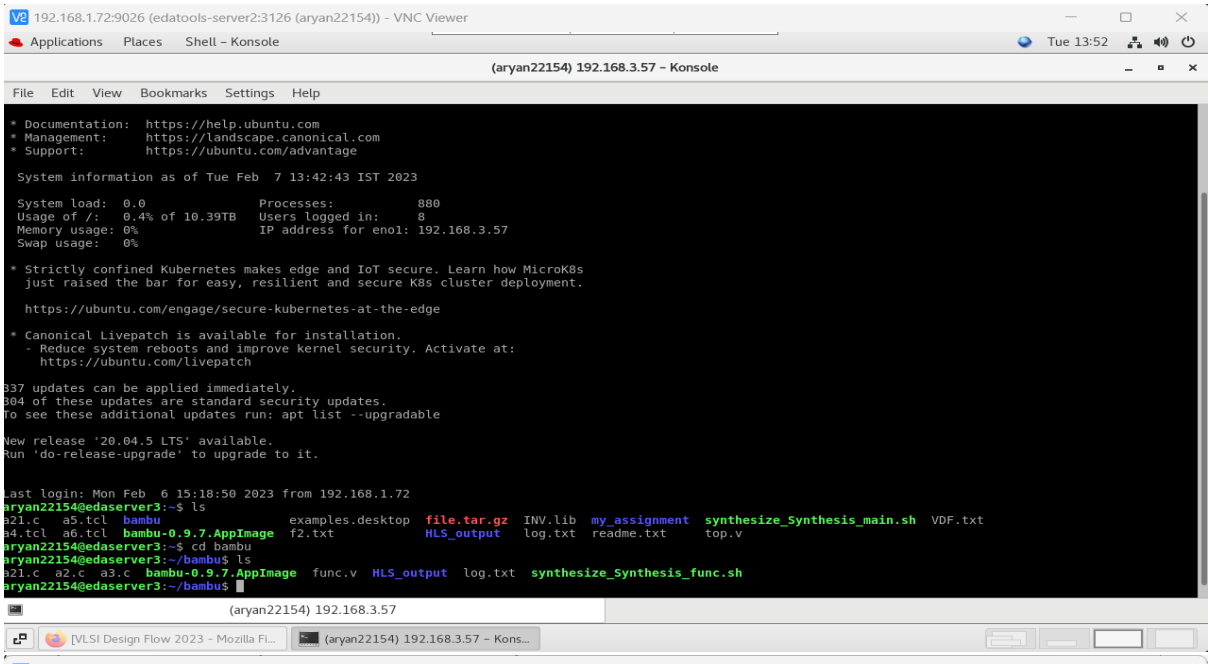
ASSIGNMENT -2

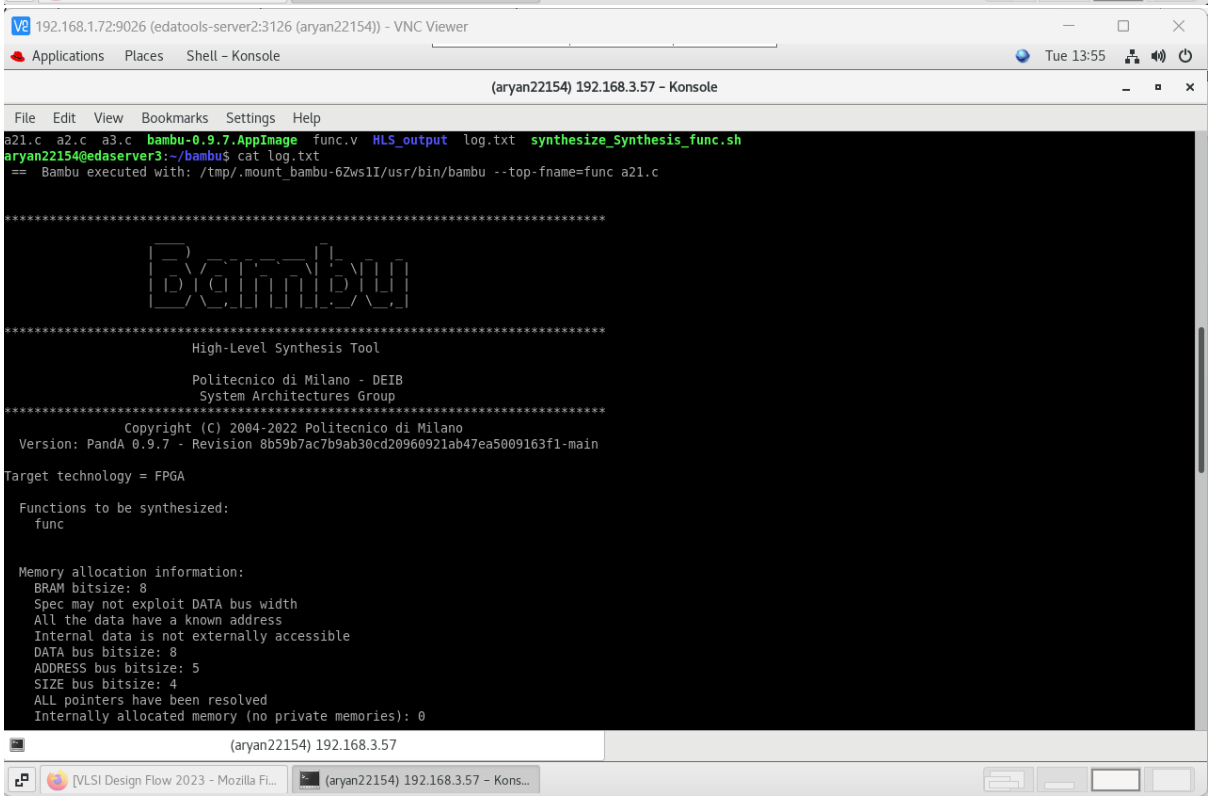
Name: - Aryan Gupta

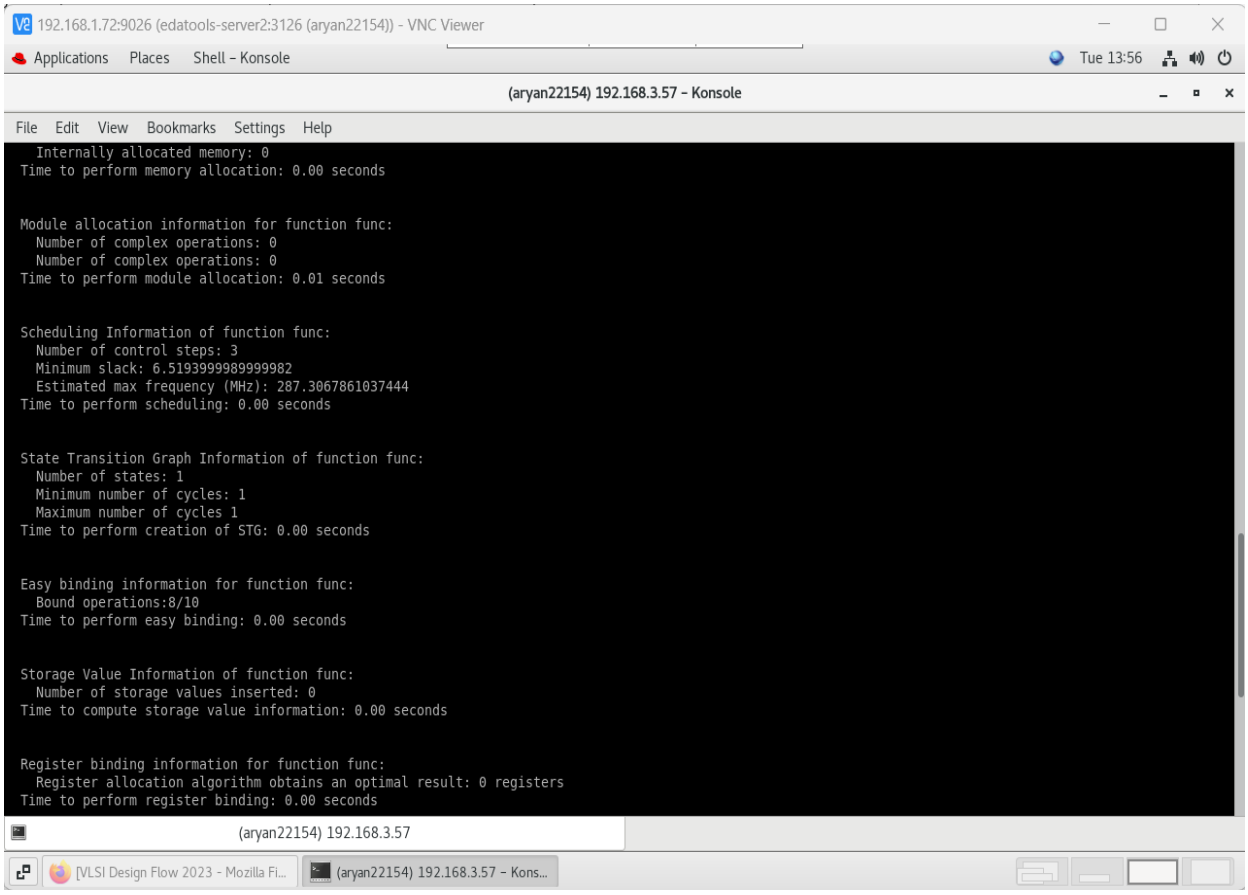
Roll No- MT22154

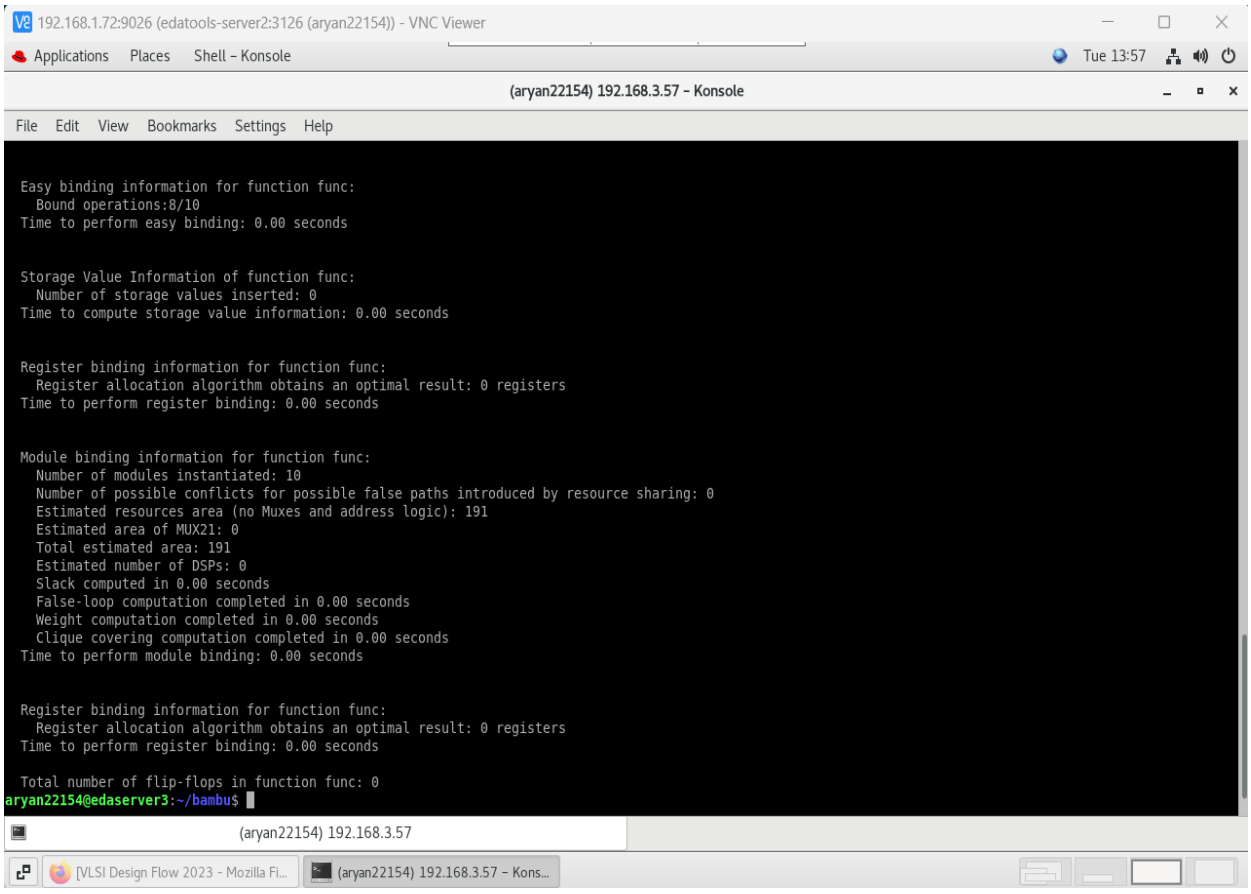
VLSI Design Flow (Submitted to Prof. Sneh Saurabh)

Q1)- Show a screenshot or snippet of the log file to prove that you have indeed run the tool [If this is not given, then your assignment will not be evaluated].






192.168.1.72:9026 (edatools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
Tue 13:56
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
Internally allocated memory: 0
Time to perform memory allocation: 0.00 seconds
Module allocation information for function func:
Number of complex operations: 0
Number of complex operations: 0
Time to perform module allocation: 0.01 seconds
Scheduling Information of function func:
Number of control steps: 3
Minimum slack: 6.5193999989999982
Estimated max frequency (MHz): 287.3067861037444
Time to perform scheduling: 0.00 seconds
State Transition Graph Information of function func:
Number of states: 1
Minimum number of cycles: 1
Maximum number of cycles 1
Time to perform creation of STG: 0.00 seconds
Easy binding information for function func:
Bound operations:8/10
Time to perform easy binding: 0.00 seconds
Storage Value Information of function func:
Number of storage values inserted: 0
Time to compute storage value information: 0.00 seconds
Register binding information for function func:
Register allocation algorithm obtains an optimal result: 0 registers
Time to perform register binding: 0.00 seconds
(aryan22154) 192.168.3.57
[VLSI Design Flow 2023 - Mozilla Fi...
(aryan22154) 192.168.3.57 – Kons...


192.168.1.72:9026 (edatools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
Tue 13:57
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
Easy binding information for function func:
Bound operations:8/10
Time to perform easy binding: 0.00 seconds
Storage Value Information of function func:
Number of storage values inserted: 0
Time to compute storage value information: 0.00 seconds
Register binding information for function func:
Register allocation algorithm obtains an optimal result: 0 registers
Time to perform register binding: 0.00 seconds
Module binding information for function func:
Number of modules instantiated: 10
Number of possible conflicts for possible false paths introduced by resource sharing: 0
Estimated resources area (no Muxes and address logic): 191
Estimated area of MUX21: 0
Total estimated area: 191
Estimated number of DSPs: 0
Slack computed in 0.00 seconds
False-loop computation completed in 0.00 seconds
Weight computation completed in 0.00 seconds
Clique covering computation completed in 0.00 seconds
Time to perform module binding: 0.00 seconds
Register binding information for function func:
Register allocation algorithm obtains an optimal result: 0 registers
Time to perform register binding: 0.00 seconds
Total number of flip-flops in function func: 0
aryan22154@edaserver3:~/bambu$
(aryan22154) 192.168.3.57
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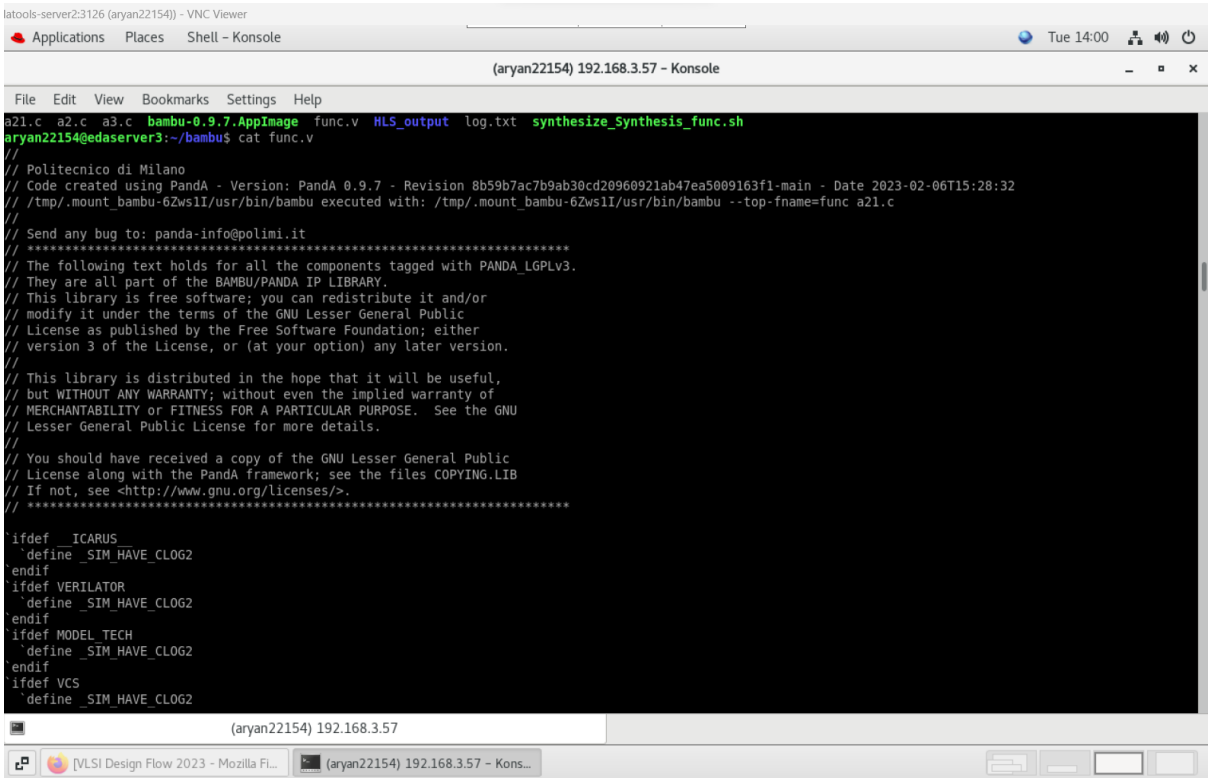
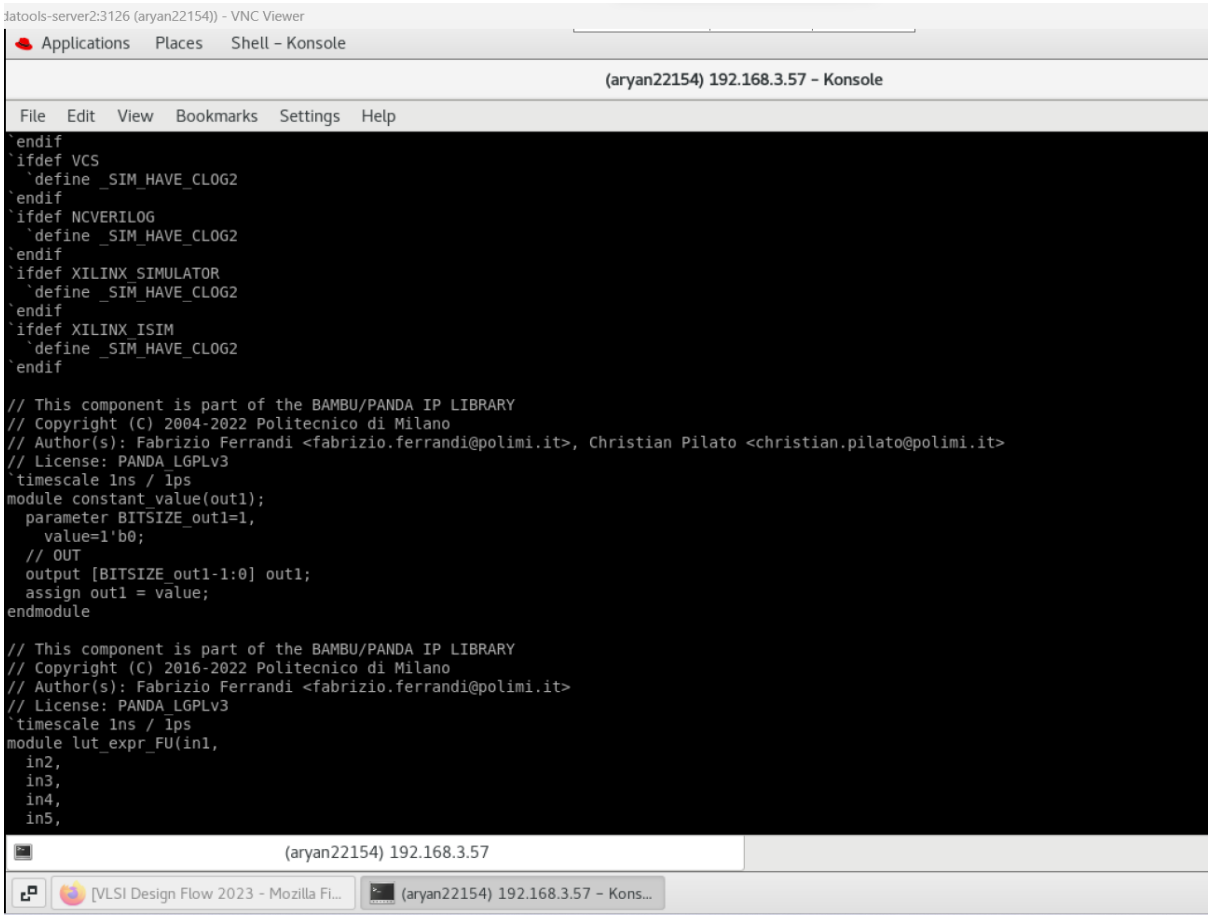
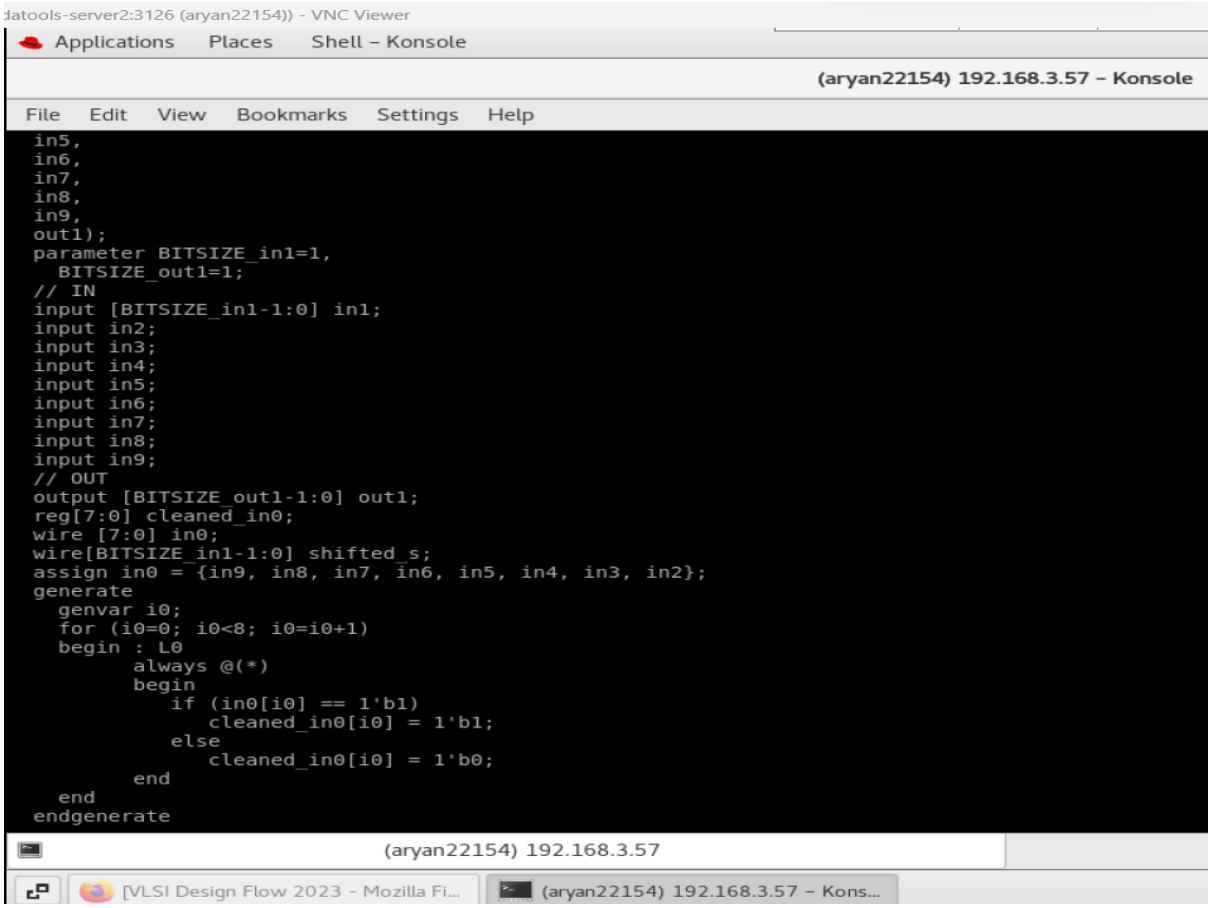
Q2) Obtain the Verilog RTL for the following C code using the HLS tool.






datools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
in5,
in6,
in7,
in8,
in9,
out1);
parameter BITSIZE_in1=1,
BITSIZE_out1=1;
// IN
input [BITSIZE_in1-1:0] in1;
input in2;
input in3;
input in4;
input in5;
input in6;
input in7;
input in8;
input in9;
// OUT
output [BITSIZE_out1-1:0] out1;
reg[7:0] cleaned_in0;
wire [7:0] in0;
wire[BITSIZE_in1-1:0] shifted_s;
assign in0 = {in9, in8, in7, in6, in5, in4, in3, in2};
generate
genvar i0;
for (i0=0; i0<8; i0=i0+1)
begin : L0
always @(*)
begin
if (in0[i0] == 1'b1)
cleaned_in0[i0] = 1'b1;
else
cleaned_in0[i0] = 1'b0;
end
end
endgenerate
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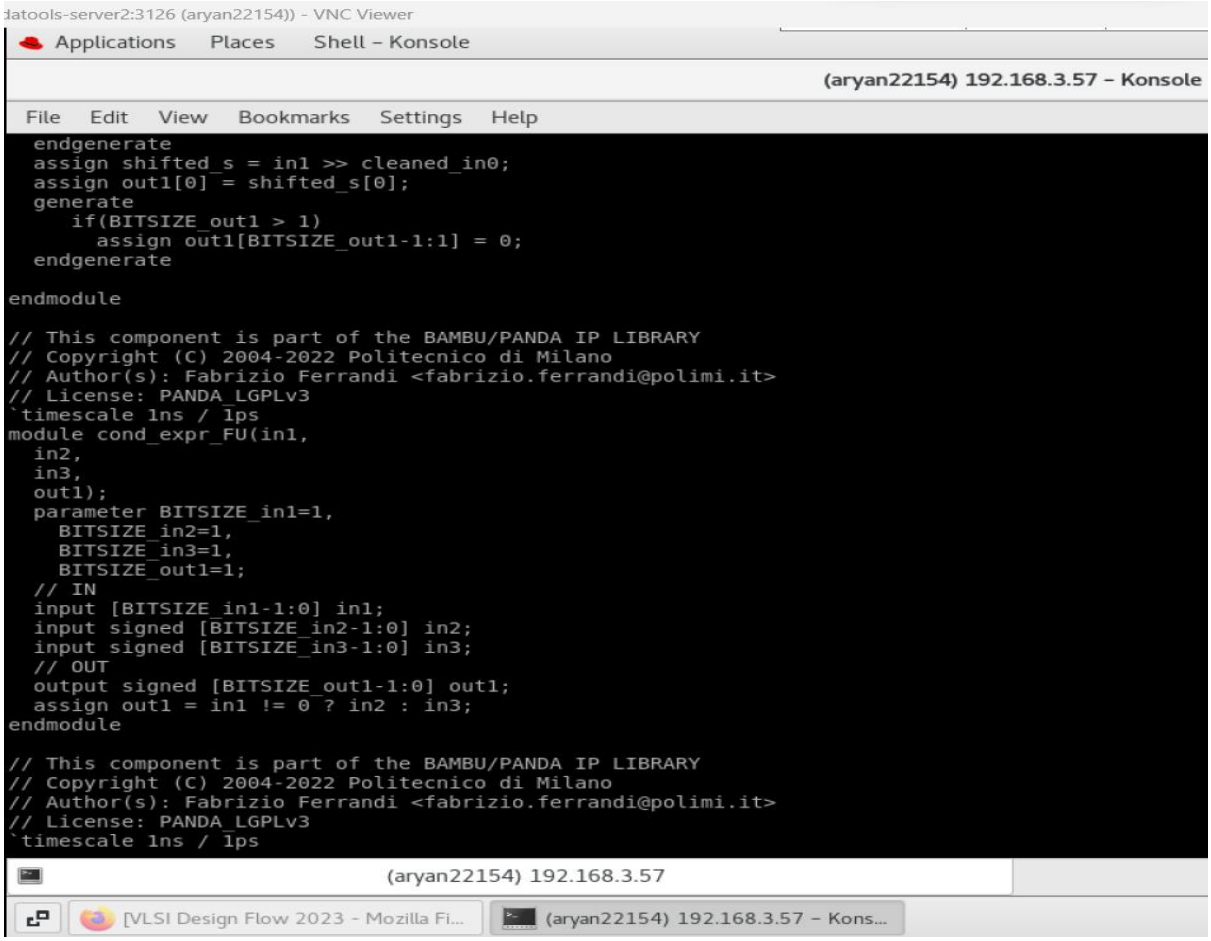
datools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
endgenerate
assign shifted_s = in1 >> cleaned_in0;
assign out1[0] = shifted_s[0];
generate
if(BITSIZE_out1 > 1)
assign out1[BITSIZE_out1-1:1] = 0;
endgenerate
endmodule
// This component is part of the BAMBU/PANDA IP LIBRARY
// Copyright (C) 2004-2022 Politecnico di Milano
// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
// License: PANDA_LGPLv3
`timescale 1ns / 1ps
module cond_expr_FU(in1,
in2,
in3,
out1);
parameter BITSIZE_in1=1,
BITSIZE_in2=1,
BITSIZE_in3=1,
BITSIZE_out1=1;
// IN
input [BITSIZE_in1-1:0] in1;
input signed [BITSIZE_in2-1:0] in2;
input signed [BITSIZE_in3-1:0] in3;
// OUT
output signed [BITSIZE_out1-1:0] out1;
assign out1 = in1 != 0 ? in2 : in3;
endmodule
// This component is part of the BAMBU/PANDA IP LIBRARY
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// License: PANDA_LGPLv3
`timescale 1ns / 1ps
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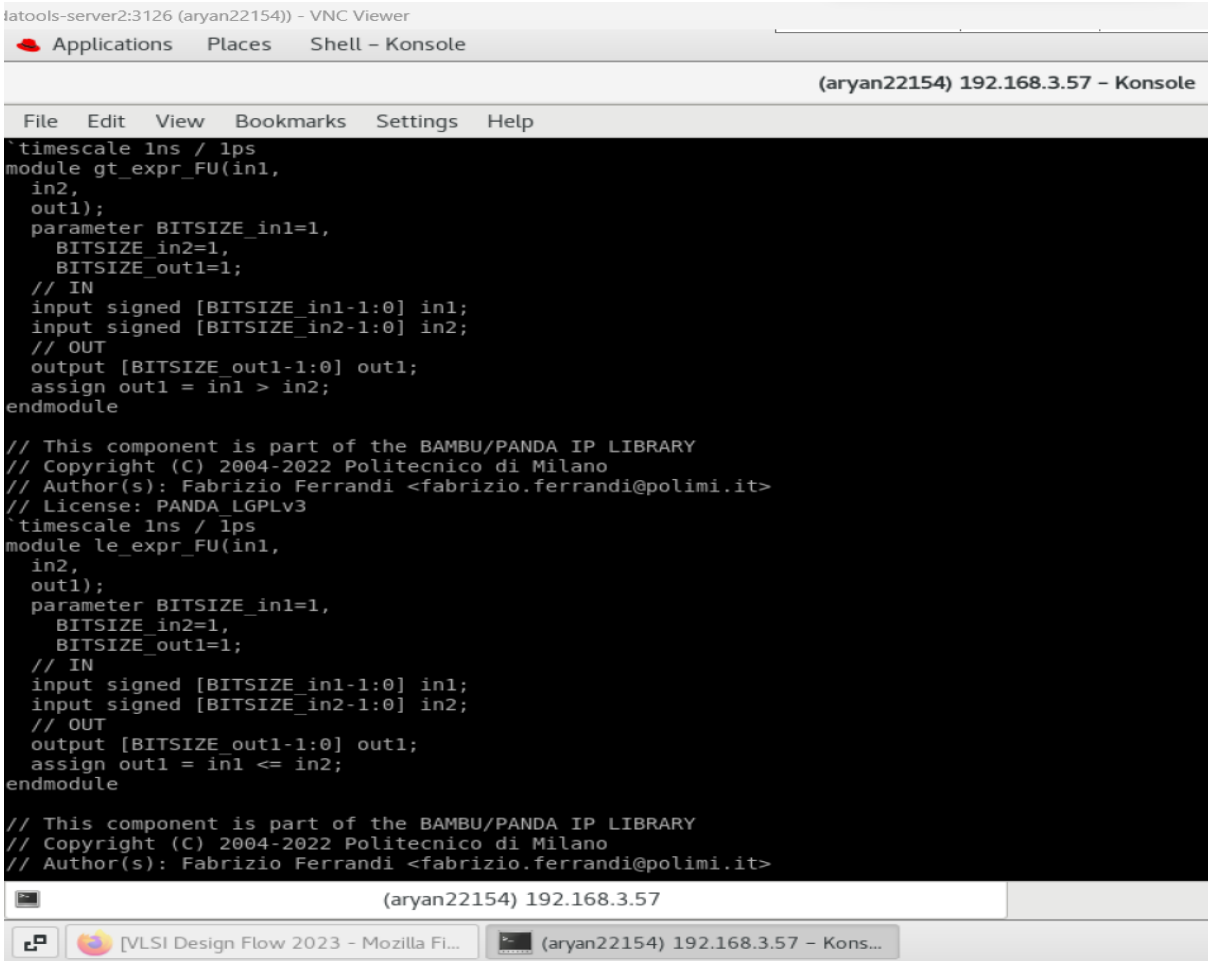
latools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
`timescale 1ns / 1ps
module gt_expr_FU(in1,
in2,
out1);
parameter BITSIZE_in1=1,
BITSIZE_in2=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
input signed [BITSIZE_in2-1:0] in2;
// OUT
output [BITSIZE_out1-1:0] out1;
assign out1 = in1 > in2;
endmodule
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`timescale 1ns / 1ps
module le_expr_FU(in1,
in2,
out1);
parameter BITSIZE_in1=1,
BITSIZE_in2=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
input signed [BITSIZE_in2-1:0] in2;
// OUT
output [BITSIZE_out1-1:0] out1;
assign out1 = in1 <= in2;
endmodule
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// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
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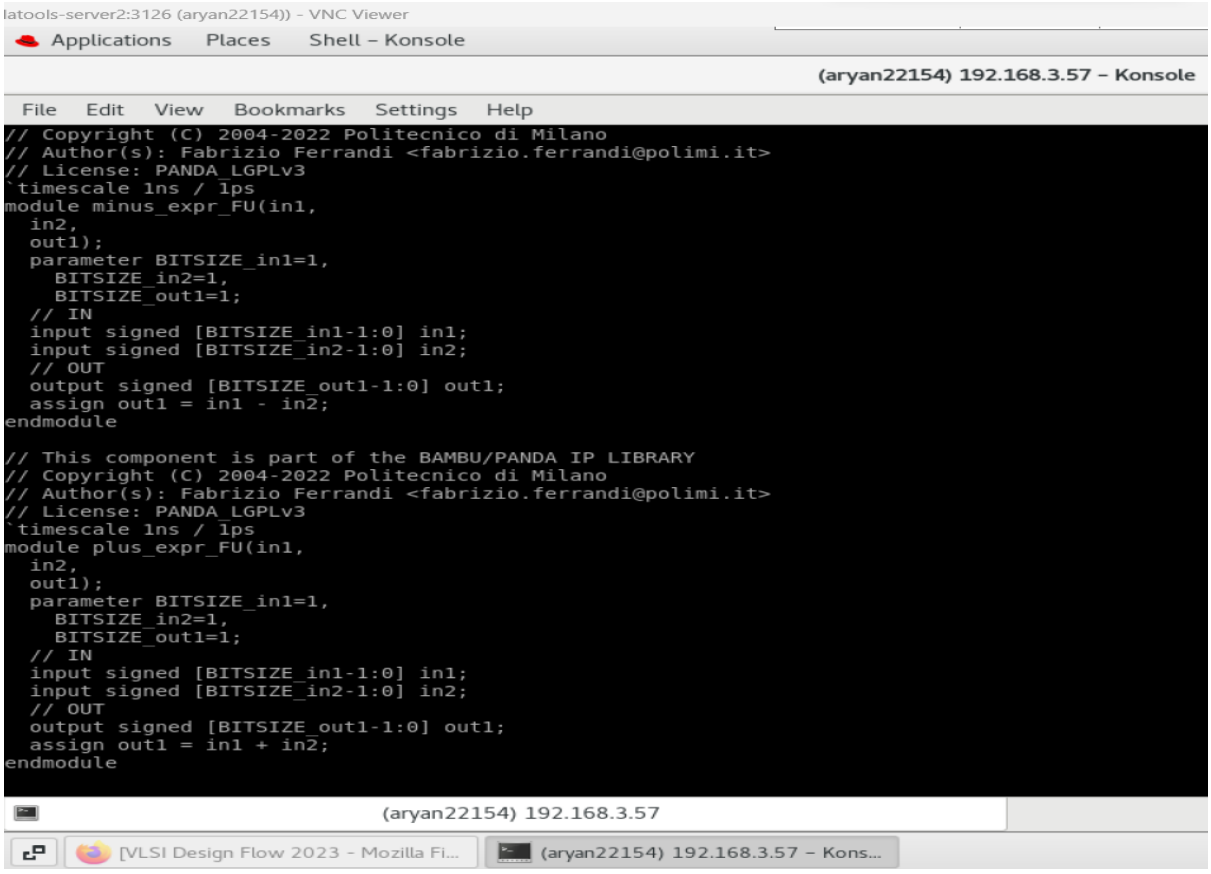
latools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
// Copyright (C) 2004-2022 Politecnico di Milano
// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
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`timescale 1ns / 1ps
module minus_expr_FU(in1,
in2,
out1);
parameter BITSIZE_in1=1,
BITSIZE_in2=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
input signed [BITSIZE_in2-1:0] in2;
// OUT
output signed [BITSIZE_out1-1:0] out1;
assign out1 = in1 - in2;
endmodule
// This component is part of the BAMBU/PANDA IP LIBRARY
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// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
// License: PANDA_LGPLv3
`timescale 1ns / 1ps
module plus_expr_FU(in1,
in2,
out1);
parameter BITSIZE_in1=1,
BITSIZE_in2=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
input signed [BITSIZE_in2-1:0] in2;
// OUT
output signed [BITSIZE_out1-1:0] out1;
assign out1 = in1 + in2;
endmodule
(aryan22154) 192.168.3.57
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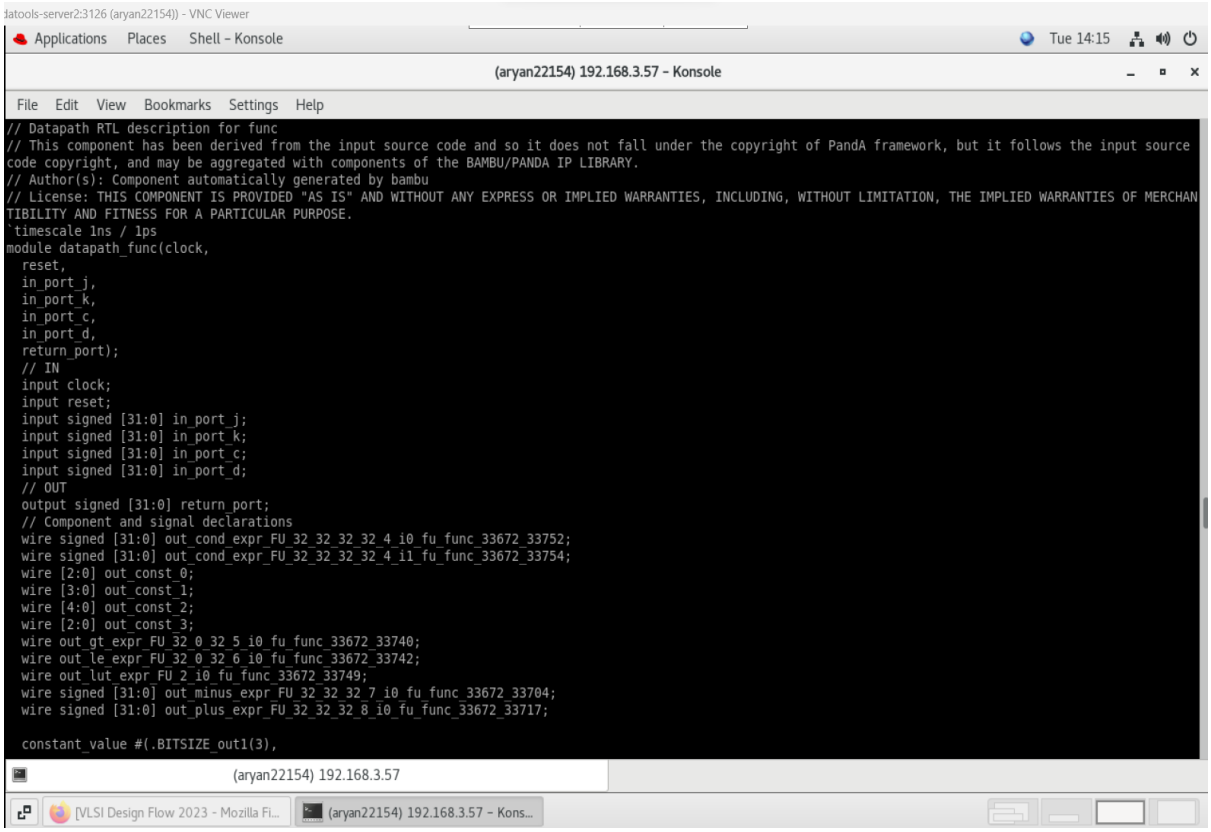
datools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
Tue 14:15
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// Datapath RTL description for func
// This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows the input source code copyright, and may be aggregated with components of the BAMBU/PANDA IP LIBRARY.
// Author(s): Component automatically generated by bambu
// License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE.
`timescale 1ns / 1ps
module datapath_func(clock,
reset,
in_port_j,
in_port_k,
in_port_c,
in_port_d,
return_port);
// IN
input clock;
input reset;
input signed [31:0] in_port_j;
input signed [31:0] in_port_k;
input signed [31:0] in_port_c;
input signed [31:0] in_port_d;
// OUT
output signed [31:0] return_port;
// Component and signal declarations
wire signed [31:0] out_cond_expr_FU_32_32_32_32_4_i0_fu_func_33672_33752;
wire signed [31:0] out_cond_expr_FU_32_32_32_32_4_i1_fu_func_33672_33754;
wire [2:0] out_const_0;
wire [3:0] out_const_1;
wire [4:0] out_const_2;
wire [2:0] out_const_3;
wire out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740;
wire out_le_expr_FU_32_0_32_6_i0_fu_func_33672_33742;
wire out_lut_expr_FU_2_i0_fu_func_33672_33749;
wire signed [31:0] out_minus_expr_FU_32_32_32_7_i0_fu_func_33672_33704;
wire signed [31:0] out_plus_expr_FU_32_32_32_8_i0_fu_func_33672_33717;
constant_value #(.BITSIZE_out1(3),
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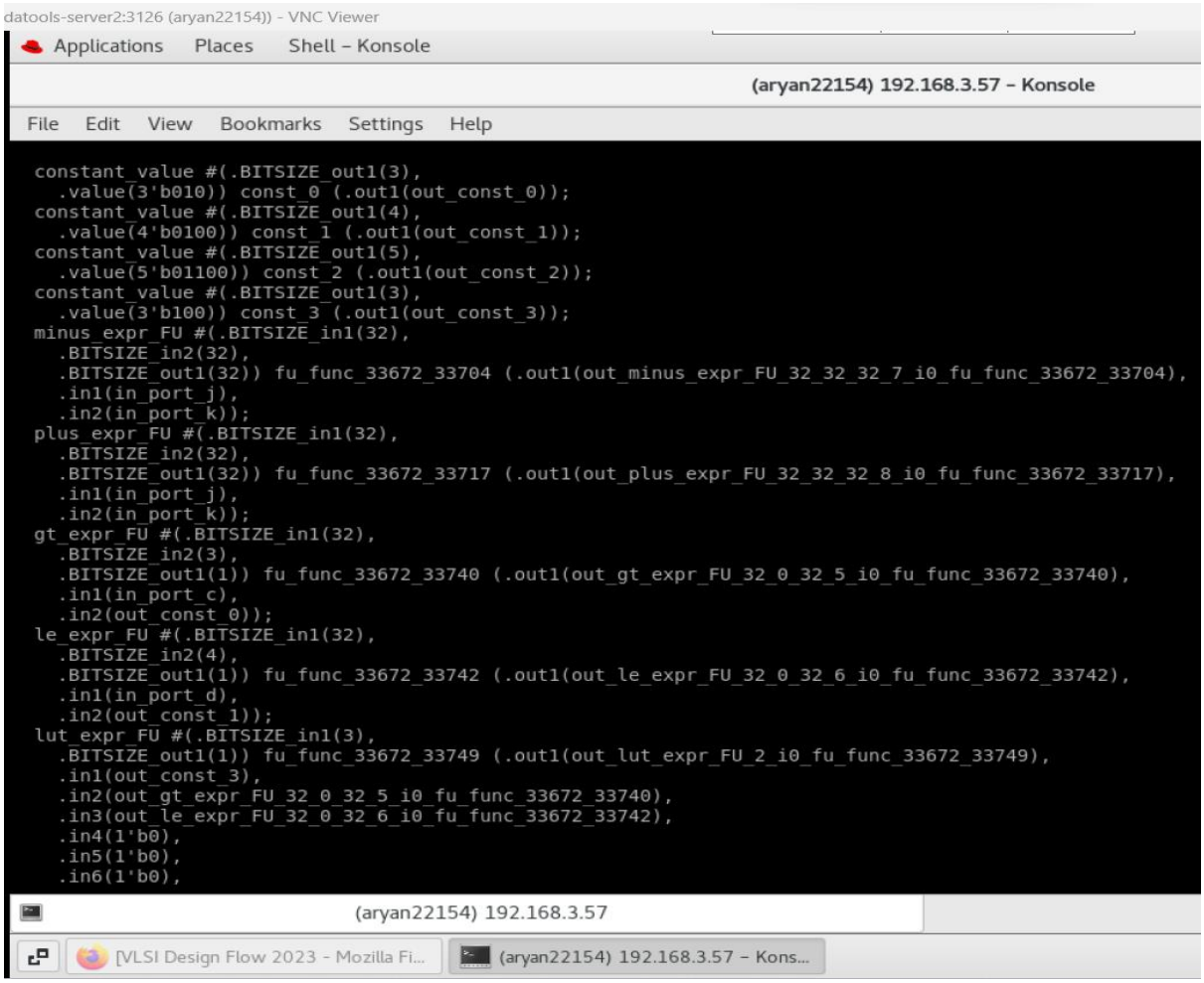
datools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
constant_value #(.BITSIZE_out1(3),
.value(3'b010)) const_0 (.out1(out_const_0));
constant_value #(.BITSIZE_out1(4),
.value(4'b0100)) const_1 (.out1(out_const_1));
constant_value #(.BITSIZE_out1(5),
.value(5'b01100)) const_2 (.out1(out_const_2));
constant_value #(.BITSIZE_out1(3),
.value(3'b100)) const_3 (.out1(out_const_3));
minus_expr_FU #(.BITSIZE_in1(32),
.BITSIZE_in2(32),
.BITSIZE_out1(32)) fu_func_33672_33704 (.out1(out_minus_expr_FU_32_32_32_7_i0_fu_func_33672_33704),
.in1(in_port_j),
.in2(in_port_k));
plus_expr_FU #(.BITSIZE_in1(32),
.BITSIZE_in2(32),
.BITSIZE_out1(32)) fu_func_33672_33717 (.out1(out_plus_expr_FU_32_32_32_8_i0_fu_func_33672_33717),
.in1(in_port_j),
.in2(in_port_k));
gt_expr_FU #(.BITSIZE_in1(32),
.BITSIZE_in2(3),
.BITSIZE_out1(1)) fu_func_33672_33740 (.out1(out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740),
.in1(in_port_c),
.in2(out_const_0));
le_expr_FU #(.BITSIZE_in1(32),
.BITSIZE_in2(4),
.BITSIZE_out1(1)) fu_func_33672_33742 (.out1(out_le_expr_FU_32_0_32_6_i0_fu_func_33672_33742),
.in1(in_port_d),
.in2(out_const_1));
lut_expr_FU #(.BITSIZE_in1(3),
.BITSIZE_out1(1)) fu_func_33672_33749 (.out1(out_lut_expr_FU_2_i0_fu_func_33672_33749),
.in1(out_const_3),
.in2(out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740),
.in3(out_le_expr_FU_32_0_32_6_i0_fu_func_33672_33742),
.in4(1'b0),
.in5(1'b0),
.in6(1'b0),
(aryan22154) 192.168.3.57
[VLSI Design Flow 2023 - Mozilla Fi...
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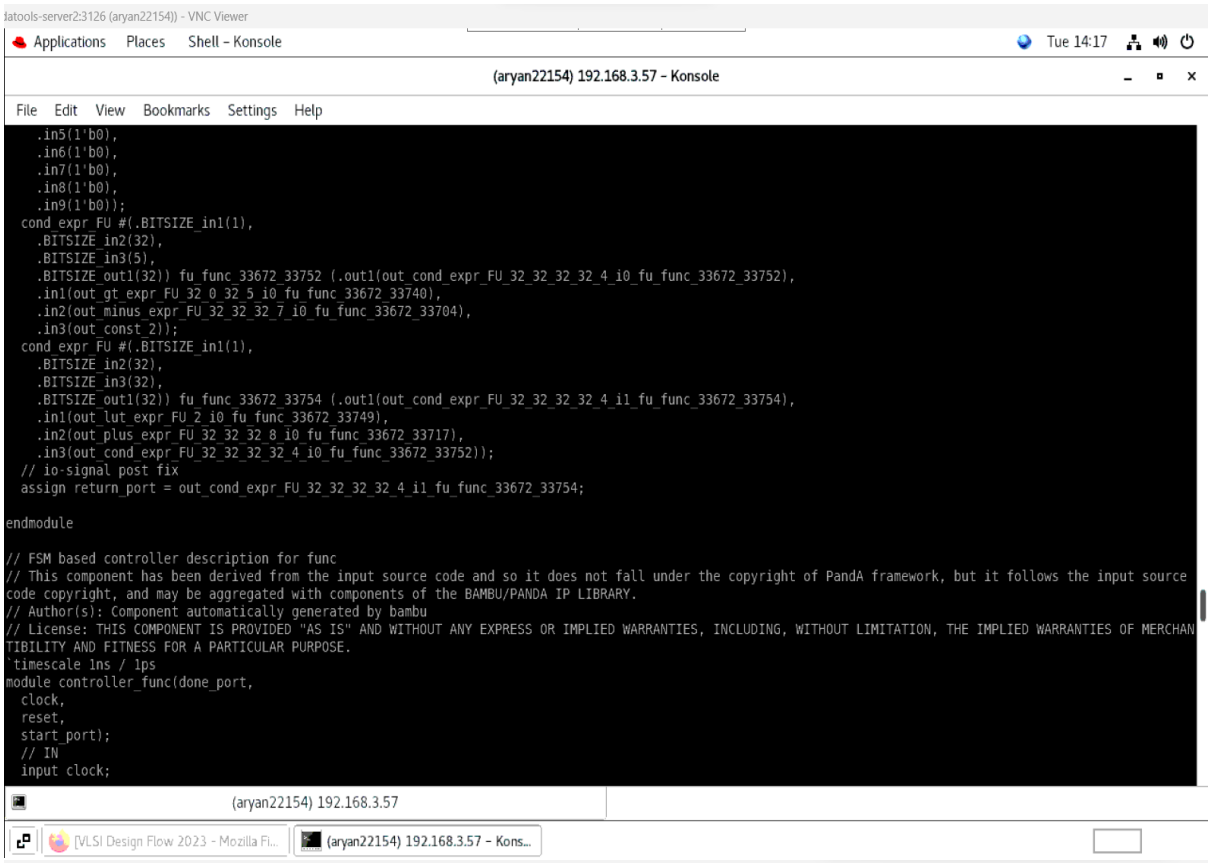
datools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
Tue 14:17
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
.in5(1'b0),
.in6(1'b0),
.in7(1'b0),
.in8(1'b0),
.in9(1'b0));
cond_expr_FU #(.BITSIZE_in1(1),
.BITSIZE_in2(32),
.BITSIZE_in3(5),
.BITSIZE_out1(32)) fu_func_33672_33752 (.out1(out_cond_expr_FU_32_32_32_32_4_i0_fu_func_33672_33752),
.in1(out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740),
.in2(out_minus_expr_FU_32_32_32_7_i0_fu_func_33672_33704),
.in3(out_const_2));
cond_expr_FU #(.BITSIZE_in1(1),
.BITSIZE_in2(32),
.BITSIZE_in3(32),
.BITSIZE_out1(32)) fu_func_33672_33754 (.out1(out_cond_expr_FU_32_32_32_32_4_i1_fu_func_33672_33754),
.in1(out_lut_expr_FU_2_i0_fu_func_33672_33749),
.in2(out_plus_expr_FU_32_32_32_8_i0_fu_func_33672_33717),
.in3(out_cond_expr_FU_32_32_32_32_4_i0_fu_func_33672_33752));
// io-signal post fix
assign return_port = out_cond_expr_FU_32_32_32_32_4_i1_fu_func_33672_33754;
endmodule
// FSM based controller description for func
// This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows the input source code copyright, and may be aggregated with components of the BAMBU/PANDA IP LIBRARY.
// Author(s): Component automatically generated by bambu
// License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE.
`timescale 1ns / 1ps
module controller_func(done_port,
clock,
reset,
start_port);
// IN
input clock;
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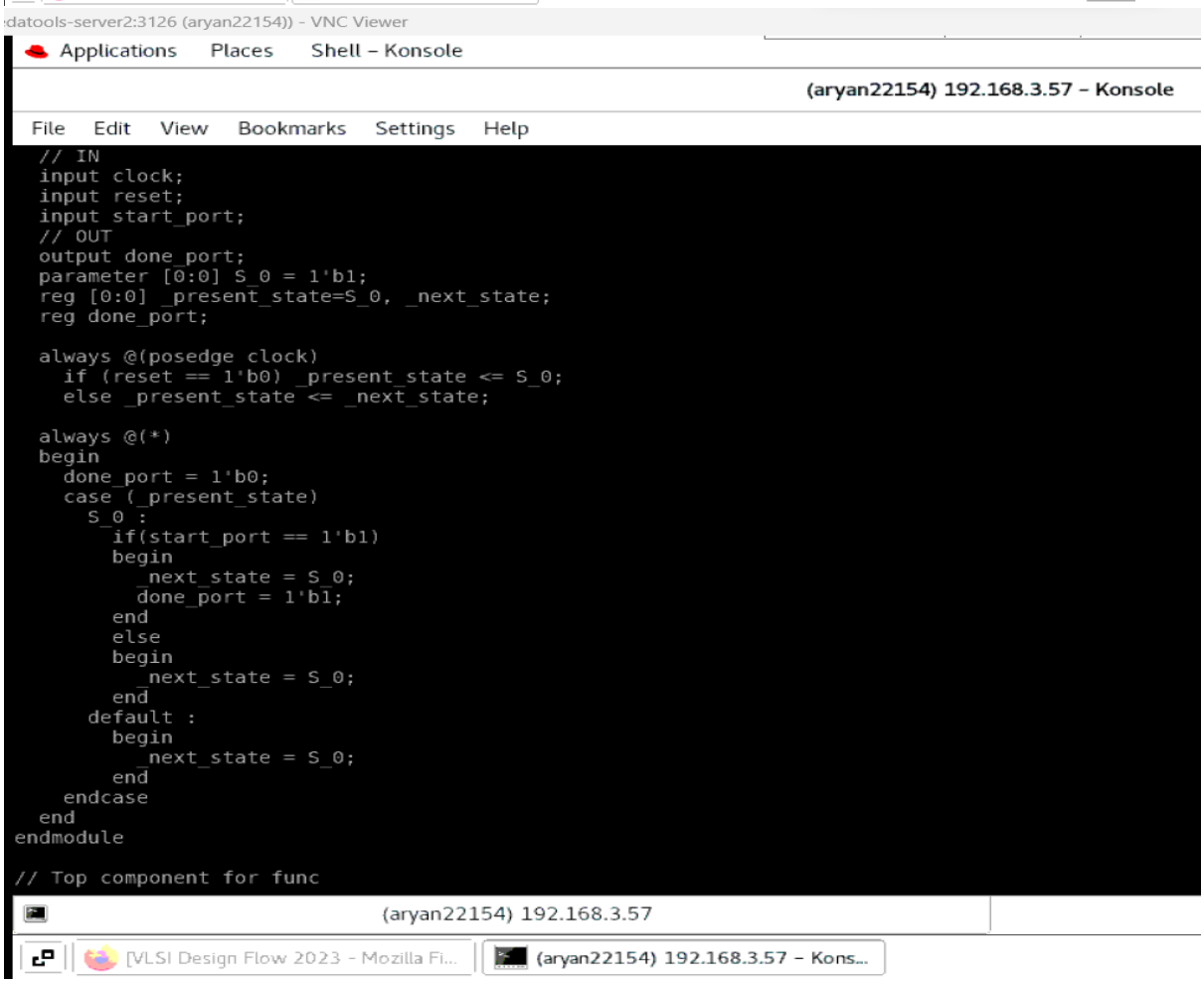
datools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
// IN
input clock;
input reset;
input start_port;
// OUT
output done_port;
parameter [0:0] S_0 = 1'b1;
reg [0:0] _present_state=S_0, _next_state;
reg done_port;
always @(posedge clock)
if (reset == 1'b0) _present_state <= S_0;
else _present_state <= _next_state;
always @(*)
begin
done_port = 1'b0;
case (_present_state)
S_0 :
if(start_port == 1'b1)
begin
_next_state = S_0;
done_port = 1'b1;
end
else
begin
_next_state = S_0;
end
default :
begin
_next_state = S_0;
end
endcase
end
endmodule
// Top component for func
(aryan22154) 192.168.3.57
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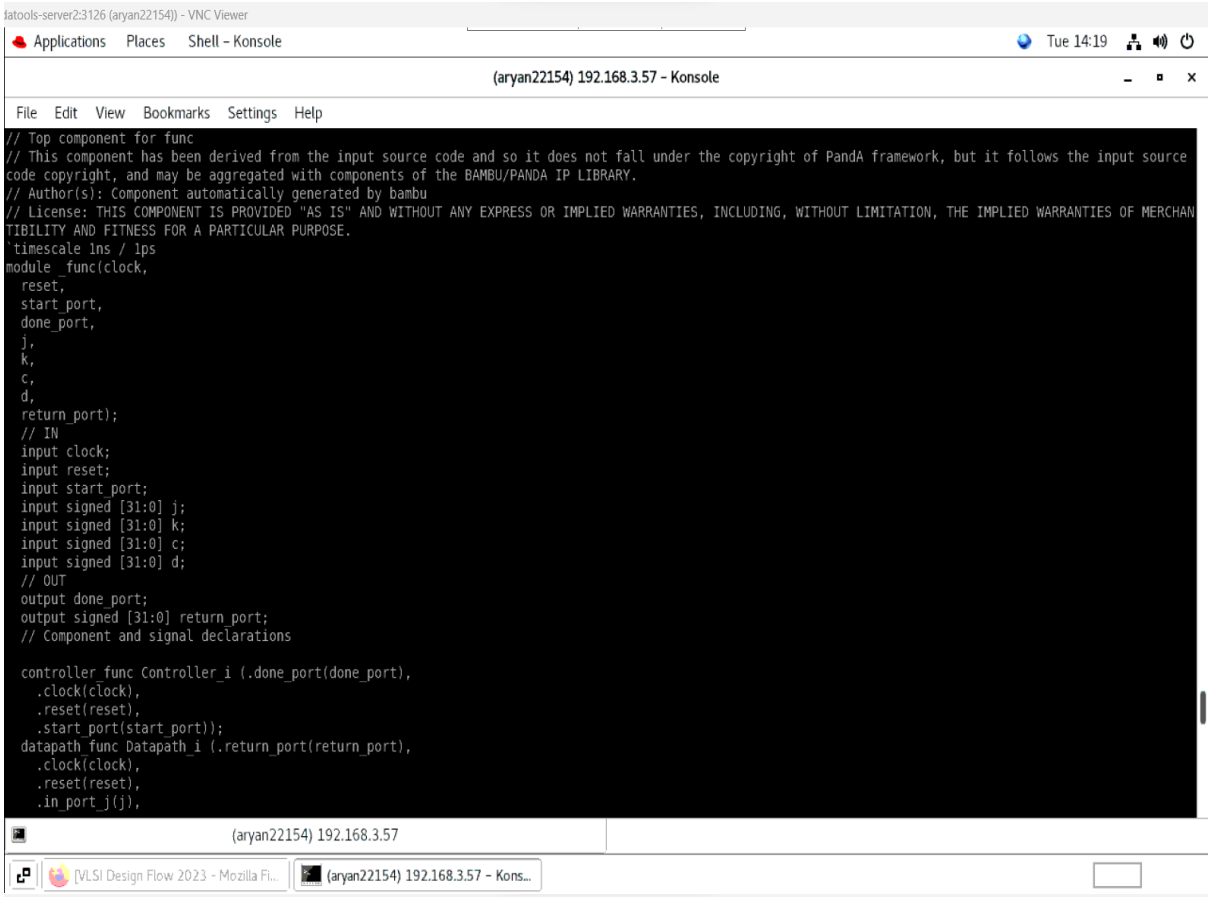
/atools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
Tue 14:19
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
// Top component for func
// This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows the input source code copyright, and may be aggregated with components of the BAMBU/PANDA IP LIBRARY.
// Author(s): Component automatically generated by bambu
// License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE.
`timescale 1ns / 1ps
module _func(clock,
reset,
start_port,
done_port,
j,
k,
c,
d,
return_port);
// IN
input clock;
input reset;
input start_port;
input signed [31:0] j;
input signed [31:0] k;
input signed [31:0] c;
input signed [31:0] d;
// OUT
output done_port;
output signed [31:0] return_port;
// Component and signal declarations
controller_func Controller_i (.done_port(done_port),
.clock(clock),
.reset(reset),
.start_port(start_port));
datapath_func Datapath_i (.return_port(return_port),
.clock(clock),
.reset(reset),
.in_port_j(j),
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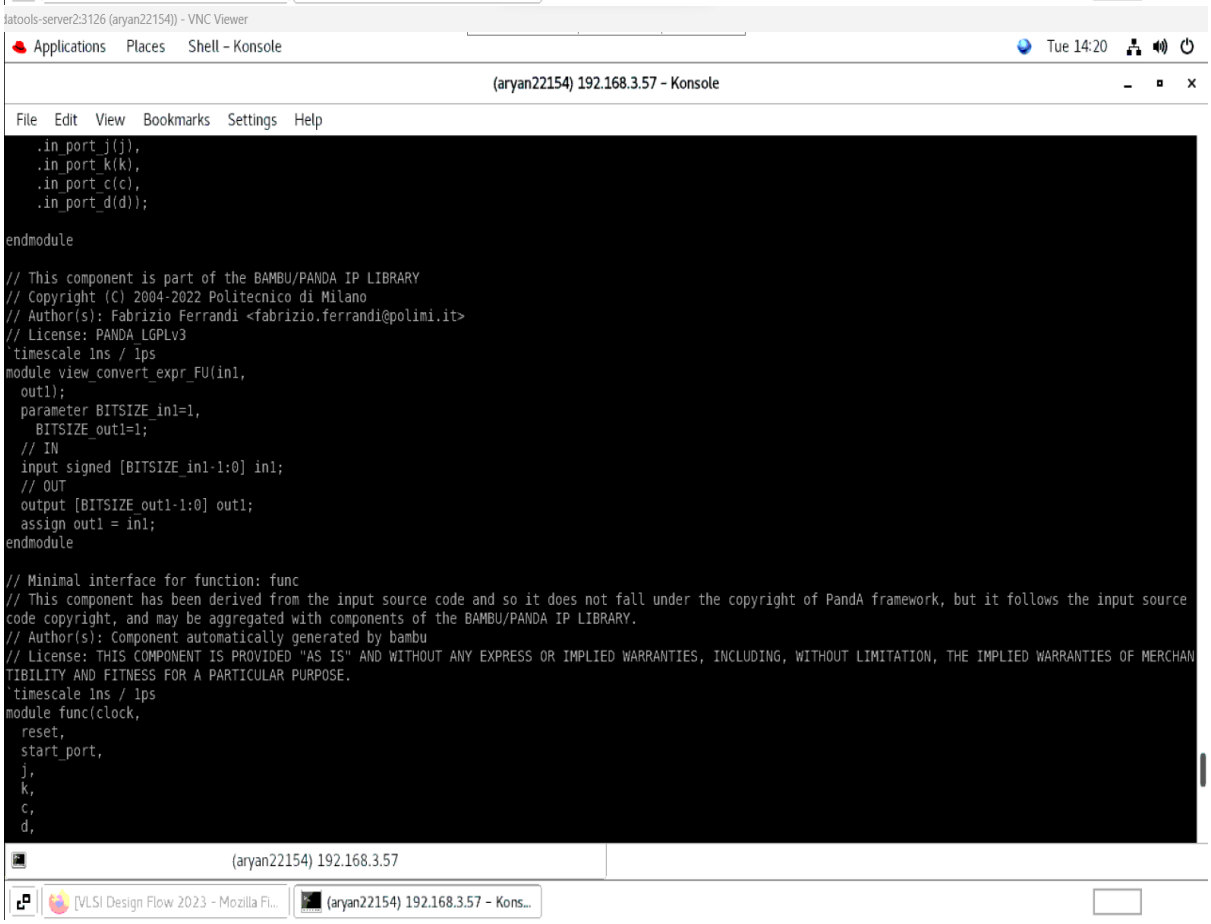
[VLSI Design Flow 2023 - Mozilla Fi...
(aryan22154) 192.168.3.57 – Kons...


/atools-server2:3126 (aryan22154)) - VNC Viewer
Applications Places Shell – Konsole
Tue 14:20
(aryan22154) 192.168.3.57 – Konsole
File Edit View Bookmarks Settings Help
.in_port_j(j),
.in_port_k(k),
.in_port_c(c),
.in_port_d(d));
endmodule
// This component is part of the BAMBU/PANDA IP LIBRARY
// Copyright (C) 2004-2022 Politecnico di Milano
// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
// License: PANDA_LGPLv3
`timescale 1ns / 1ps
module view_convert_expr_FU(in1,
out1);
parameter BITSIZE_in1=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
// OUT
output [BITSIZE_out1-1:0] out1;
assign out1 = in1;
endmodule
// Minimal interface for function: func
// This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows the input source code copyright, and may be aggregated with components of the BAMBU/PANDA IP LIBRARY.
// Author(s): Component automatically generated by bambu
// License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE.
`timescale 1ns / 1ps
module func(clock,
reset,
start_port,
j,
k,
c,
d,
(aryan22154) 192.168.3.57
[VLSI Design Flow 2023 - Mozilla Fi...
(aryan22154) 192.168.3.57 – Kons...

datools-server2:3126 (aryan22154)) - VNC Viewer

Applications Places Shell – Konsole

(aryan22154) 192.168.3.57 – Konsole

File Edit View Bookmarks Settings Help

```
  j,
  k,
  c,
  d,
  done_port,
  return_port);
  // IN
  input clock;
  input reset;
  input start_port;
  input [31:0] j;
  input [31:0] k;
  input [31:0] c;
  input [31:0] d;
  // OUT
  output done_port;
  output [31:0] return_port;
  // Component and signal declarations
  wire signed [31:0] out_return_port_view_convert_expr_FU;

  _func _func_i0 (.done_port(done_port),
    .return_port(out_return_port_view_convert_expr_FU),
    .clock(clock),
    .reset(reset),
    .start_port(start_port),
    .j(j),
    .k(k),
    .c(c),
    .d(d));
  view_convert_expr_FU #(.BITSIZE_in1(32),
    .BITSIZE_out1(32)) return_port_view_convert_expr_FU (.out1(return_port),
    .in1(out_return_port_view_convert_expr_FU));

endmodule
```

```
aryan22154@edaserver3:~/bambu$
```

(aryan22154) 192.168.3.57

[VLSI Design Flow 2023 - Mozilla Fi... (aryan22154) 192.168.3.57 – Kons...

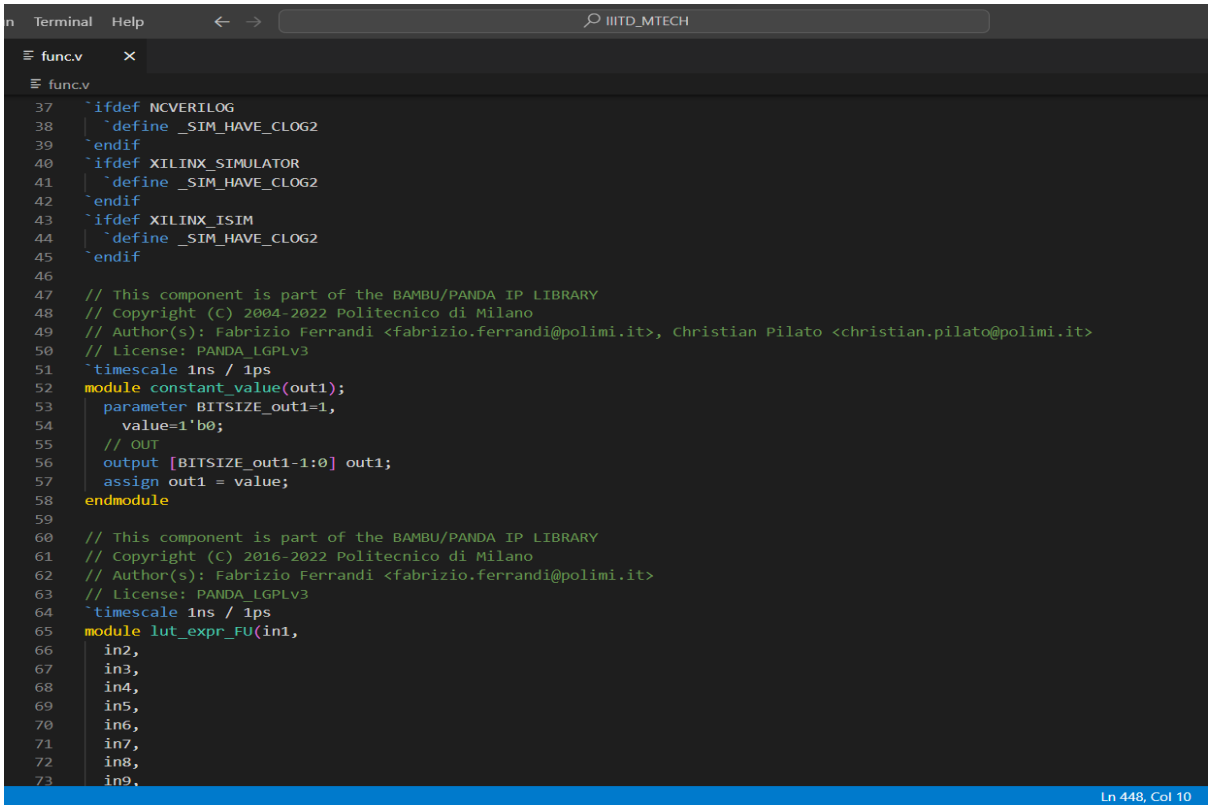
in Terminal Help IIITD_MTECH

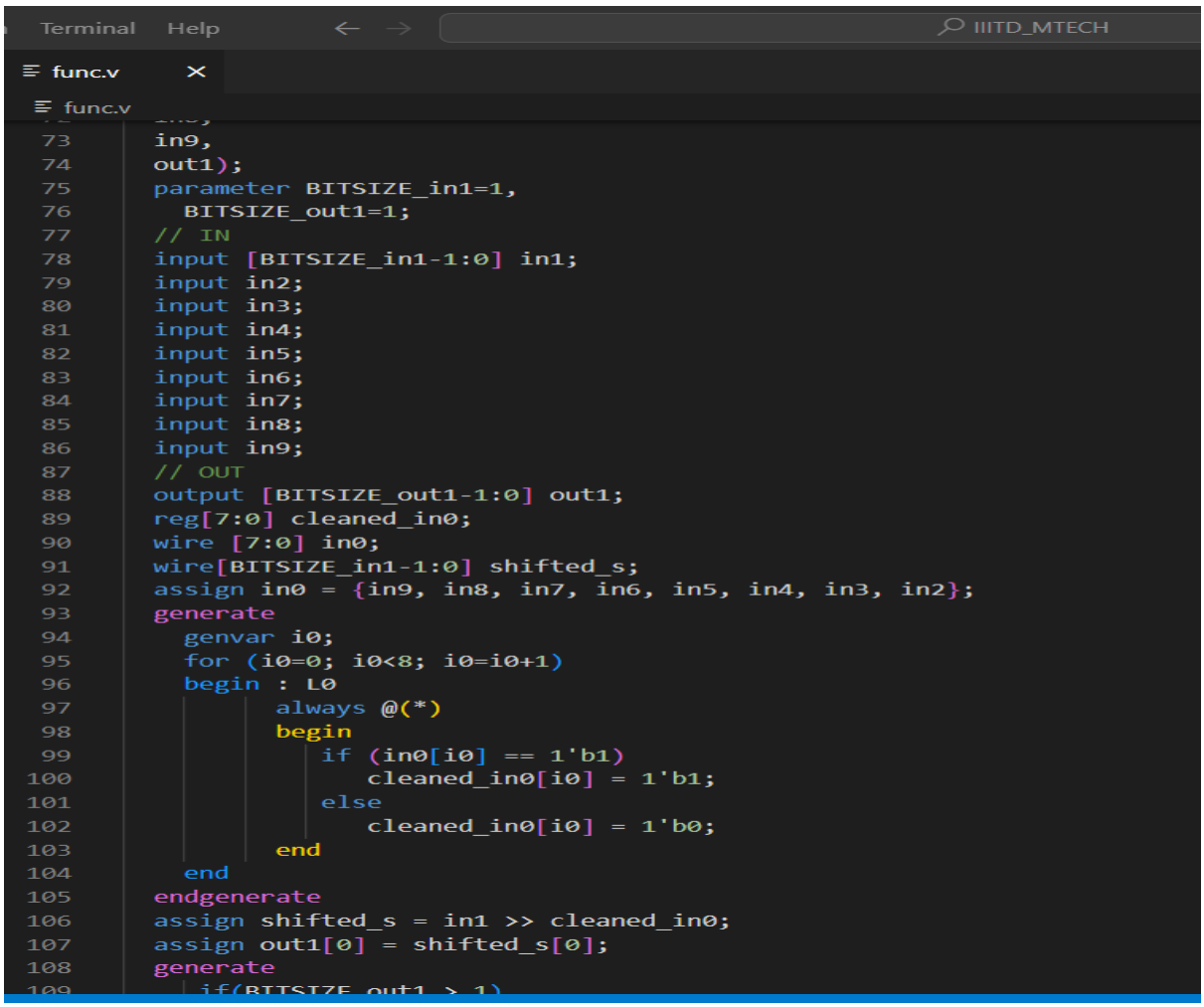
func.v

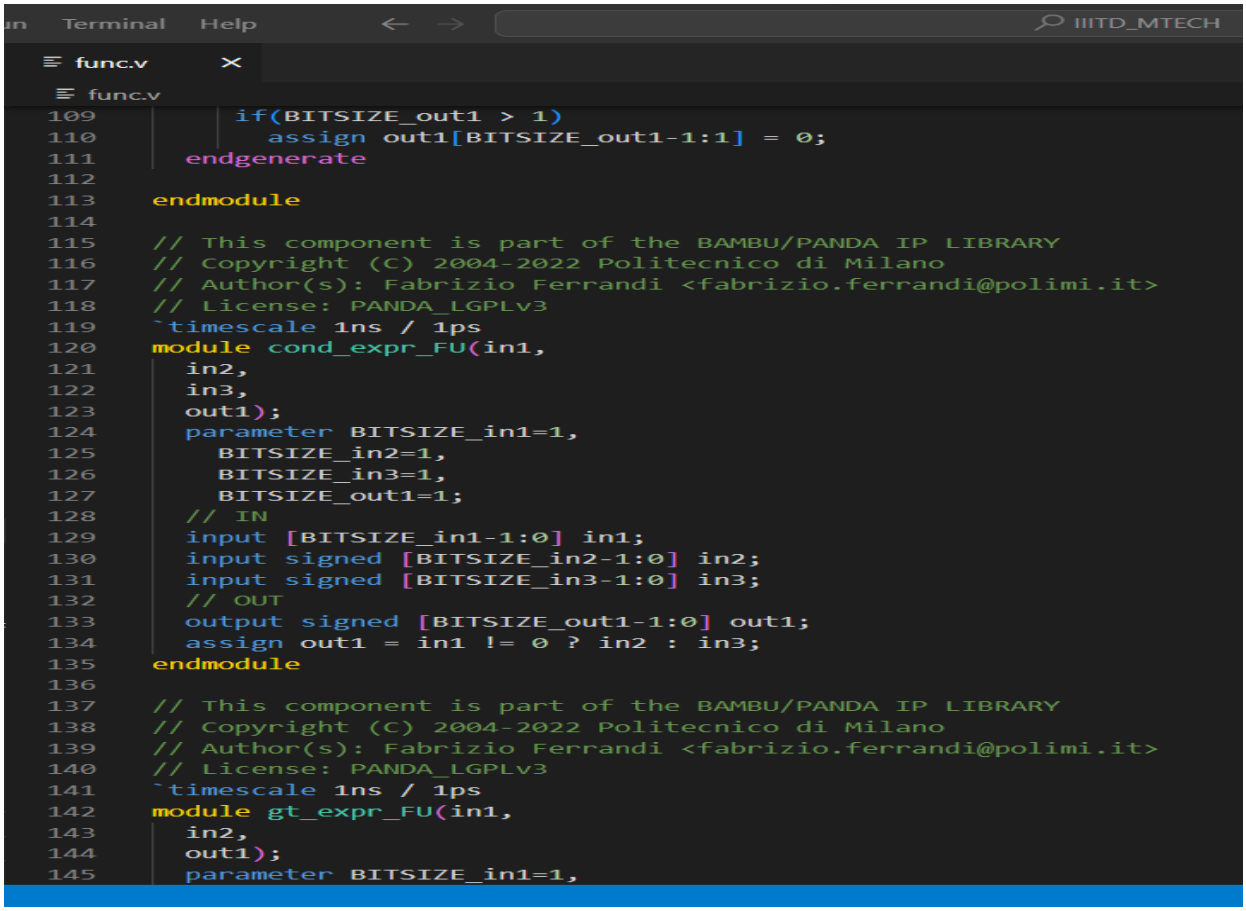
func.v

```
1   //
2   // Politecnico di Milano
3   // Code created using PandA - Version: PandA 0.9.7 - Revision 8b59b7ac7b9ab30cd20960921ab47ea5009163f1-main - Date 2023-02-07T14:33:39
4   // /tmp/.mount_bambu-0VIhYR/usr/bin/bambu executed with: /tmp/.mount_bambu-0VIhYR/usr/bin/bambu --top-fname=func a21.c
5   //
6   // Send any bug to: panda-info@polimi.it
7   // ******************************************************************************
8   // The following text holds for all the components tagged with PANDA_LGPLv3.
9   // They are all part of the BAMBU/PANDA IP LIBRARY.
10  // This library is free software; you can redistribute it and/or
11  // modify it under the terms of the GNU Lesser General Public
12  // License as published by the Free Software Foundation; either
13  // version 3 of the License, or (at your option) any later version.
14  //
15  // This library is distributed in the hope that it will be useful,
16  // but WITHOUT ANY WARRANTY; without even the implied warranty of
17  // MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE.  See the GNU
18  // Lesser General Public License for more details.
19  //
20  // You should have received a copy of the GNU Lesser General Public
21  // License along with the PandA framework; see the files COPYING.LIB
22  // If not, see <http://www.gnu.org/licenses/>.
23  // ******************************************************************************
24
25  `ifdef __ICARUS__
26  | `define _SIM_HAVE_CLOG2
27  `endif
28  `ifdef VERILATOR
29  | `define _SIM_HAVE_CLOG2
30  `endif
31  `ifdef MODEL_TECH
32  | `define _SIM_HAVE_CLOG2
33  `endif
34  `ifdef VCS
35  | `define _SIM_HAVE_CLOG2
36  `endif
37  `ifdef NCVERILOG
```

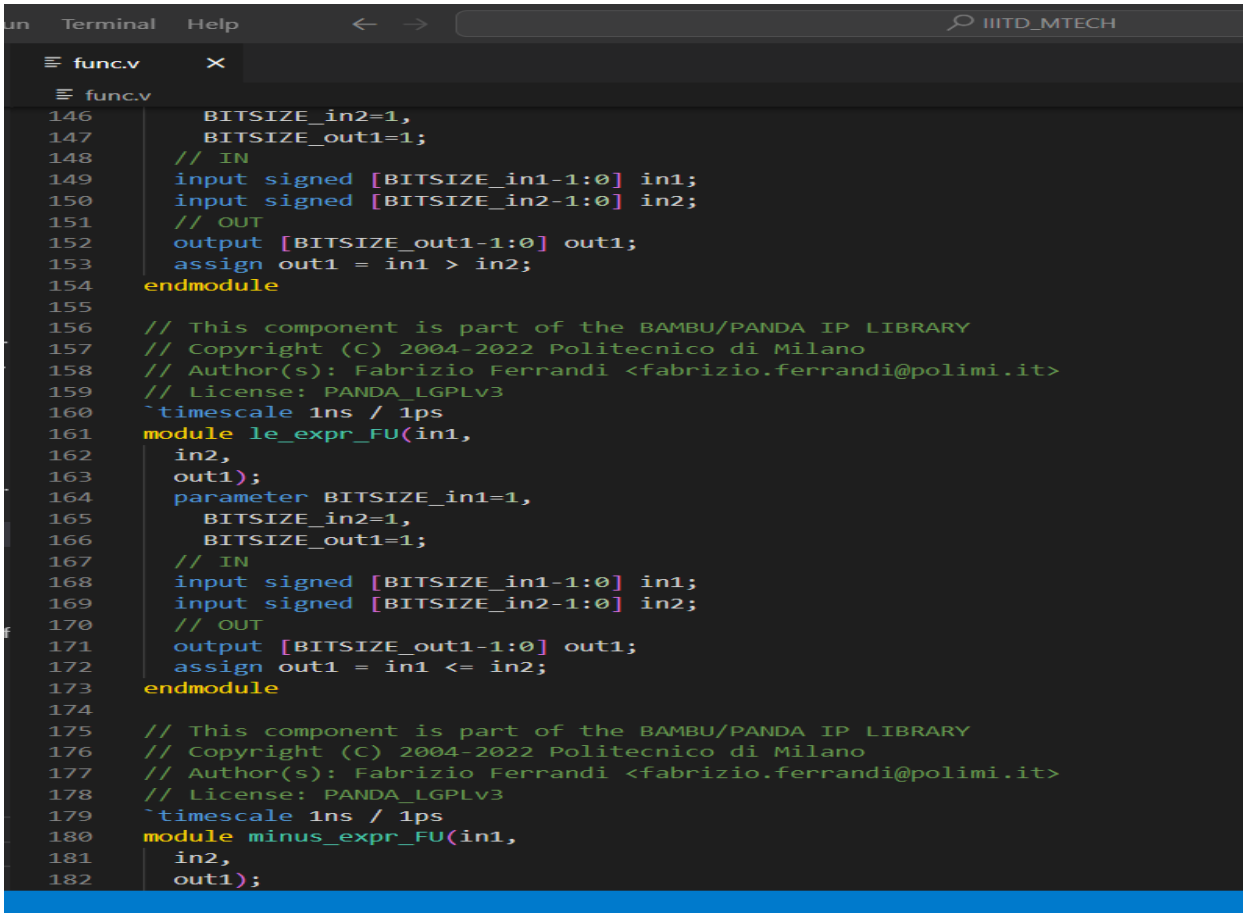
Ln 448, Col 10 Spaces: 4 UTF-8 CR


Terminal Help
IIITD_MTECH
func.v
func.v
`ifdef NCVERILOG
`define _SIM_HAVE_CLOG2
`endif
`ifdef XILINX_SIMULATOR
`define _SIM_HAVE_CLOG2
`endif
`ifdef XILINX_ISIM
`define _SIM_HAVE_CLOG2
`endif
// This component is part of the BAMBU/PANDA IP LIBRARY
// Copyright (C) 2004-2022 Politecnico di Milano
// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>, Christian Pilato <christian.pilato@polimi.it>
// License: PANDA_LGPLv3
`timescale 1ns / 1ps
module constant_value(out1);
parameter BITSIZE_out1=1,
value=1'b0;
// OUT
output [BITSIZE_out1-1:0] out1;
assign out1 = value;
endmodule
// This component is part of the BAMBU/PANDA IP LIBRARY
// Copyright (C) 2016-2022 Politecnico di Milano
// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
// License: PANDA_LGPLv3
`timescale 1ns / 1ps
module lut_expr_FU(in1,
in2,
in3,
in4,
in5,
in6,
in7,
in8,
in9,
Ln 448, Col 10

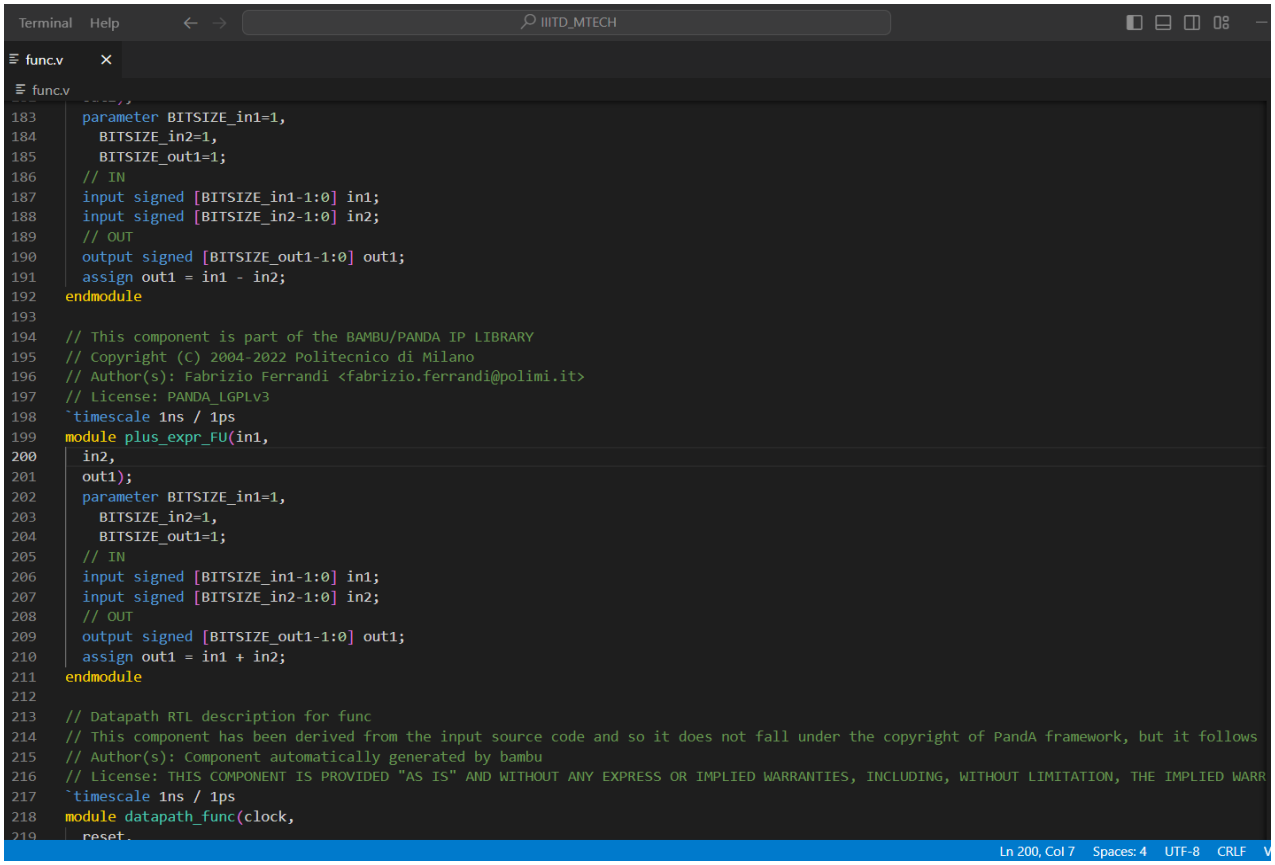

Terminal Help
IIITD_MTECH
func.v
func.v
in9,
out1);
parameter BITSIZE_in1=1,
BITSIZE_out1=1;
// IN
input [BITSIZE_in1-1:0] in1;
input in2;
input in3;
input in4;
input in5;
input in6;
input in7;
input in8;
input in9;
// OUT
output [BITSIZE_out1-1:0] out1;
reg[7:0] cleaned_in0;
wire [7:0] in0;
wire[BITSIZE_in1-1:0] shifted_s;
assign in0 = {in9, in8, in7, in6, in5, in4, in3, in2};
generate
genvar i0;
for (i0=0; i0<8; i0=i0+1)
begin : L0
always @(*)
begin
if (in0[i0] == 1'b1)
cleaned_in0[i0] = 1'b1;
else
cleaned_in0[i0] = 1'b0;
end
end
endgenerate
assign shifted_s = in1 >> cleaned_in0;
assign out1[0] = shifted_s[0];
generate



```
un  Terminal  Help                                   IIITD_MTECH
func.v
func.v
109         if(BITSIZE_out1 > 1)
110           assign out1[BITSIZE_out1-1:1] = 0;
111       endgenerate
112
113     endmodule
114
115     // This component is part of the BAMBU/PANDA IP LIBRARY
116     // Copyright (C) 2004-2022 Politecnico di Milano
117     // Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
118     // License: PANDA_LGPLv3
119     `timescale 1ns / 1ps
120     module cond_expr_FU(in1,
121       in2,
122       in3,
123       out1);
124       parameter BITSIZE_in1=1,
125         BITSIZE_in2=1,
126         BITSIZE_in3=1,
127         BITSIZE_out1=1;
128       // IN
129       input [BITSIZE_in1-1:0] in1;
130       input signed [BITSIZE_in2-1:0] in2;
131       input signed [BITSIZE_in3-1:0] in3;
132       // OUT
133       output signed [BITSIZE_out1-1:0] out1;
134       assign out1 = in1 != 0 ? in2 : in3;
135     endmodule
136
137     // This component is part of the BAMBU/PANDA IP LIBRARY
138     // Copyright (C) 2004-2022 Politecnico di Milano
139     // Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
140     // License: PANDA_LGPLv3
141     `timescale 1ns / 1ps
142     module gt_expr_FU(in1,
143       in2,
144       out1);
145       parameter BITSIZE_in1=1,
```



```
un  Terminal  Help                                   IIITD_MTECH
func.v
func.v
146         BITSIZE_in2=1,
147         BITSIZE_out1=1;
148       // IN
149       input signed [BITSIZE_in1-1:0] in1;
150       input signed [BITSIZE_in2-1:0] in2;
151       // OUT
152       output [BITSIZE_out1-1:0] out1;
153       assign out1 = in1 > in2;
154     endmodule
155
156     // This component is part of the BAMBU/PANDA IP LIBRARY
157     // Copyright (C) 2004-2022 Politecnico di Milano
158     // Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
159     // License: PANDA_LGPLv3
160     `timescale 1ns / 1ps
161     module le_expr_FU(in1,
162       in2,
163       out1);
164       parameter BITSIZE_in1=1,
165         BITSIZE_in2=1,
166         BITSIZE_out1=1;
167       // IN
168       input signed [BITSIZE_in1-1:0] in1;
169       input signed [BITSIZE_in2-1:0] in2;
170       // OUT
171       output [BITSIZE_out1-1:0] out1;
172       assign out1 = in1 <= in2;
173     endmodule
174
175     // This component is part of the BAMBU/PANDA IP LIBRARY
176     // Copyright (C) 2004-2022 Politecnico di Milano
177     // Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
178     // License: PANDA_LGPLv3
179     `timescale 1ns / 1ps
180     module minus_expr_FU(in1,
181       in2,
182       out1);
```


Terminal Help
IIITD_MTECH
func.v
func.v
parameter BITSIZE_in1=1,
BITSIZE_in2=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
input signed [BITSIZE_in2-1:0] in2;
// OUT
output signed [BITSIZE_out1-1:0] out1;
assign out1 = in1 - in2;
endmodule
// This component is part of the BAMBU/PANDA IP LIBRARY
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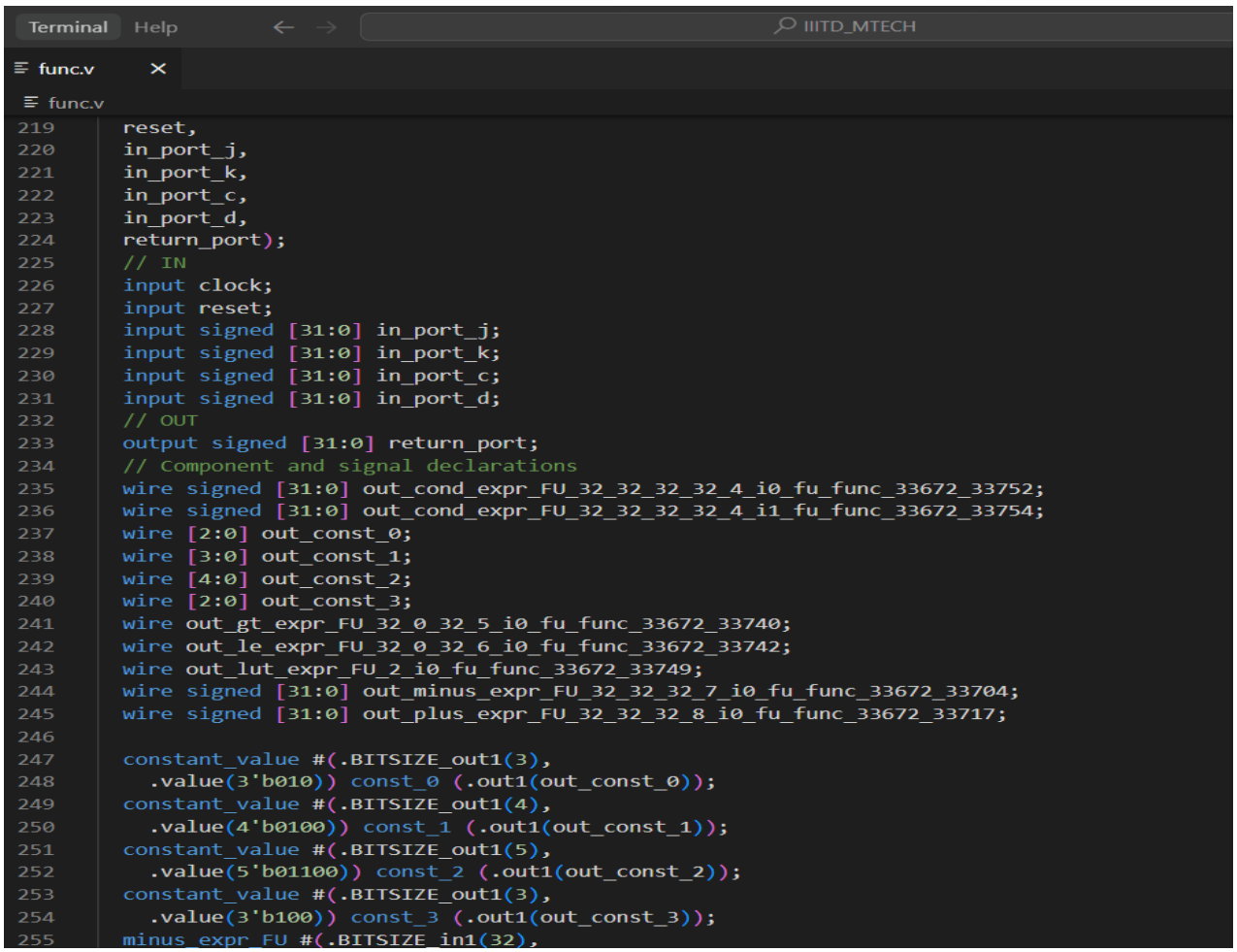
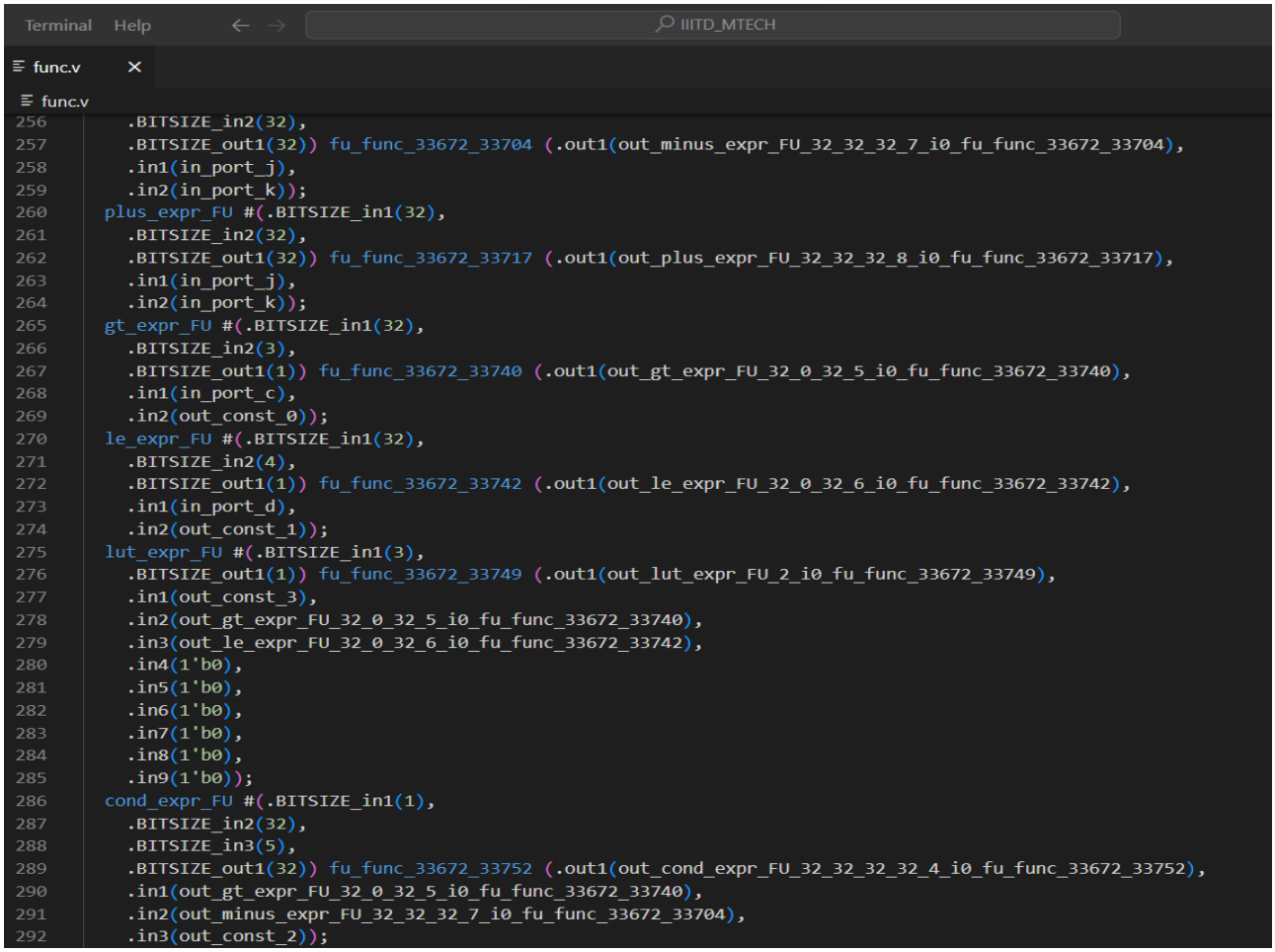
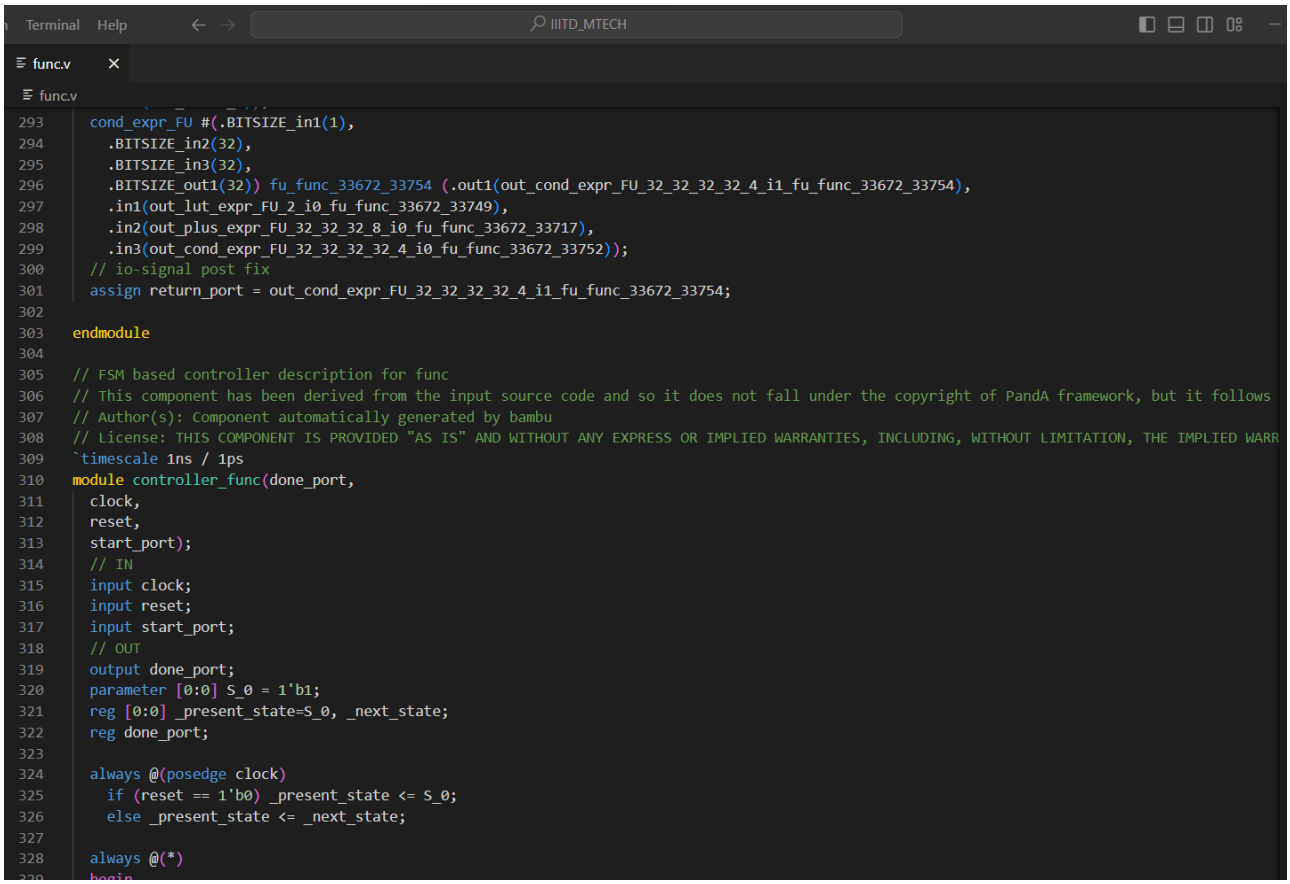
// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
// License: PANDA_LGPLv3
`timescale 1ns / 1ps
module plus_expr_FU(in1,
in2,
out1);
parameter BITSIZE_in1=1,
BITSIZE_in2=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
input signed [BITSIZE_in2-1:0] in2;
// OUT
output signed [BITSIZE_out1-1:0] out1;
assign out1 = in1 + in2;
endmodule
// Datapath RTL description for func
// This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows
// Author(s): Component automatically generated by bambu
// License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARR
`timescale 1ns / 1ps
module datapath_func(clock,
reset,
Ln 200, Col 7 Spaces: 4 UTF-8 CRLF

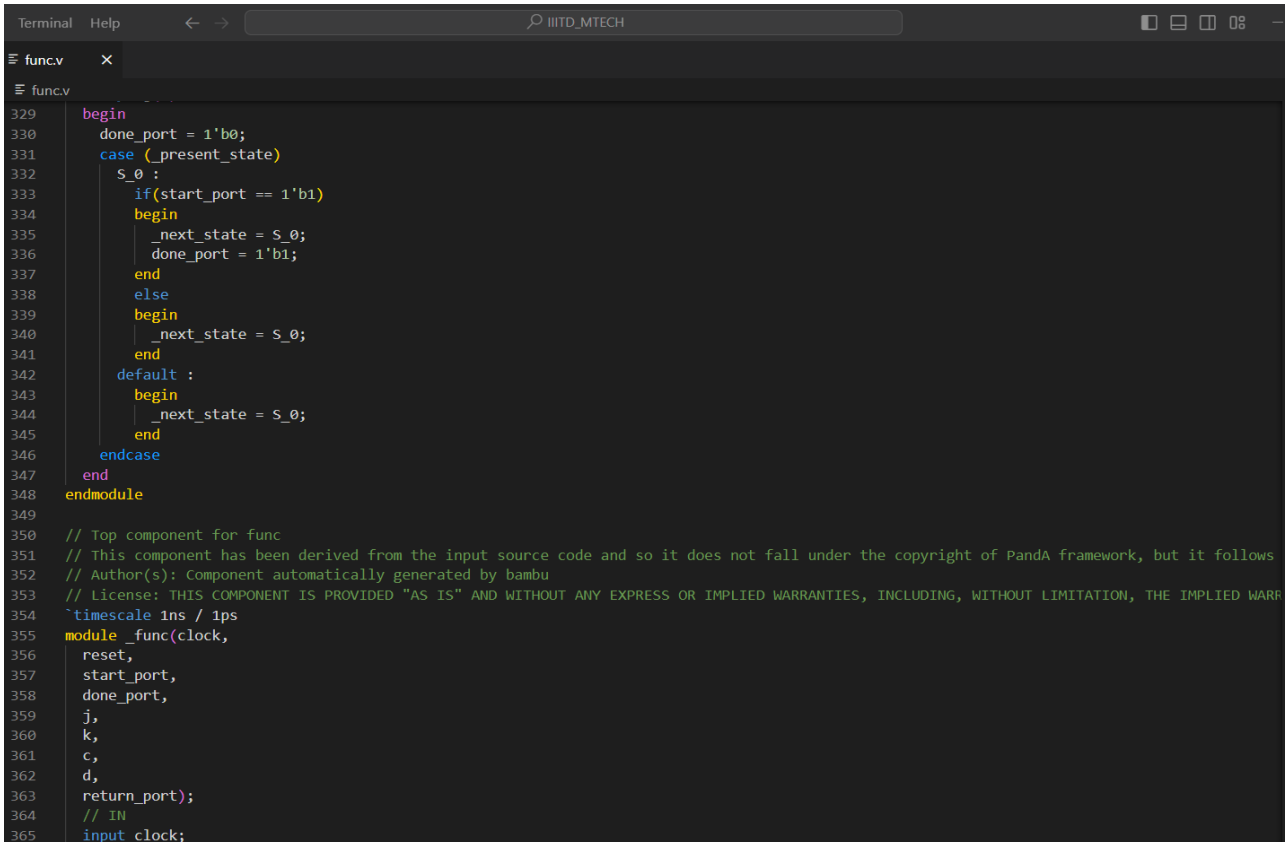

Terminal Help
IIITD_MTECH
func.v
func.v
reset,
in_port_j,
in_port_k,
in_port_c,
in_port_d,
return_port);
// IN
input clock;
input reset;
input signed [31:0] in_port_j;
input signed [31:0] in_port_k;
input signed [31:0] in_port_c;
input signed [31:0] in_port_d;
// OUT
output signed [31:0] return_port;
// Component and signal declarations
wire signed [31:0] out_cond_expr_FU_32_32_32_32_4_i0_fu_func_33672_33752;
wire signed [31:0] out_cond_expr_FU_32_32_32_32_4_i1_fu_func_33672_33754;
wire [2:0] out_const_0;
wire [3:0] out_const_1;
wire [4:0] out_const_2;
wire [2:0] out_const_3;
wire out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740;
wire out_le_expr_FU_32_0_32_6_i0_fu_func_33672_33742;
wire out_lut_expr_FU_2_i0_fu_func_33672_33749;
wire signed [31:0] out_minus_expr_FU_32_32_32_7_i0_fu_func_33672_33704;
wire signed [31:0] out_plus_expr_FU_32_32_32_8_i0_fu_func_33672_33717;
constant_value #(.BITSIZE_out1(3),
.value(3'b010)) const_0 (.out1(out_const_0));
constant_value #(.BITSIZE_out1(4),
.value(4'b0100)) const_1 (.out1(out_const_1));
constant_value #(.BITSIZE_out1(5),
.value(5'b01100)) const_2 (.out1(out_const_2));
constant_value #(.BITSIZE_out1(3),
.value(3'b100)) const_3 (.out1(out_const_3));
minus_expr_FU #(.BITSIZE_in1(32),

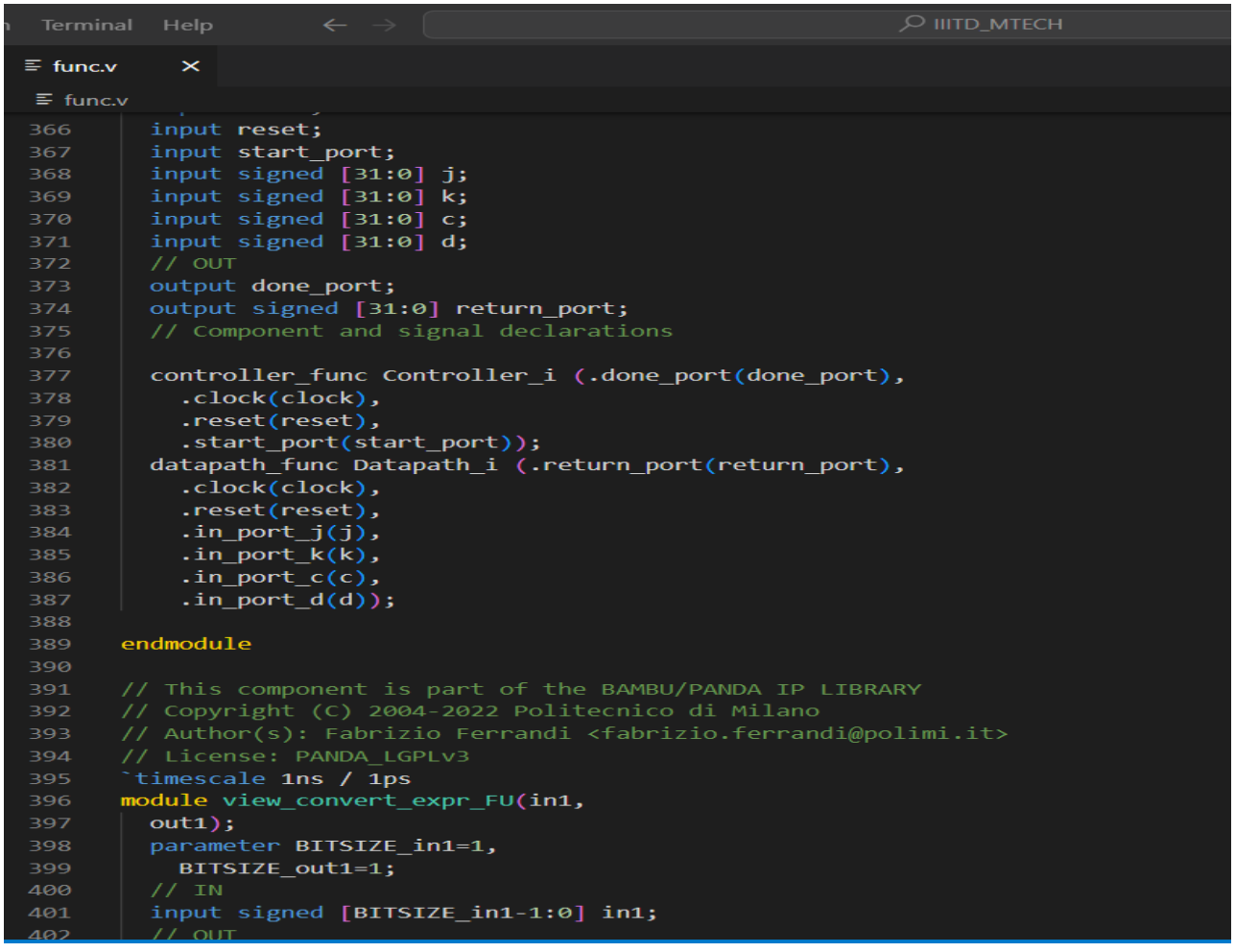


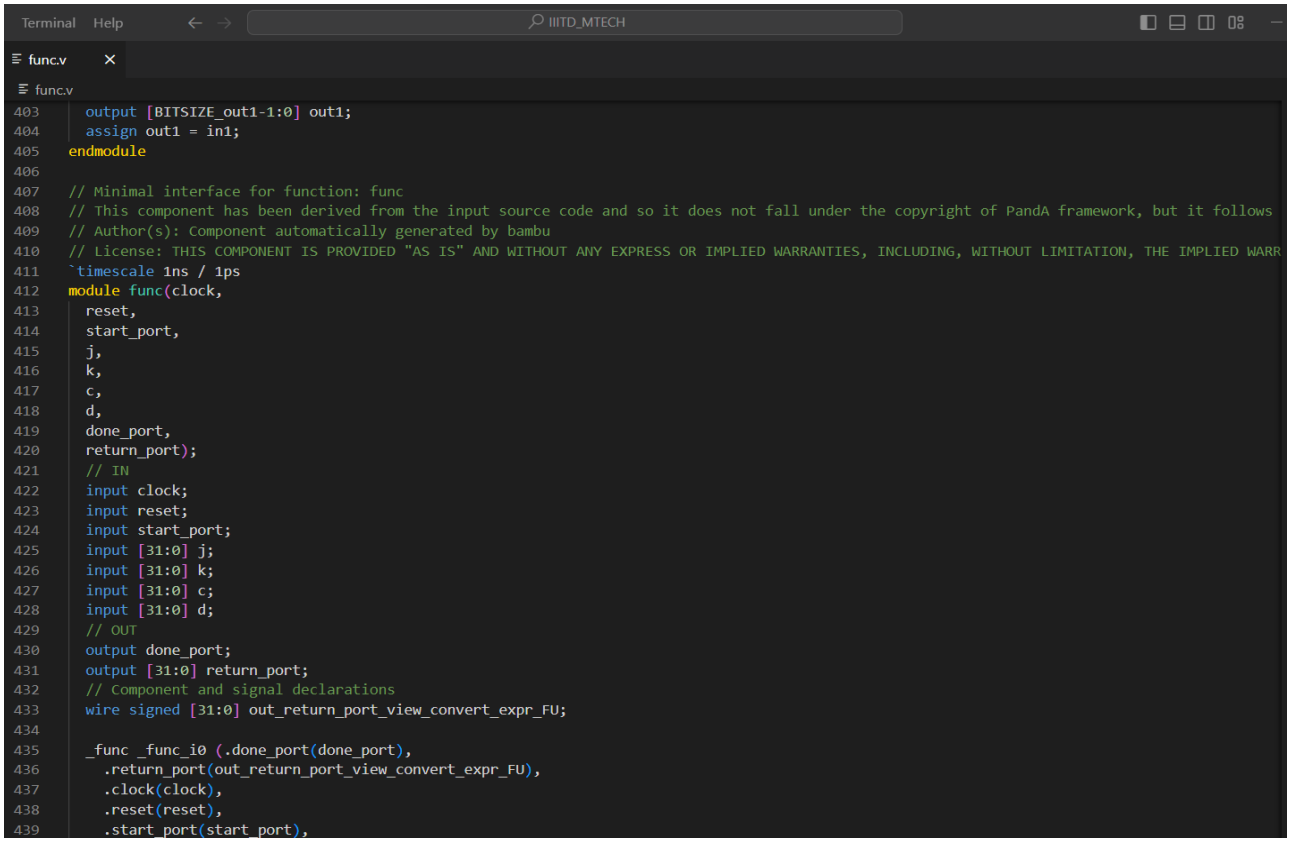
```
Terminal  Help  ← →  IIITD_MTECH
func.v
func.v
256       .BITSIZE_in2(32),
257       .BITSIZE_out1(32)) fu_func_33672_33704 (.out1(out_minus_expr_FU_32_32_32_7_i0_fu_func_33672_33704),
258       .in1(in_port_j),
259       .in2(in_port_k));
260     plus_expr_FU #(.BITSIZE_in1(32),
261       .BITSIZE_in2(32),
262       .BITSIZE_out1(32)) fu_func_33672_33717 (.out1(out_plus_expr_FU_32_32_32_8_i0_fu_func_33672_33717),
263       .in1(in_port_j),
264       .in2(in_port_k));
265     gt_expr_FU #(.BITSIZE_in1(32),
266       .BITSIZE_in2(3),
267       .BITSIZE_out1(1)) fu_func_33672_33740 (.out1(out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740),
268       .in1(in_port_c),
269       .in2(out_const_0));
270     le_expr_FU #(.BITSIZE_in1(32),
271       .BITSIZE_in2(4),
272       .BITSIZE_out1(1)) fu_func_33672_33742 (.out1(out_le_expr_FU_32_0_32_6_i0_fu_func_33672_33742),
273       .in1(in_port_d),
274       .in2(out_const_1));
275     lut_expr_FU #(.BITSIZE_in1(3),
276       .BITSIZE_out1(1)) fu_func_33672_33749 (.out1(out_lut_expr_FU_2_i0_fu_func_33672_33749),
277       .in1(out_const_3),
278       .in2(out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740),
279       .in3(out_le_expr_FU_32_0_32_6_i0_fu_func_33672_33742),
280       .in4(1'b0),
281       .in5(1'b0),
282       .in6(1'b0),
283       .in7(1'b0),
284       .in8(1'b0),
285       .in9(1'b0));
286     cond_expr_FU #(.BITSIZE_in1(1),
287       .BITSIZE_in2(32),
288       .BITSIZE_in3(5),
289       .BITSIZE_out1(32)) fu_func_33672_33752 (.out1(out_cond_expr_FU_32_32_32_32_4_i0_fu_func_33672_33752),
290       .in1(out_gt_expr_FU_32_0_32_5_i0_fu_func_33672_33740),
291       .in2(out_minus_expr_FU_32_32_32_7_i0_fu_func_33672_33704),
292       .in3(out_const_2));
```

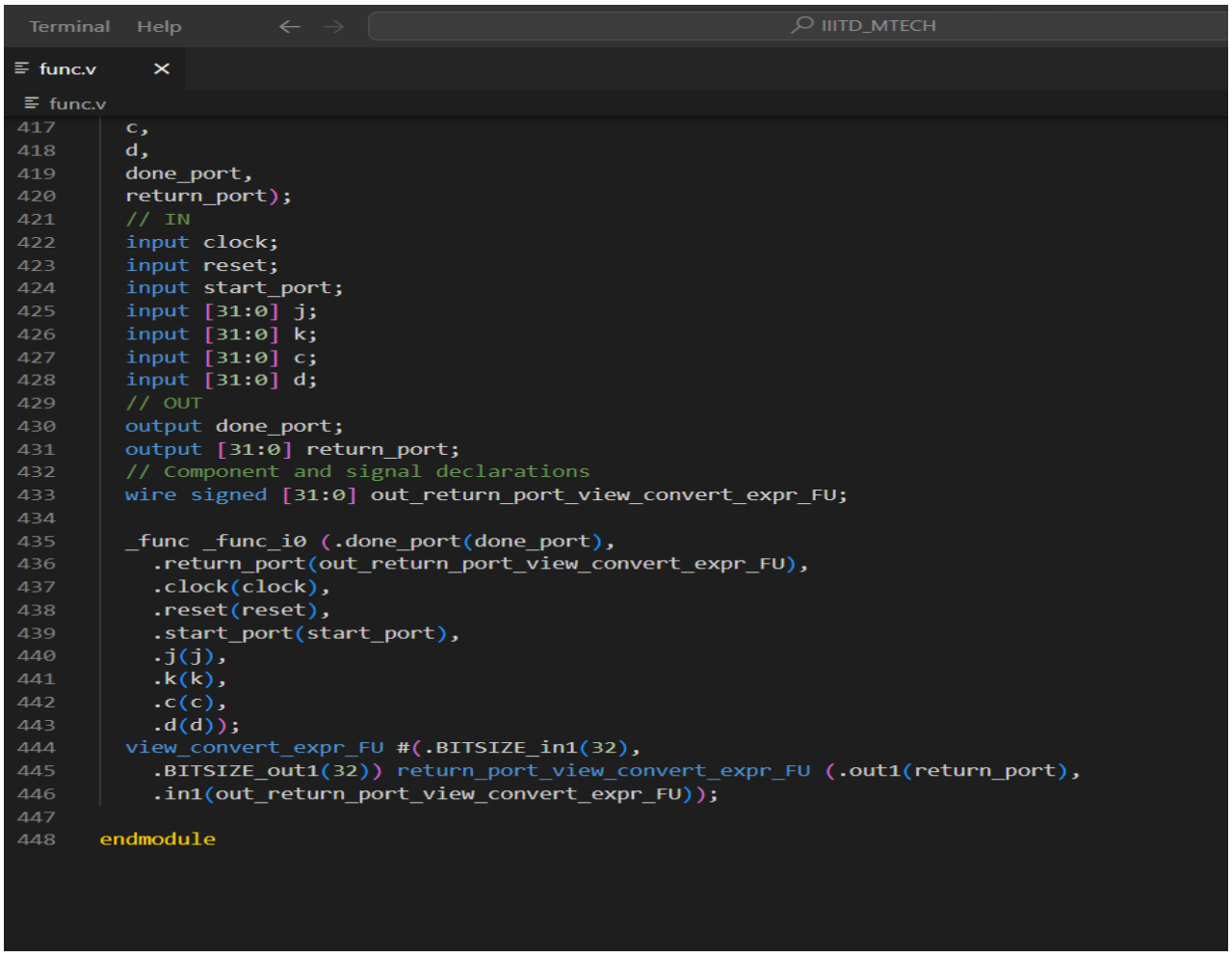


```
Terminal  Help  ← →  IIITD_MTECH
func.v
func.v
293     cond_expr_FU #(.BITSIZE_in1(1),
294       .BITSIZE_in2(32),
295       .BITSIZE_in3(32),
296       .BITSIZE_out1(32)) fu_func_33672_33754 (.out1(out_cond_expr_FU_32_32_32_32_4_i1_fu_func_33672_33754),
297       .in1(out_lut_expr_FU_2_i0_fu_func_33672_33749),
298       .in2(out_plus_expr_FU_32_32_32_8_i0_fu_func_33672_33717),
299       .in3(out_cond_expr_FU_32_32_32_32_4_i0_fu_func_33672_33752));
300     // io-signal post fix
301     assign return_port = out_cond_expr_FU_32_32_32_32_4_i1_fu_func_33672_33754;
302
303   endmodule
304
305   // FSM based controller description for func
306   // This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows
307   // Author(s): Component automatically generated by bambu
308   // License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARR
309   `timescale 1ns / 1ps
310   module controller_func(done_port,
311     clock,
312     reset,
313     start_port);
314     // IN
315     input clock;
316     input reset;
317     input start_port;
318     // OUT
319     output done_port;
320     parameter [0:0] S_0 = 1'b1;
321     reg [0:0] _present_state=S_0, _next_state;
322     reg done_port;
323
324     always @(posedge clock)
325       if (reset == 1'b0) _present_state <= S_0;
326       else _present_state <= _next_state;
327
328     always @(*)
```


Terminal Help
IIITD_MTECH
func.v
func.v
begin
done_port = 1'b0;
case (_present_state)
S_0 :
if(start_port == 1'b1)
begin
_next_state = S_0;
done_port = 1'b1;
end
else
begin
_next_state = S_0;
end
default :
begin
_next_state = S_0;
end
endcase
end
endmodule
// Top component for func
// This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows
// Author(s): Component automatically generated by bambu
// License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARR
`timescale 1ns / 1ps
module _func(clock,
reset,
start_port,
done_port,
j,
k,
c,
d,
return_port);
// IN
input clock;


Terminal Help
IIITD_MTECH
func.v
func.v
input reset;
input start_port;
input signed [31:0] j;
input signed [31:0] k;
input signed [31:0] c;
input signed [31:0] d;
// OUT
output done_port;
output signed [31:0] return_port;
// Component and signal declarations
controller_func Controller_i (.done_port(done_port),
.clock(clock),
.reset(reset),
.start_port(start_port));
datapath_func Datapath_i (.return_port(return_port),
.clock(clock),
.reset(reset),
.in_port_j(j),
.in_port_k(k),
.in_port_c(c),
.in_port_d(d));
endmodule
// This component is part of the BAMBU/PANDA IP LIBRARY
// Copyright (C) 2004-2022 Politecnico di Milano
// Author(s): Fabrizio Ferrandi <fabrizio.ferrandi@polimi.it>
// License: PANDA_LGPLv3
`timescale 1ns / 1ps
module view_convert_expr_FU(in1,
out1);
parameter BITSIZE_in1=1,
BITSIZE_out1=1;
// IN
input signed [BITSIZE_in1-1:0] in1;
// OUT


Terminal Help
IIITD_MTECH
func.v
func.v
403 output [BITSIZE_out1-1:0] out1;
404 assign out1 = in1;
405 endmodule
406
407 // Minimal interface for function: func
408 // This component has been derived from the input source code and so it does not fall under the copyright of PandA framework, but it follows
409 // Author(s): Component automatically generated by bambu
410 // License: THIS COMPONENT IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARR
411 `timescale 1ns / 1ps
412 module func(clock,
413 reset,
414 start_port,
415 j,
416 k,
417 c,
418 d,
419 done_port,
420 return_port);
421 // IN
422 input clock;
423 input reset;
424 input start_port;
425 input [31:0] j;
426 input [31:0] k;
427 input [31:0] c;
428 input [31:0] d;
429 // OUT
430 output done_port;
431 output [31:0] return_port;
432 // Component and signal declarations
433 wire signed [31:0] out_return_port_view_convert_expr_FU;
434
435 _func _func_i0 (.done_port(done_port),
436 .return_port(out_return_port_view_convert_expr_FU),
437 .clock(clock),
438 .reset(reset),
439 .start_port(start_port),


Terminal Help
IIITD_MTECH
func.v
func.v
417 c,
418 d,
419 done_port,
420 return_port);
421 // IN
422 input clock;
423 input reset;
424 input start_port;
425 input [31:0] j;
426 input [31:0] k;
427 input [31:0] c;
428 input [31:0] d;
429 // OUT
430 output done_port;
431 output [31:0] return_port;
432 // Component and signal declarations
433 wire signed [31:0] out_return_port_view_convert_expr_FU;
434
435 _func _func_i0 (.done_port(done_port),
436 .return_port(out_return_port_view_convert_expr_FU),
437 .clock(clock),
438 .reset(reset),
439 .start_port(start_port),
440 .j(j),
441 .k(k),
442 .c(c),
443 .d(d));
444 view_convert_expr_FU #(.BITSIZE_in1(32),
445 .BITSIZE_out1(32)) return_port_view_convert_expr_FU (.out1(return_port),
446 .in1(out_return_port_view_convert_expr_FU));
447
448 endmodule

Q3) - Explain the role of each module in the generated RTL.

The FSM here contains a single state S_0=1'b1.

And if the reset =1'b0, then the _present_state<=S_0. Otherwise, the _present_state<=next_state.

Initially, the done_port=1'b0.

```
case (_present_state)
      S_0 :
        if(start_port == 1'b1)
        begin
          _next_state = S_0;
          done_port = 1'b1;
        end
        else
        begin
          _next_state = S_0;
        end
      default :
        begin
          _next_state = S_0;
        end
    endcase
```

Top module: _func → data path →Controller → helper modules to operate.

1)- module constant_value () – This component is part of the BAMBU/PANDA IP LIBRARY. it generates the constant value with a size of [BITSIZE_out1-1:0].

2)- module lut_expr_FU () – This component is part of the BAMBU/PANDA IP LIBRARY. This module takes the 9 inputs and gives the 1 output. The output depends on the following factors using the loop and the output is the shifted + several values. (If the BITSIZE_out1 >1).

3)- module cond_expr_FU () – This component is part of the BAMBU/PANDA IP LIBRARY. This component is part of the BAMBU/PANDA IP LIBRARY. This module performs the conditional operation.

assign out1 = in1! = 0? in2: in3.

4)- module gt_expr_FU () – This component is part of the BAMBU/PANDA IP LIBRARY. This module performs the greater operation.

assign out1 = in1 > in2.

5)- module le_expr_FU () – This component is part of the BAMBU/PANDA IP LIBRARY. This is the module assign out1 = in1 <= in2.

6)- module minus_expr_FU () – This component is part of the BAMBU/PANDA IP LIBRARY. This module performs the minus operation between two inputs. assign out1 = in1 - in2.

7)- module plus_expr_FU () – This component is part of the BAMBU/PANDA IP LIBRARY. This module performs the plus operation between two inputs. Assign out1 = in1 + in2.

8)- module datapath_func () –Datapath RTL description for func.This module calls the other function with the parameters and is responsible for handling the Datapath of func function of c.

9)- module controller_func () – This module deals with the FSM based controller description for func.

10)- module _func () –Top component for func.

11)- module view_convert_expr_FU () – This component is part of the BAMBU/PANDA IP LIBRARY.To view the convert, assign out1 = in1.

12)- module func() - Minimal interface for function: func.

Q4) - Explain how + and – are computed in the data path in the generated Verilog model.

The module plus_expr_FU and module minus_expr_FU perform the + and the – operation in the Verilog model.

Plus_expr_FU - assign out1 = in1 + in2.

Minus_expr_FU - assign out1 = in1 - in2.

So, now let's take an example from the code in the datapath

```
minus_expr_FU #(.BITSIZE_in1(32),
    .BITSIZE_in2(32),
    .BITSIZE_out1(32)) fu_func_33672_33704
(.out1(out_minus_expr_FU_32_32_32_7_i0_fu_func_33672_33704),
    .in1(in_port_j),
    .in2(in_port_k));
  plus_expr_FU #(.BITSIZE_in1(32),
    .BITSIZE_in2(32),
    .BITSIZE_out1(32)) fu_func_33672_33717
(.out1(out_plus_expr_FU_32_32_32_8_i0_fu_func_33672_33717),
    .in1(in_port_j),
    .in2(in_port_k));
```

This is the code snippet of the datapath in the module.

So, the data path will call these modules when + and – are needed to perform with the parameters.