

CS224

Section No.: 1

Spring 2021

Lab No.: 6

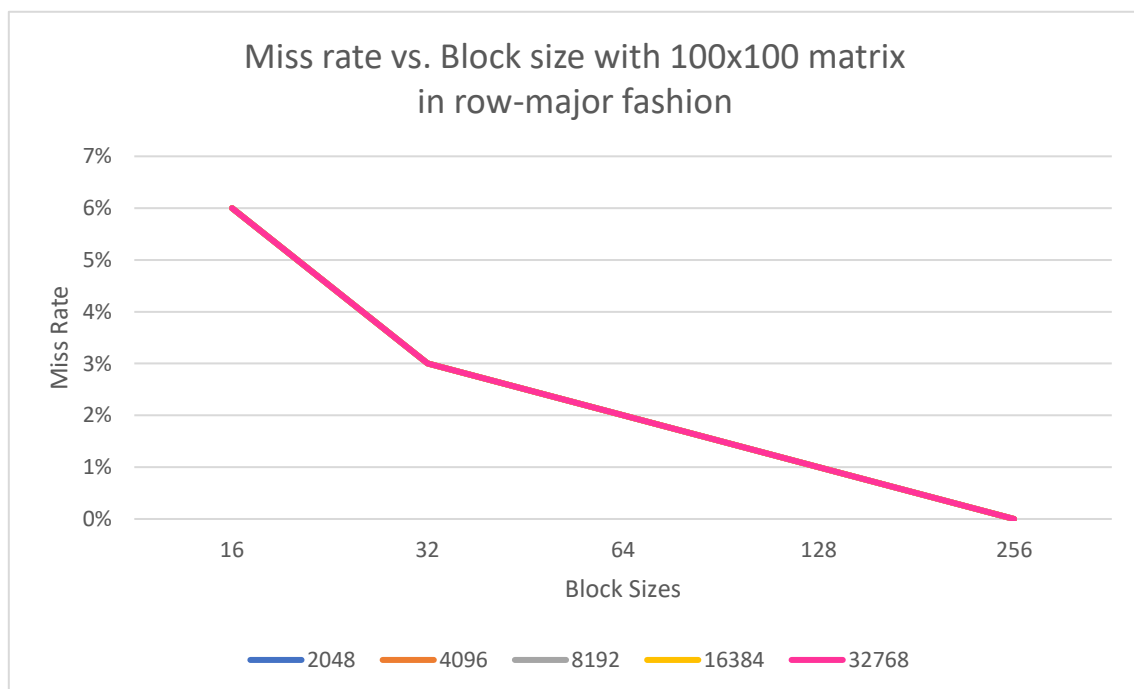
Full Name/Bilkent ID: Ata Seren/21901575

Lab Work Report

Part 2.a:

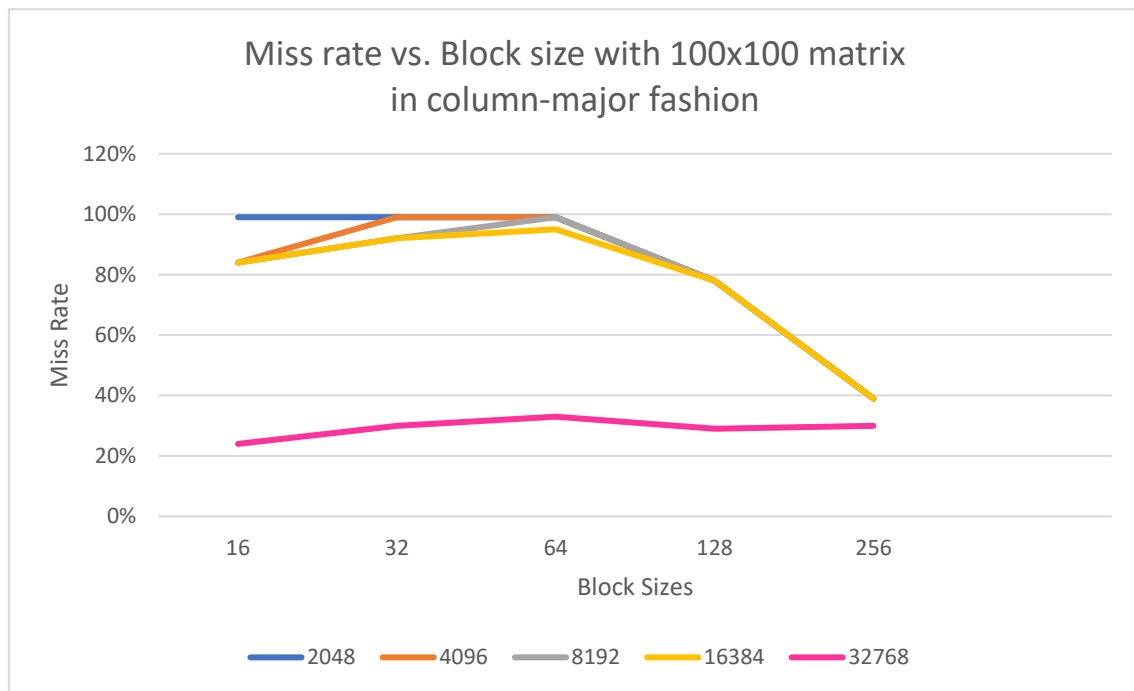
Row-major average for 100x100 matrix:

| | Block size | | | | |
|------------|-----------------------------------|-----------------------------------|-----------------------------------|----------------------------------|----------------------------------|
| Cache size | 16 | 32 | 64 | 128 | 256 |
| 2048 | Miss rate: %6 # of misses: 630 | Miss rate: %3 # of misses: 317 | Miss rate: %2 # of misses: 159 | Miss rate: %1 # of misses: 80 | Miss rate: %0 # of misses: 41 |
| 4096 | Miss rate: %6 # of misses: 630 | Miss rate: %3 # of misses: 317 | Miss rate: %2 # of misses: 159 | Miss rate: %1 # of misses: 80 | Miss rate: %0 # of misses: 41 |
| 8192 | Miss rate: %6 # of misses: 630 | Miss rate: %3 # of misses: 317 | Miss rate: %2 # of misses: 159 | Miss rate: %1 # of misses: 80 | Miss rate: %0 # of misses: 41 |
| 16384 | Miss rate: %6 # of misses: 630 | Miss rate: %3 # of misses: 317 | Miss rate: %2 # of misses: 159 | Miss rate: %1 # of misses: 80 | Miss rate: %0 # of misses: 41 |
| 32768 | Miss rate: %6 # of misses: 630 | Miss rate: %3 # of misses: 317 | Miss rate: %2 # of misses: 159 | Miss rate: %1 # of misses: 80 | Miss rate: %0 # of misses: 41 |



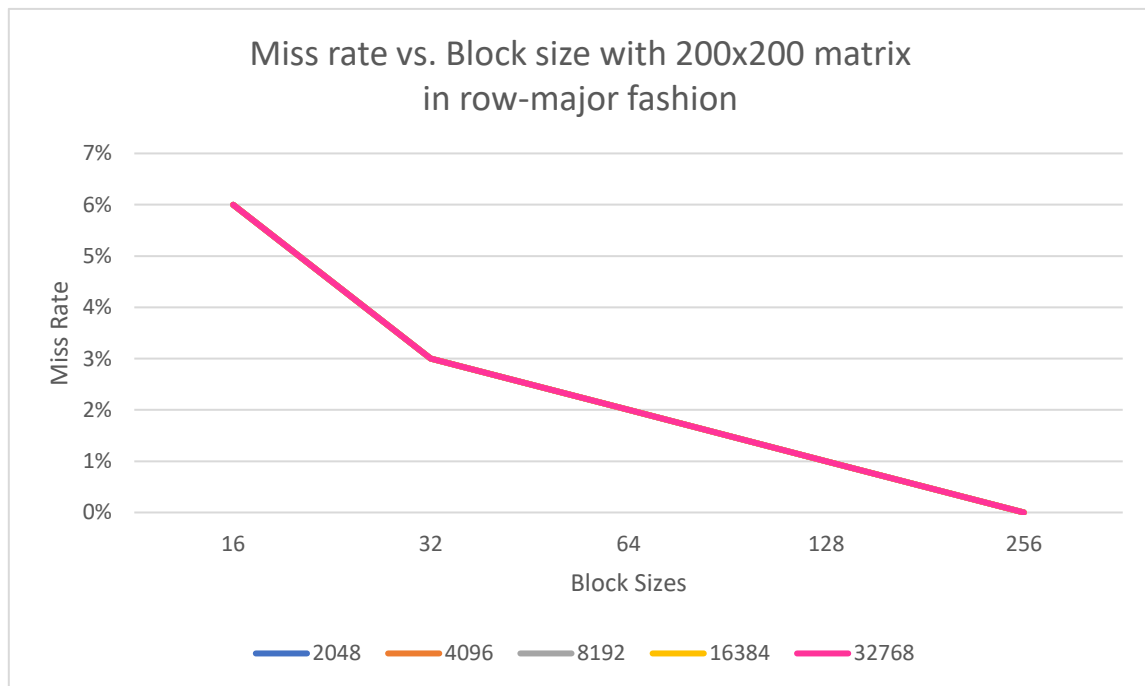
Column-major average for 100x100 matrix:

| | Block size | | | | |
|------------|--------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|-------------------------------------|
| Cache size | 16 | 32 | 64 | 128 | 256 |
| 2048 | Miss rate: %99 # of misses: 10004 | Miss rate: %99 # of misses: 10003 | Miss rate: %99 # of misses: 10002 | Miss rate: %78 # of misses: 7817 | Miss rate: %39 # of misses: 3917 |
| 4096 | Miss rate: %84 # of misses: 8468 | Miss rate: %99 # of misses: 10003 | Miss rate: %99 # of misses: 10002 | Miss rate: %78 # of misses: 7817 | Miss rate: %39 # of misses: 3917 |
| 8192 | Miss rate: %84 # of misses: 8468 | Miss rate: %92 # of misses: 9235 | Miss rate: %99 # of misses: 10002 | Miss rate: %78 # of misses: 7817 | Miss rate: %39 # of misses: 3917 |
| 16384 | Miss rate: %84 # of misses: 8468 | Miss rate: %92 # of misses: 9235 | Miss rate: %95 # of misses: 9618 | Miss rate: %78 # of misses: 7817 | Miss rate: %39 # of misses: 3917 |
| 32768 | Miss rate: %24 # of misses: 2445 | Miss rate: %30 # of misses: 3024 | Miss rate: %33 # of misses: 3313 | Miss rate: %29 # of misses: 2882 | Miss rate: %14 # of misses: 1457 |



Row-major average for 200x200 matrix:

| Cache size | Block size | | | | |
|------------|------------------------------------|------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| | 16 | 32 | 64 | 128 | 256 |
| 2048 | Miss rate: %6 # of misses: 2505 | Miss rate: %3 # of misses: 1254 | Miss rate: %2 # of misses: 627 | Miss rate: %1 # of misses: 314 | Miss rate: %0 # of misses: 158 |
| 4096 | Miss rate: %6 # of misses: 2505 | Miss rate: %3 # of misses: 1254 | Miss rate: %2 # of misses: 627 | Miss rate: %1 # of misses: 314 | Miss rate: %0 # of misses: 158 |
| 8192 | Miss rate: %6 # of misses: 2505 | Miss rate: %3 # of misses: 1254 | Miss rate: %2 # of misses: 627 | Miss rate: %1 # of misses: 314 | Miss rate: %0 # of misses: 158 |
| 16384 | Miss rate: %6 # of misses: 2505 | Miss rate: %3 # of misses: 1254 | Miss rate: %2 # of misses: 627 | Miss rate: %1 # of misses: 314 | Miss rate: %0 # of misses: 158 |
| 32768 | Miss rate: %6 # of misses: 2505 | Miss rate: %3 # of misses: 1254 | Miss rate: %2 # of misses: 627 | Miss rate: %1 # of misses: 314 | Miss rate: %0 # of misses: 158 |



Column-major average for 200x200 matrix:

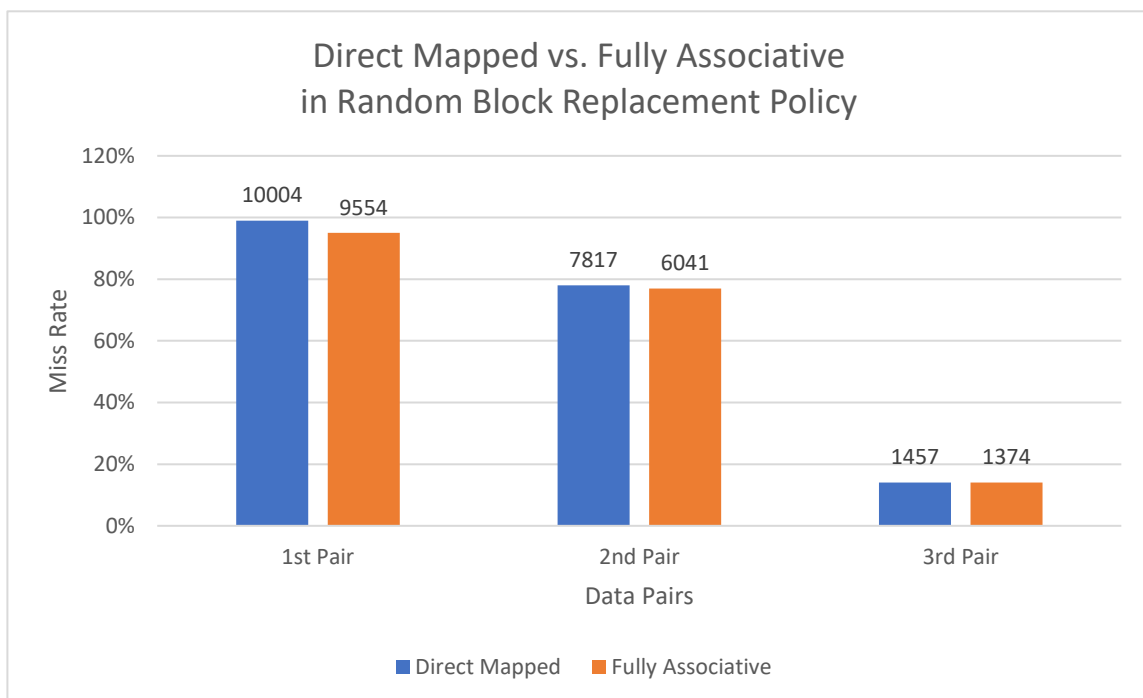
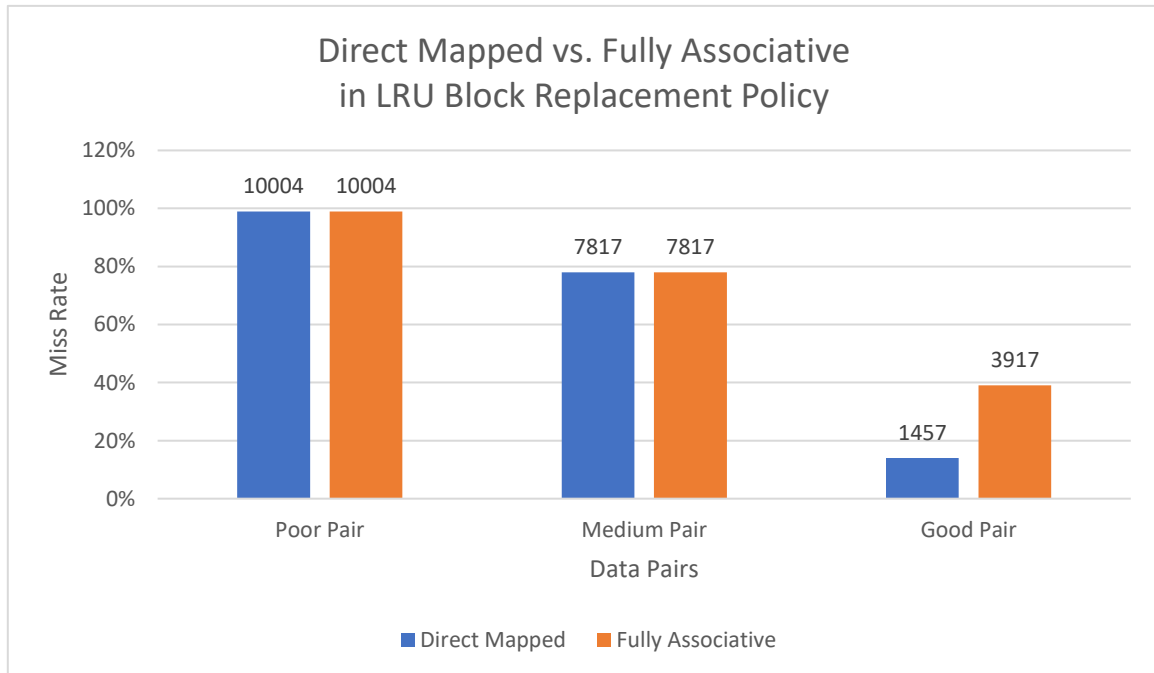
| | Block size | | | | |
|------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|--------------------------------------|
| Cache size | 16 | 32 | 64 | 128 | 256 |
| 2048 | Miss rate: %100 # of misses: 40004 | Miss rate: %100 # of misses: 40003 | Miss rate: %100 # of misses: 40002 | Miss rate: %100 # of misses: 40001 | Miss rate: %78 # of misses: 31265 |
| 4096 | Miss rate: %100 # of misses: 40002 | Miss rate: %100 # of misses: 40003 | Miss rate: %100 # of misses: 40002 | Miss rate: %100 # of misses: 40001 | Miss rate: %78 # of misses: 31265 |
| 8192 | Miss rate: %82 # of misses: 32836 | Miss rate: %100 # of misses: 40002 | Miss rate: %100 # of misses: 40002 | Miss rate: %100 # of misses: 40001 | Miss rate: %78 # of misses: 31265 |
| 16384 | Miss rate: %82 # of misses: 32836 | Miss rate: %91 # of misses: 36419 | Miss rate: %95 # of misses: 38210 | Miss rate: %100 # of misses: 40001 | Miss rate: %78 # of misses: 31265 |
| 32768 | Miss rate: %82 # of misses: 32836 | Miss rate: %91 # of misses: 36419 | Miss rate: %95 # of misses: 38210 | Miss rate: %98 # of misses: 39105 | Miss rate: %78 # of misses: 31265 |



Part 2.b

I got my data from 100x100 matrix column-major results which are:

| Pair No. | 1 (Poor) | 2 (Medium) | 3 (Good) |
|-------------|----------|------------|----------|
| Block Size | 16 | 128 | 256 |
| Cache Size | 2048 | 8192 | 32768 |
| Miss Rate | %99 | %78 | %14 |
| # of Misses | 10004 | 7817 | 1457 |

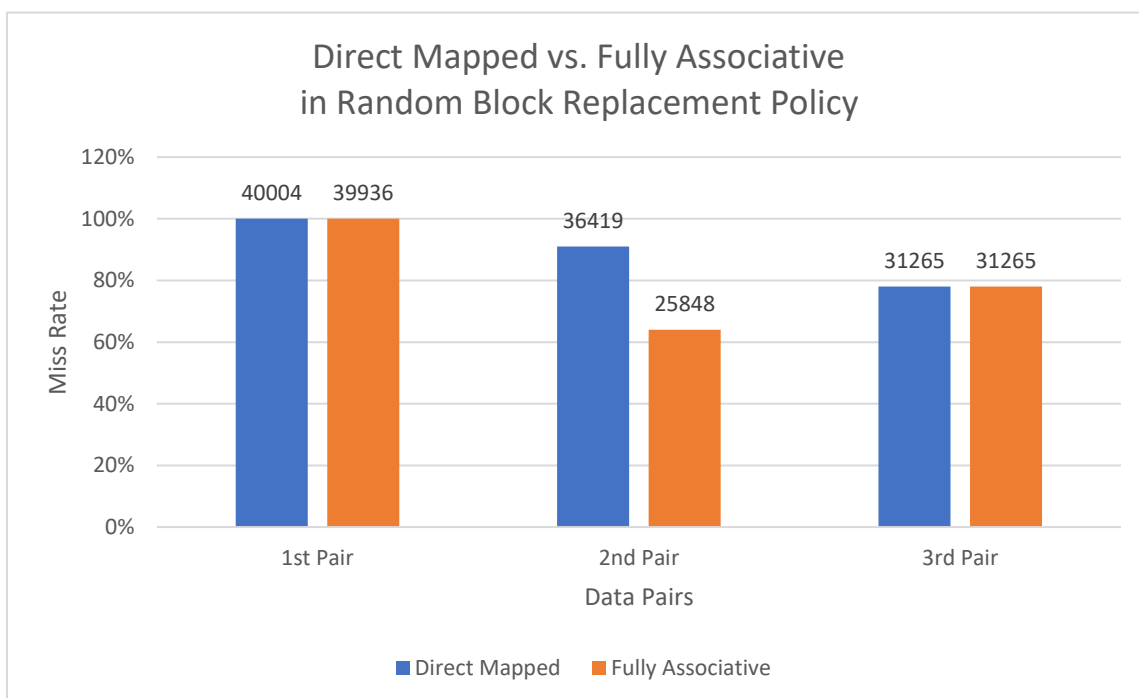
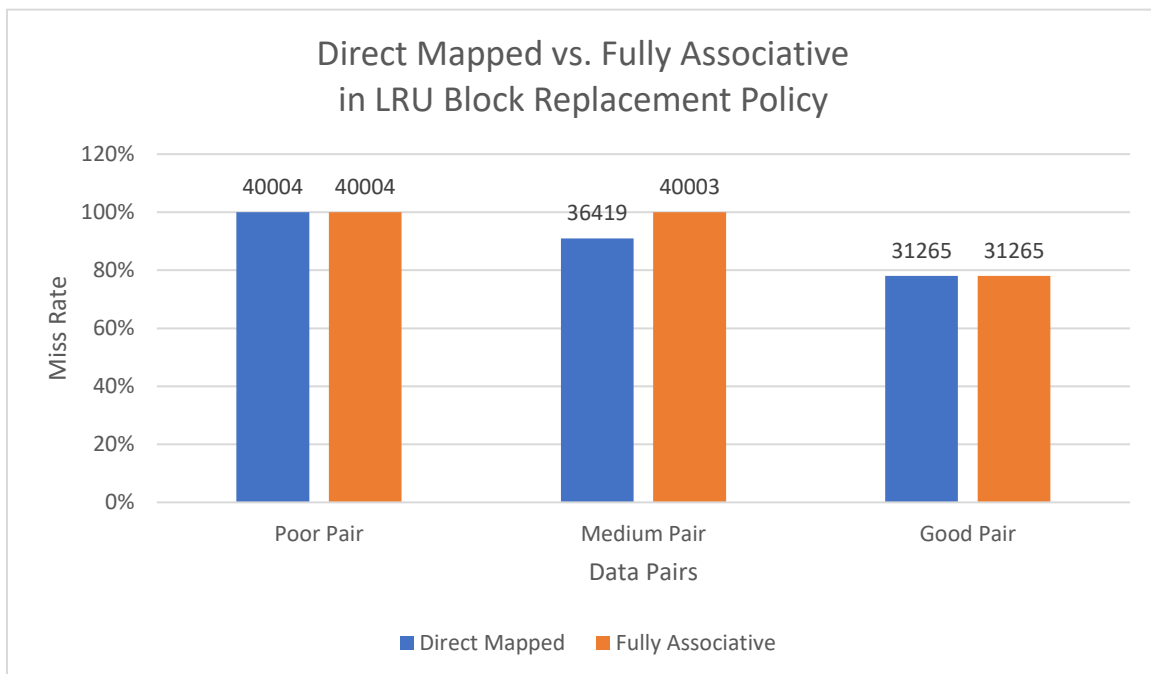


In first graph with LRU policy, we can see that in poor and medium hit rate, fully associative architecture didn't make any change. However, in good hit rate, it makes slightly worse.

In second graph with Random policy, we can see that architecture affected all rates in a slightly positive way.

I got my data from 200x200 matrix column-major results which are:

| Pair No. | 1 (Poor) | 2 (Medium) | 3 (Good) |
|-------------|----------|------------|----------|
| Block Size | 16 | 32 | 256 |
| Cache Size | 2048 | 16384 | 2048 |
| Miss Rate | %100 | %91 | %78 |
| # of Misses | 40004 | 36419 | 31265 |



In first graph with LRU policy, we can see that in poor and good hit rate, fully associative architecture didn't make any change. However, in medium hit rate, it makes slightly worse.

In second graph with Random policy, we can see that architecture affected poor pair in a positive way slightly but it affected medium pair very well.

My theory about these changes is that, LRU policy replaces a data that will be used in the future, even if it is the least recently used data. Because of this, cache misses data. It is similar in random policy too. However it is not always the same. Sometimes, data that will be used next is replaced but sometimes another data replaced instead. Miss values are close because randomly replaced data will be used too, not now but later. Therefore, misses happen less with random policy.

Part 2.c:

Results for 100x100 matrix:

Results for good rate:

| | | | | |
|-------------|------|------|------|------|
| Set size | 2 | 4 | 8 | 16 |
| Miss rate | %21 | %36 | %39 | %39 |
| # of misses | 2165 | 3581 | 3917 | 3917 |

Results for medium rate:

| | | | | |
|-------------|------|------|------|------|
| Set size | 2 | 4 | 8 | 16 |
| Miss rate | %78 | %78 | %78 | %78 |
| # of misses | 5013 | 5013 | 5013 | 5013 |

Results for poor rate:

| | | | | |
|-------------|-------|-------|-------|-------|
| Set size | 2 | 4 | 8 | 16 |
| Miss rate | %99 | %99 | %99 | %99 |
| # of misses | 10004 | 10004 | 10004 | 10004 |

N-way architecture didn't make a change in medium and poor rate. However, it made good rate worse. It is mostly affected when way number increased 2 to 4.

Results for 200x200 matrix:

Results for good rate:

| | |
|-------------|-------|
| Set size | 2 |
| Miss rate | %78 |
| # of misses | 31265 |

Results for medium rate:

| | | | | |
|-------------|-------|-------|-------|-------|
| Set size | 2 | 4 | 8 | 16 |
| Miss rate | %89 | %100 | %100 | %100 |
| # of misses | 35875 | 40003 | 40003 | 40003 |

Results for poor rate:

| | | | | |
|-------------|-------|-------|-------|-------|
| Set size | 2 | 4 | 8 | 16 |
| Miss rate | %100 | %100 | %100 | %100 |
| # of misses | 40004 | 40004 | 40004 | 40004 |

N-way architecture didn't make a change in good and poor rate. However, it made medium rate worse. It is mostly affected when way number increased 2 to 4.