CS224

Section No.: 1

Spring 2021

Lab No.: 6

Full Name/Bilkent ID: Ata Seren/21901575

Preliminary Report

Part 1.1:

No.	Cache Size KB	N-way cache	Word size in bits	Block size (no. of words)	No. of sets	Tag size in bits	Index size (Set No.) in bits	Word block offset size in bits	Byte offset size in bits	Block replacement policy needed(Yes/No)
1	**8**	**1**	**8**	**8**	2^{10}	16	10	3	0	No
2	**8**	**2**	**16**	**8**	2^{8}	17	8	3	1	Yes
3	**8**	**4**	**16**	**4**	2^{8}	18	8	2	1	Yes
4	**8**	**Full**	**16**	**4**	2^{0}	26	0	2	1	Yes
9	**32**	**1**	**16**	**2**	2^{13}	14	13	1	1	No
10	**32**	**2**	**16**	**2**	2^{12}	15	12	1	1	Yes
11	**32**	**4**	**8**	**8**	2^{10}	16	10	3	0	Yes
12	**32**	**Full**	**8**	**8**	2^{0}	26	0	3	0	Yes

Part 1.2:

a.

Instructions	Iteration no.				
	1	2	3	4	5
lw $t1, 0xA4($0)	Compulsory	Hit	Hit	Hit	Hit
lw $t2, 0xA8($0)	Hit	Hit	Hit	Hit	Hit
lw $t3, 0xAC($0)	Hit	Hit	Hit	Hit	Hit

b.

Memory size of one set: 1 bit “valid”+27 bits “tag”+4*32 bits “data” = 156 bits

Total cache memory (SRAM) size: 2 sets → 156*2 = 312 bits

c.

1 AND gate, 1 equality comparator, 1 4-to-1 MUX needed, no OR gate needed.

Part 1.3:

a.

Instructions	Iteration no.				
	1	2	3	4	5
lw $t1, 0xA4($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xA8($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0xAC($0)	Capacity	Capacity	Capacity	Capacity	Capacity

b.

For LRU policy, 1 bit for way 1 and 1 bit for way 0 is needed.

For a set, 1 bit “valid” + 1 bit “U” + 30 bits “tag”+ 32 bits “data” needed for way 1. For way 0, we need 1 bit “valid” + 30 bits “tag”+ 32 bits “data”.

Therefore, total size of cache is 127 bits.

c.

2 AND gates, 1 OR gate, 2 equality comparators and 1 2-to-1 MUX is needed.