

DA1458x Reference Design

Design Name	DA1458xDEVKT-B-VA (QFN40)
Ref. Number	321-4-B
Version	B00
Date	May, 02, 2017
Designer	PR KR

History Table		
Version	Date	Comments
A00	19 /Oct / 2016	Initial Schematic
A01	02 /Jan / 2017	1. R17, R18, R19: changed from 4.7k to 6.8k 2. U6 inverter NC7SZ04P5X changed to populated
A02	02 /May / 2017	3.Xtall Y2 changed to TXC 9HT11-32.768KDZB-T (6pF)
B00	08 /May / 2018	4. Critical change on the footprint of U4

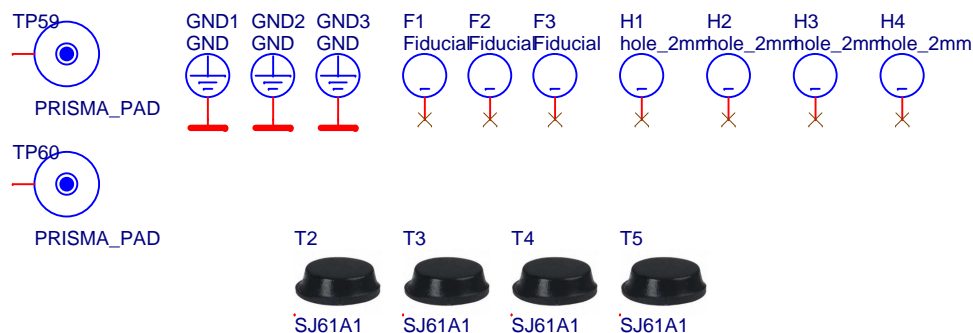
Configuration note

NOTE box

Changes in this Version.



Label_Dialog_L6008



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Title : DA1458xDEVKT-B

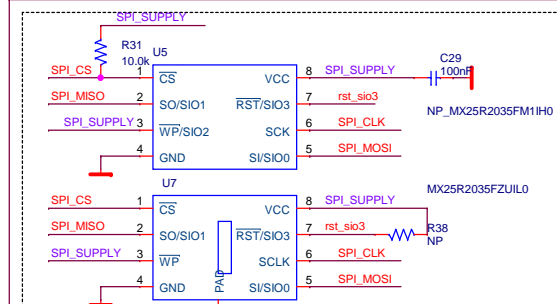
Doc. Nr.

Designer: PR

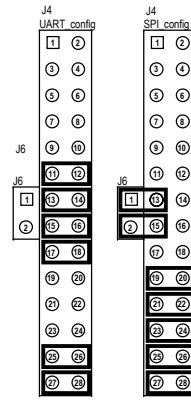
Rev:B

Date: Wednesday, May 09, 2018

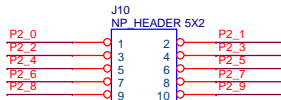
Sheet: 0 of 2



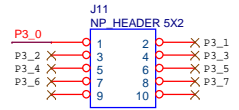
POPT PIN	UART	SPI
P0_0		SCK
P0_1		
P0_2		
P0_3		CS
P0_4	UTX	
P0_5	URX	MISO
P0_6	CTS	MOSI
P0_7	RTS	



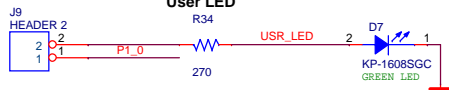
Available on QFN40 - QFN48



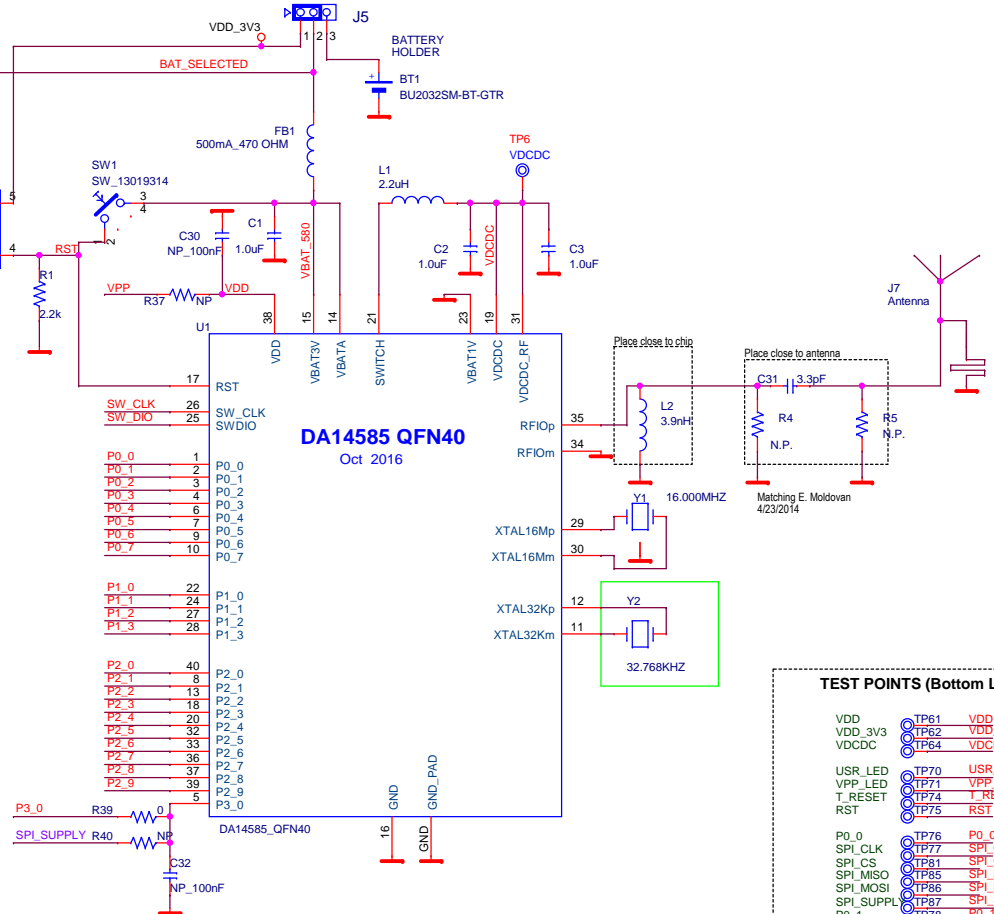
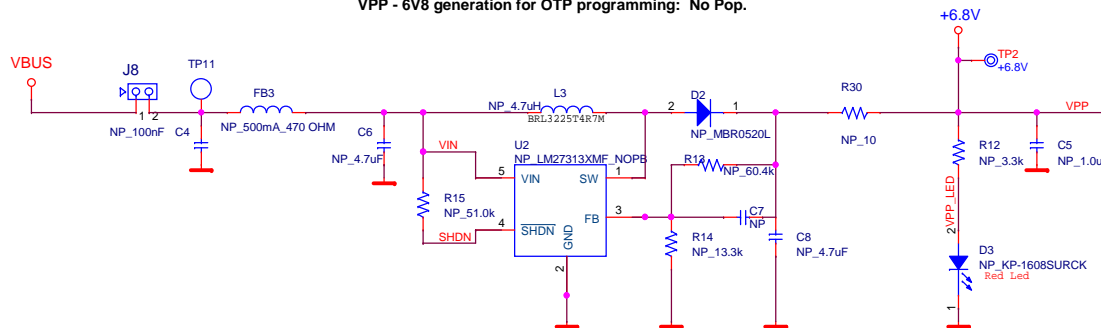
Available on QFN48



User LED



VPP - 6V8 generation for OTP programming: No Pop.



TEST POINTS (Bottom Layer)

VDD	TP61	VDD
VDD_3V3	TP62	VDD_3V3
VDDCDC	TP64	VDDCDC
USR_LED	TP70	USR_LED
VPP_LED	TP71	VPP_LED
T_RESET	TP74	T_RESET
RST	TP75	RST
P0_0	TP76	P0_0
SPI_CLK	TP77	SPI_CLK
SPI_CS	TP81	SPI_CS
SPI_MISO	TP85	SPI_MISO
SPI_MOSI	TP86	SPI_MOSI
SPI_SUPPLY	TP87	SPI_SUPPLY
P0_1	TP78	P0_1
P0_2	TP79	P0_2
P0_3	TP80	P0_3
P0_4	TP82	P0_4
P0_5	TP83	P0_5
P0_6	TP84	P0_6
BAT_SELECTED	TP88	BAT_SELECTED
GND1	TP89	
GND2	TP90	
GND3	TP91	
GND4	TP92	

Configuration					
Description	to VPP	Decoupling to VDD	to P3_0	VBAT3V	Decoupling
580	0ohm	NP	NP	NP	NP
581	0ohm	NP	NP	NP	NP
583	0ohm	NP	NP	0ohm	100nF
584	0ohm	NP	NP	0ohm	100nF
585 (default)	NP	NP	0ohm	NP	NP
586	NP	NP	NP	0ohm	100nF



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Title:	DA14585DEVKT-8	Designer:	PR	Rev:	A
Doc. No.:		Date:	Tuesday, May 08, 2018	Sheet:	1 of 2

