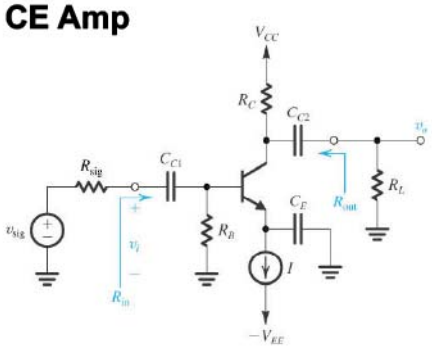
Outline

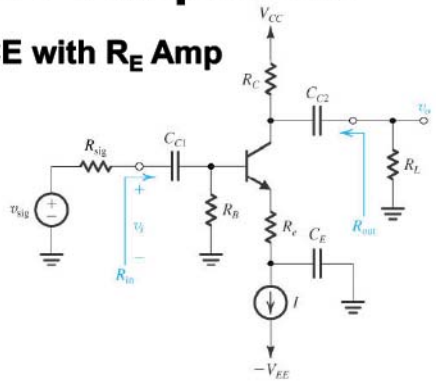
- Device Structure and Physical Operation
  - Current-Voltage Characteristics
- The BJT as an Amplifier
  - Biasing in BJT Amplifier Circuits
  - Small-Signal Operation and Models
- Single-Stage BJT Amplifiers
- Design Of Single-Stage BJT Amplifiers
  - Simulating BJT Circuits With SPICE
  - CE Amplifier Example
- Frequency Response Behavior
  - CE Amplifier
- Summary

Single Stage BJT Amplifiers

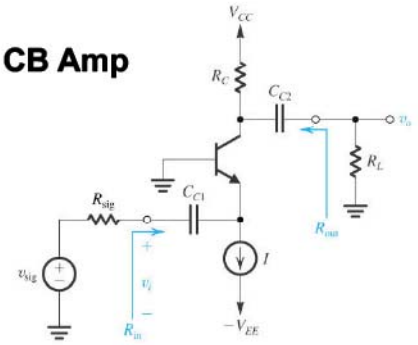
CE Amp



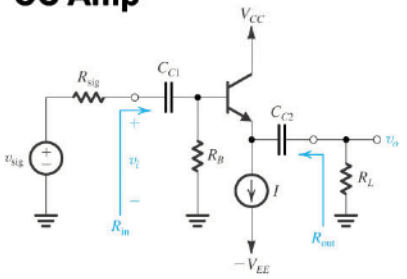
CE with R_E Amp



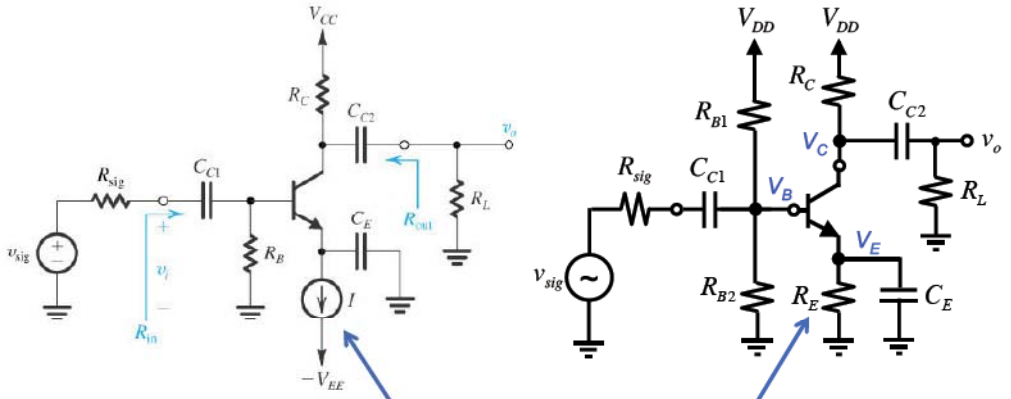
CB Amp



CC Amp

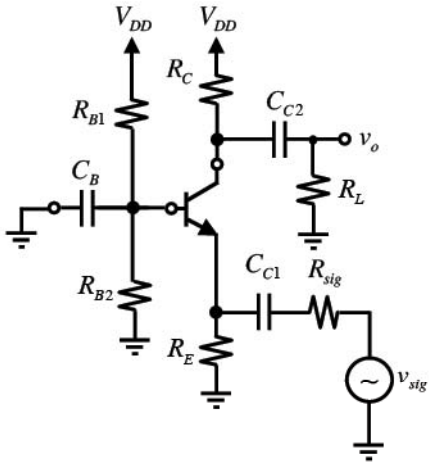


Single-Power Supply Common-Source Amplifier With Resistor Biasing

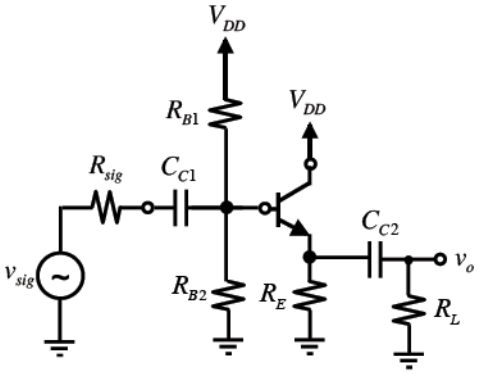


Replace *I* source with R_E @ V_E

Discrete Implementation Of Single-Supply CMOS Amplifiers



Common-Gate Amp.



Common-Drain Amp.

Basic BJT Amplifier Attributes

Amplifier	No-Load Voltage Gain	Current Gain	Input Resistance	Output Resistance
CE	No greater than 300 V/V (-ve)	β	Large (10k – 100k)	High (10k – 100k)
CB	No greater than 300 V/V (+ve)	α	Small (10 – 10k)	High (10k – 100k)
CC	Near Unity +ve	β+1	Medium (1k – 10k)	Small (10 – 1k)

Design Of A CE Amplifier

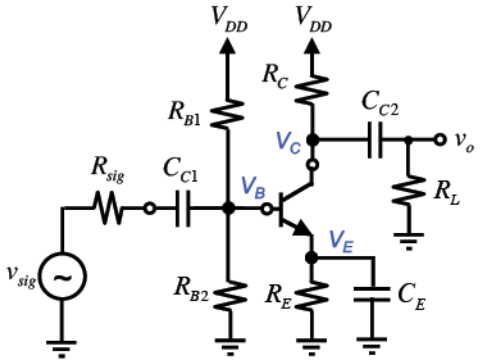
The design problem is to select V_E, V_C and I_C.

V_B is not a design variable, as it can be expressed as

$$V_B = V_E + V_T \ln\left(I_C / I_S\right) \approx V_E + 0.7 \text{ V}$$

Another design variable is R_{B1}. We are free to choose any value for it to set V_B:

$$V_B = \frac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} \Rightarrow R_{B2} = \left(\frac{V_B}{V_{CC}-V_B}\right) R_{B1}$$



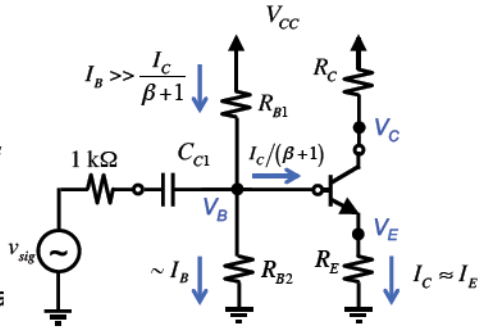
Design Of A CE Amplifier
Biasing Considerations

There are several biasing constraints on BJT amps:

(1) The input resistance to the amplifier should be set much larger than the source resistance to reduce any signal loss, i.e.,

$$R_{in} = R_{B1} \| R_{B2} \| (\beta+1) r_e >> R_{sig} \quad \Rightarrow \quad R_{B1} \| R_{B2} \| \frac{(\beta+1) V_T}{I_C} >> R_{sig}$$

Condition is not critical as the gain loss can be corrected using the transistor gain.



(2) Bias current through resistor divider at base termina $V_{DD}/(R_{B1}+R_{B2})$ must be much greater than the transistor base current $I_C/(\beta+1)$, i.e.

$$\frac{V_{CC}}{R_{B1}+R_{B2}} >> \frac{I_C}{(\beta+1)} \quad \Rightarrow \quad \frac{(V_E+0.7)(\beta+1)}{I_C} >> R_{B1}$$

R_{B1} should be made small enough to ensure voltage divider current is much greater than transistor base current.

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Design Of A CE Amplifier
Biasing Considerations

(3) The collector current I_C is selected to ensure the gain requirements are met:

Consider the loaded voltage gain of amplifier from base terminal to output terminal:

$$|A_v| = \frac{v_o}{v_b} = g_m \times R_C \| R_L \| r_o \geq |A_v^D|$$

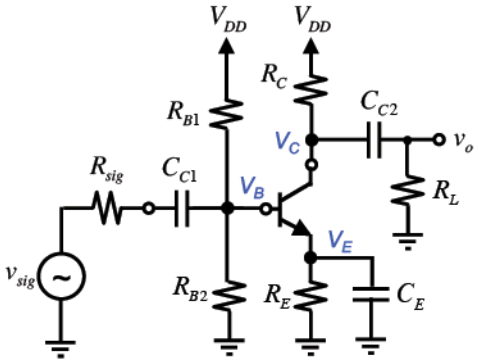
Substituting for known values, we write

$$|A_v| = \frac{V_T}{I_C} \times \left(\frac{V_{CC}-V_C}{I_C} \| R_L \| \frac{V_A}{I_C} \right) \geq |A_v^D| \Rightarrow \frac{I_C/V_T}{\frac{I_C}{V_{CC}-V_C} + \frac{1}{R_L} + \frac{I_C}{V_A}} \geq |A_v^D|$$

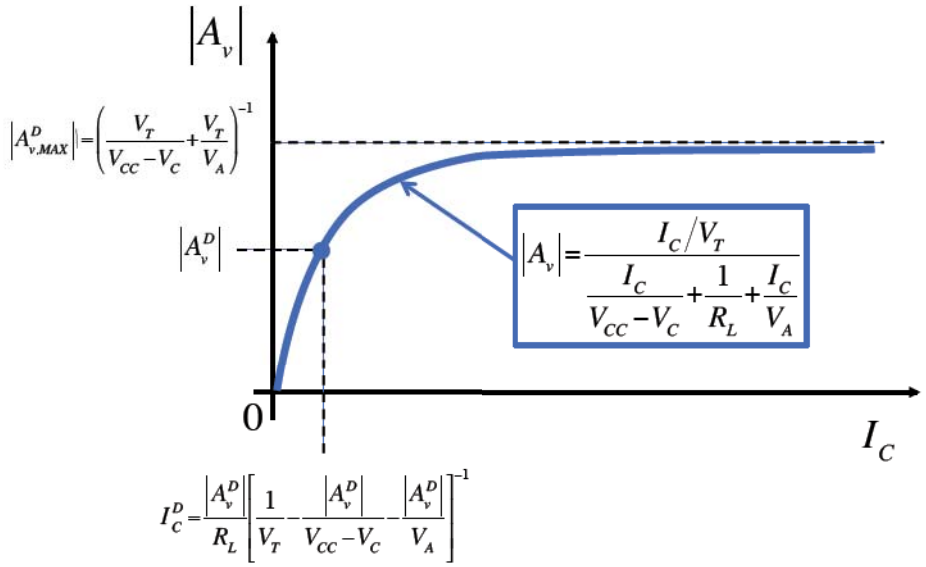
After some re-arranging,

$$I_C \geq \frac{|A_v^D|}{R_L} \left[\frac{1}{V_T} - \frac{|A_v^D|}{V_{CC}-V_C} - \frac{|A_v^D|}{V_A} \right]^{-1}$$

The higher the desired voltage gain, the larger the collector current.



Design Of A CE Amplifier
Voltage Gain Vs. I_C



$$I_C^D = \frac{|A_v^D|}{R_L}\left[\frac{1}{V_T}-\frac{|A_v^D|}{V_{CC}-V_C}-\frac{|A_v^D|}{V_A}\right]^{-1}$$

Design Of A CE Amplifier
Maximum Voltage Gain

We recognize from the collector current – voltage gain equation, i.e.,

$$I_C \geq \frac{|A_v^D|}{R_L}\left[\frac{1}{V_T}-\frac{|A_v^D|}{V_{CC}-V_C}-\frac{|A_v^D|}{V_A}\right]^{-1}$$

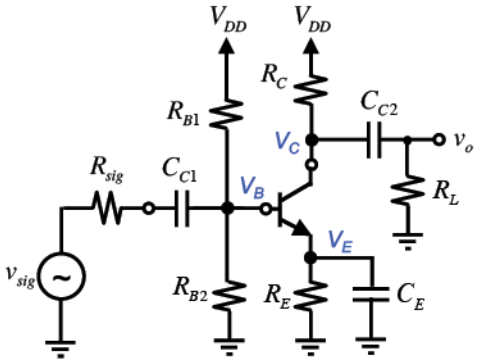
that the denominator goes to zero when

$$\frac{1}{V_T} = \frac{|A_v^D|}{V_{CC}-V_C}+\frac{|A_v^D|}{V_A}$$

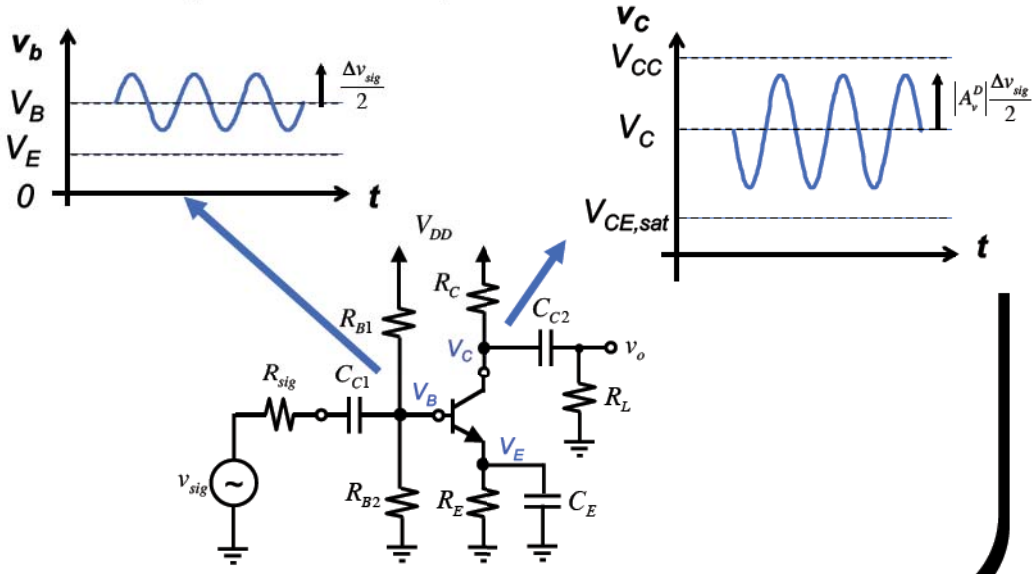
This in turn sets the upper limit on the desired voltage gain achievable by the CS amplifier as:

$$|A_{v,MAX}^D| = \left(\frac{V_T}{V_{CC}-V_C}+\frac{V_T}{V_A}\right)^{-1}$$

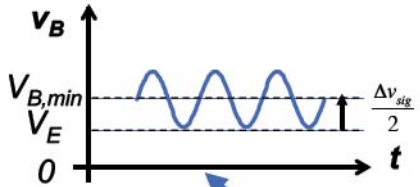
Don't expect to get more gain than above!



Design Of A CE Amplifier
Input and Output Signal Swings

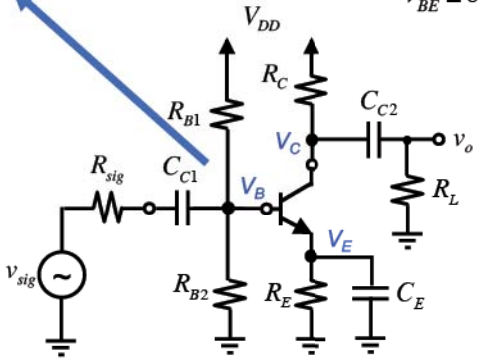


Design Of A CE Amplifier
Minimum Input Biasing Condition



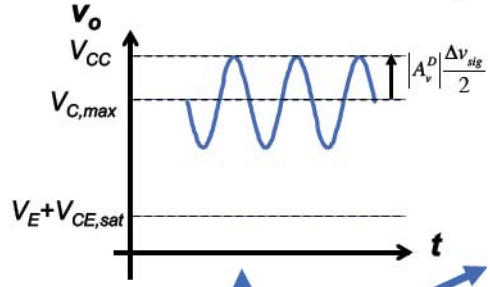
To allow a full input swing, the voltage across the base-emitter terminals of the transistor must satisfy:

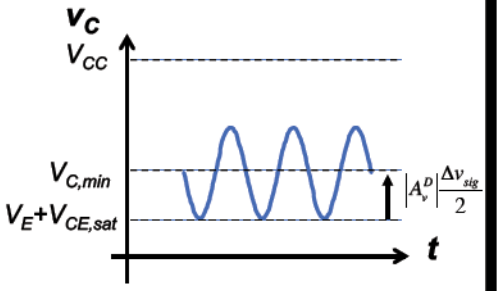
$$v_{BE} \geq 0 \Rightarrow V_{B,MIN} = V_E + \frac{\Delta v_{sig}}{2}$$

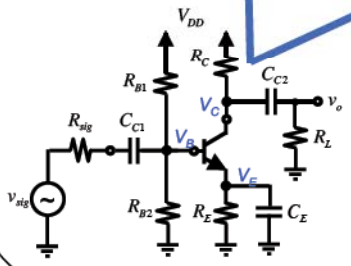


Design Of A CE Amplifier

Maximum Output Signal Swing







To allow the required output signal to swing while transistor remains in its active region, the following two conditions must be met:

$$V_{C,MAX} = V_{CC} - |A_v^D|\frac{\Delta v_{sig}}{2}$$

$$V_{C,MIN} = V_E + V_{CE,sat} + |A_v^D|\frac{\Delta v_{sig}}{2}$$

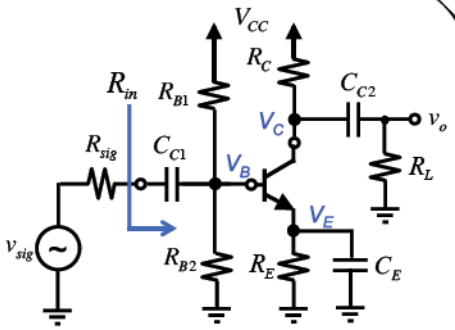
Bias Levels For CE Amplifier

Design Conditions

$$R_{in} = R_{B1} \| R_{B2} \| (\beta+1) r_e >> R_{sig}$$

$$\frac{V_{CC}}{R_{B1}+R_{B2}} >> \frac{I_C}{(\beta+1)}$$

$$|A_v^D| < \left(\frac{V_T}{V_{CC}-V_C} + \frac{V_T}{V_A}\right)^{-1}$$



Amplifier Type		Node Voltages				Collector Current	
		V_E	V_B	$V_{C,MIN,AC}$	$V_{C,MAX,AC}$	$I_{C,MIN}$	$I_{C,Av}$
CE	Bias Voltage	V_E	$V_E + V_T \ln(I_C/I_S) \approx V_E + 0.7$ V	$V_E + V_{CE,sat} + \|A_v^D\|\frac{\Delta v_{sig}}{2}$	$V_{CC} - \|A_v^D\|\frac{\Delta v_{sig}}{2}$	$I_s e^{\left(\frac{\Delta v_{sig}}{2}\right)/V_T}$	$\frac{\|A_v^D\|}{R_L}\left[\frac{1}{V_T} - \frac{\|A_v^D\|}{V_{CC}-V_C} - \frac{\|A_v^D\|}{V_A}\right]^{-1}$
	Res.	$R_{B1} = R_{nom}$		$R_{B2} = \left(\frac{V_B}{V_{CC}-V_B}\right)R_{B1}$		$R_E = \frac{V_E}{I_C}$	$R_C = \frac{V_{CC}-V_C}{I_C}$
	Caps.	$C_{C1} = \frac{1}{(R_{sig}+R_{B1}\|R_{B2})\omega_{p,2}}$		$C_{C2} = \frac{1}{(R_C+R_L)\omega_{p,3}}$		$C_E = 1/(R_E\|r_e)\omega_{p1}$	

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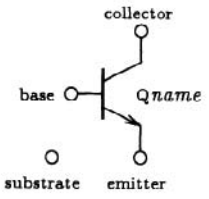
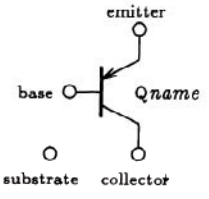
SPICE BJT Statement

Element	Spice Description
	Q*name* collector base emitter [substrate] *BJT_model_name* [*#_in_parallel*] .MODEL *BJT_model_name* NPN (*parameter_name=value* ....)
	Q*name* collector base emitter [substrate] *BJT_model_name* [*#_in_parallel*] .MODEL *BJT_model_name* PNP (*parameter_name=value* ....)

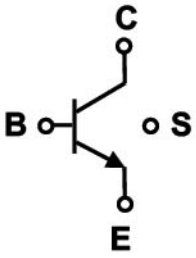
- SPICE has a built-in model for an npn and pnp BJTs.

BJT SPICE Model

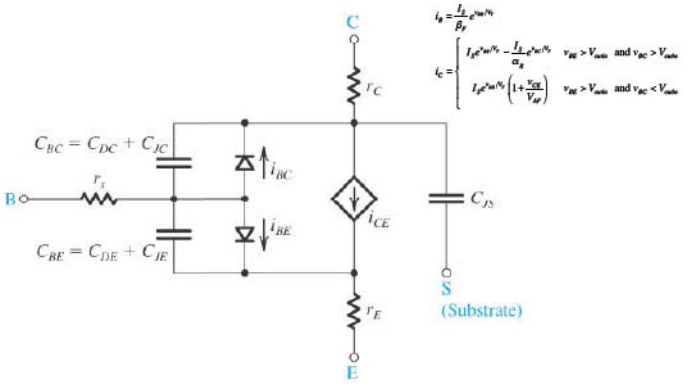
- The following is a partial listing of the SPICE parameters for a static BJT model:

Symbol	SPICE Name	Model Parameter	Units	Default
I_S	Is	Saturation Current	Amps	$1x10^{-16}$
β_F	Bf	Forward Current Gain		100
V_{AF}	VAf	Forward Early Voltage	Volts	∞
r_B	Rb	Base Ohmic Resistance	Ohms	0
r_C	Rc	Collector Ohmic Resistance	Ohms	0
r_E	Re	Emitter Ohmic Resistance	Ohms	0

SPICE Large Signal NPN BJT Model



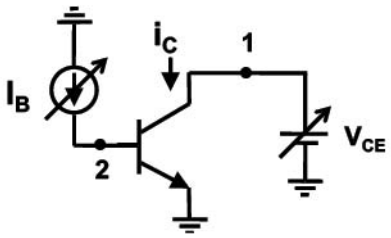
symbol



Equivalent SPICE Circuit

- Any time an NPN BJT appears in a circuit it is replaced by the circuit model shown here.
  - Static and dynamic behavior is captured by model.

SPICE Curve Tracer Example



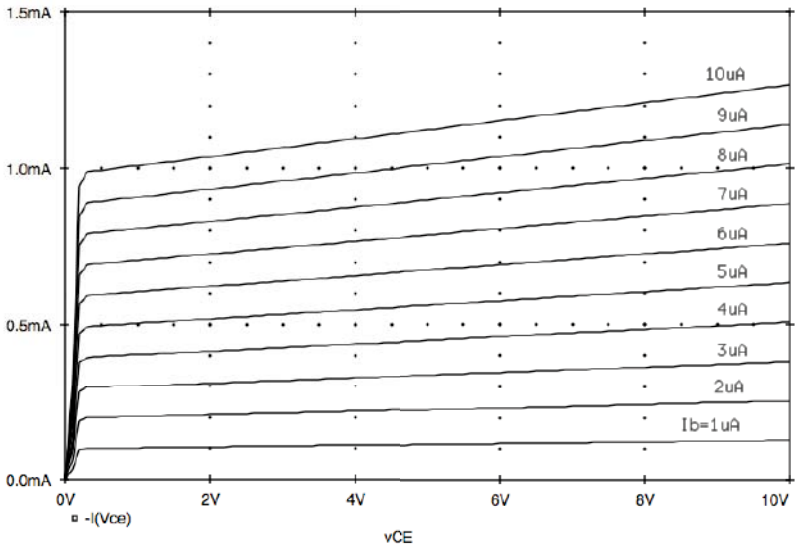
BJT Curve Tracer Setup

```
Spice As A Curve Tracer: BJT I-V Characteristics

** Circuit Description **
Vce 1 0 DC 0V
Ib 0 2 DC 10uA
* device under test
Q1 1 2 0 npn_transistor
* transistor model statement
.model npn_transistor NPN (Is=1.8104e-15A Bf=100
VAf=35V)

** Analysis Requests **
* vary Vce from 0V to 10V in steps of 100mV
.DC Vce 0V +10V 100mV Ib 1u 10u 1u

** Output Requests **
.plot DC I(Vce)
.end
```

SPICE Input Deck

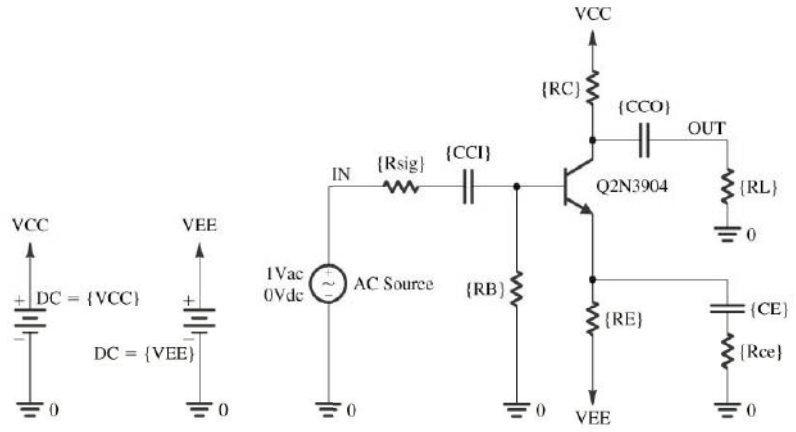
Simulation Results

IC-VCE Vs IB

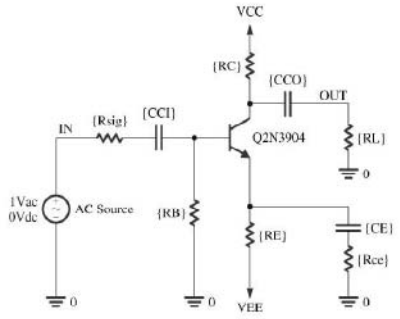


Frequency Response Of A CE Amp

PARAMETERS:
CE = 10u
CCI = 10u
CCO = 10u
RC = 10K
RB = 340K
RE = 6K
Rce = 130
RL = 10K
Rsig = 10K
VCC = 5
VEE = −5



SPICE Deck

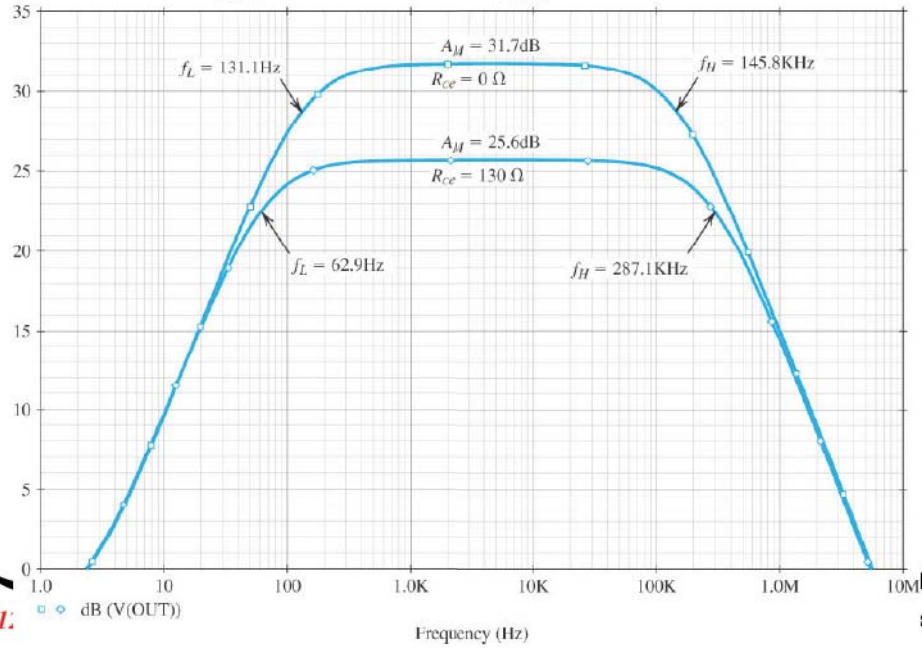


Common-Emitter Amplifier Stage

```
** Circuit Description **
* power supplies
Vcc 1 0 DC +10V
Vee 8 0 DC -10V
* input signal
Vs 6 0 AC 10mV
Rs 5 6 10k
* amplifier
C1 4 5 1GF
Rb 4 0 100k
Q1 2 4 3 Q2N3904
Rc 1 2 10k
Re 3 8 10k
C2 2 7 1GF
C3 3 0 1GF
* load + ammeter
Rl 7 9 10k
Vout 9 0 0
```

```
* transistor model statement for the Q2N3904
.model Q2N3904 NPN (Is=14.34f Xti=3 Eg=1.11 Vaf=74.03 Bf=255.9 Ne=1.307
+                   Ise=14.34f Ikf=.2847 Xtb=1.5 Br=6.092 Nc=2 Isc=0 Ikr=0 Rc=1
+                   Cjc=7.306p Mjc=.3416 Vjc=.75 Fc=.5 Cje=22.01p Mje=.377 Vje=.75
+                   Tr=46.91n Tf=411.1p Itf=.6 Vtf=1.7 Xtf=3 Rb=10)

** Analysis Requests **
* calculate DC bias point information
.OP
.AC DEC1 1Hz 10MegHz

** Output Requests **
*  voltage gain Av=Vo/Vs
.PRINT AC VdB(7)
.end
```

Simulation Results
R_{ce}=0 and R_{ce}=130 Ω



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Design Of A CE Amplifier
Example

Design a DC coupled CE amplifier with a voltage gain having a magnitude of at least 30 V/V driven by a source with resistance of 1000 Ω and loaded by a 15 kΩ / 10 pF load. The input will vary over 20 mV voltage range with a range of signals from 100 Hz to 10 kHz. The power supply is assumed to be +12 V. The BJT can be described by $I_s=10^{-15}$ A, β=100 and V_A=100 V.

Solution:

The design problem is to select V_E, V_C and I_C.

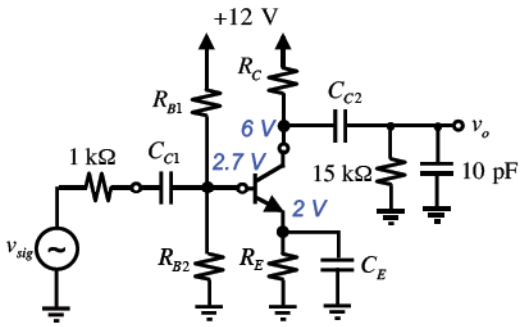
Let us begin with setting the node voltages:

$$V_E=2.0\text{ V},\quad V_C=6.0\text{ V}$$

and approximate the base voltage as

$$V_B=V_E+0.7=2.7\text{ V}$$

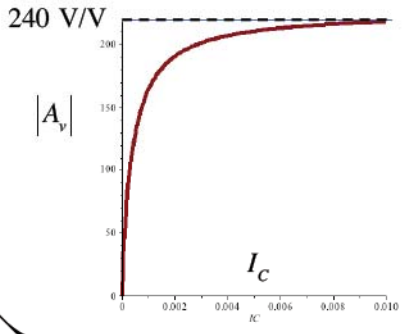
The drain voltage is positioned almost in the middle of the power supply – the best possible place for it.

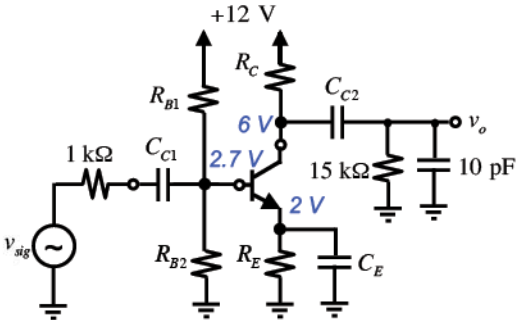


Design Of A CE Amplifier
Example

$$|A_v|=\frac{I_C/V_T}{\dfrac{I_C}{V_{CC}-V_C}+\dfrac{1}{R_L}+\dfrac{I_C}{V_A}}$$

$$V_E=2.0\text{ V},\quad V_B=2.7\text{ V},\quad V_C=6.0\text{ V}$$





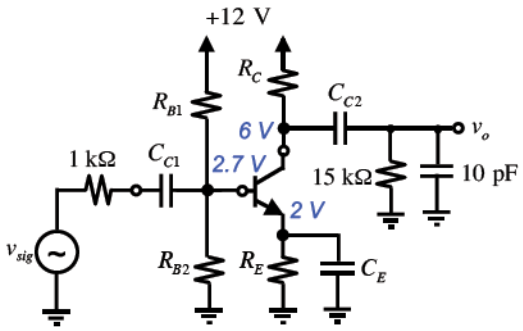
Design Of A CE Amplifier
Example Continued

Next, we compute the desired current level from the desired voltage gain equation, i.e.,

$$I_C \geq \frac{|A_v^D|}{R_L}\left[\frac{1}{V_T}-\frac{|A_v^D|}{V_{CC}-V_C}-\frac{|A_v^D|}{V_A}\right]^{-1}$$

First, lets check to see what the maximum achievable gain is and whether our desired gain is achievable:

$$\begin{aligned}|A_{v,MAX}^D| &= \left(\frac{V_T}{V_{CC}-V_C}+\frac{V_T}{V_A}\right)^{-1}\\ &= \left(\frac{0.025}{12-6}+\frac{0.025}{100}\right)^{-1}\\ &= \left(0.0042+0.00025\right)^{-1}\\ &\approx \left(0.0042\right)^{-1}\\ &= 240\frac{V}{V}\end{aligned}$$



Here we see the maximum gain of 240 V/V far exceeds our gain requirements of 30 V.V.

Design Of A CE Amplifier
Example Continued

Returning to the current equation, we solve

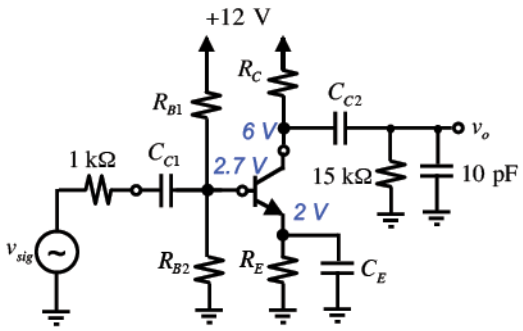
$$\begin{aligned}I_C &\geq \frac{|A_v^D|}{R_L}\left[\frac{1}{V_T}-\frac{|A_v^D|}{V_{CC}-V_C}-\frac{|A_v^D|}{V_A}\right]^{-1}\\ &\geq \frac{30}{15}\left[\frac{1}{25\times10^{-3}}-\frac{30}{12-6}-\frac{30}{100}\right]^{-1}\text{ mA}\\ &\geq 0.06\text{ mA}\end{aligned}$$

To provide some design margin, we'll select the collector current as

$$I_C = 0.1\text{ mA},$$

Now, we can compute the upper limit to R_{B1} according to

$$\frac{(V_E+0.7)(\beta+1)}{I_C} >> R_{B1} \Rightarrow \frac{(2.0+0.7)(100+1)}{0.1\text{ mA}} >> R_{B1} \Rightarrow 2660\text{ k}\Omega >> R_{B1}$$



Therefore we select R_{B1} as:

$$R_{B1} = 266\text{ k}\Omega$$

Design Of A CE Amplifier
Example Continued

With R_{B1} now known, we can compute the value for R_{B2} according to

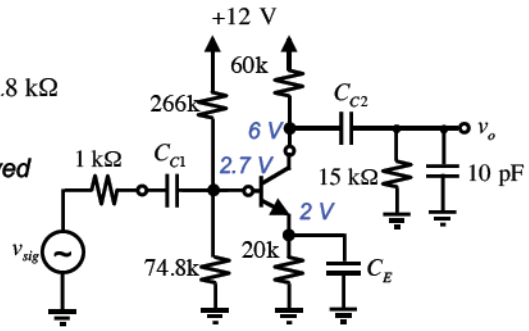
$$R_{B2}=\left(\frac{V_B}{V_{CC}-V_B}\right)R_{B1} \Rightarrow R_{B2}=\left(\frac{2.7}{12-2.7}\right)(266\ \text{k}\Omega)=74.8\ \text{k}\Omega$$

Note, a more accurate value for V_B can be derived but this is seldom necessary, as the component tolerances will mask any improvement.

Next, we compute R_E and R_C according to

$$R_E=\frac{V_E}{I_C}=\frac{2\ \text{V}}{0.1\ \text{mA}}=20\ \text{k}\Omega$$

$$R_C=\frac{V_{CC}-V_C}{I_C}=\frac{12-6\ \text{V}}{0.1\ \text{mA}}=60\ \text{k}\Omega$$



Final Design

Calculate Circuit Parameters

BJT CE Amplifier Requirements							
Input Signal Swing (V)	*Desired Voltage Gain (V/V)*	*Lower frequency (Hz)*	*Upper frequency (Hz)*	*Source Resistance (Ohms)*	*Load Resistance (kOhms)*	*Min. Input Resistance (kOhms)*	*Power Supply Voltage (V)*
0.020	-30.0	100	10000	1000	15	10	12

BJT Transistor Process Parameters					
# Parallel	Saturation Current (fA)	Beta	VT (mV)	Early Voltage (V)	Satuation Voltage (V)
1	1.0	100	25.0	100	0.2

Transistor Node Voltages			
Computed Value	*Designer Selected*		
VB (V)	IC (mA)	VE (V)	VC (V)
2.633	0.1000	2.00	6.00

Everything Below This Line Is Calculated

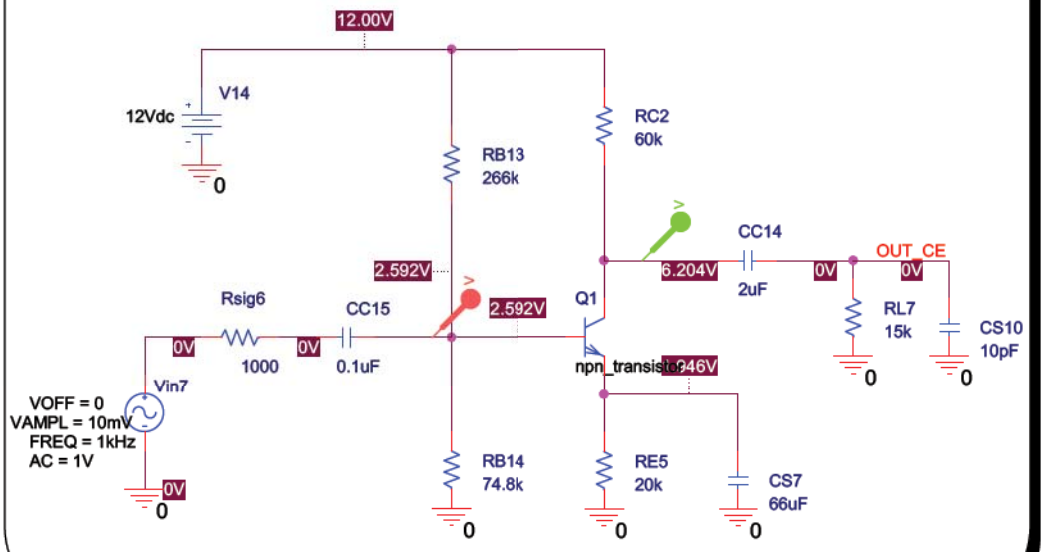
Collector Voltage AC Signal Limits, VC	
VC,MIN (V)	VC,MAX (V)
2.50	11.7

Collector Current Limits		
IC,min (mA)	IC,Av (mA)	Av,max (V/V)
0.0	0.0576	226.4

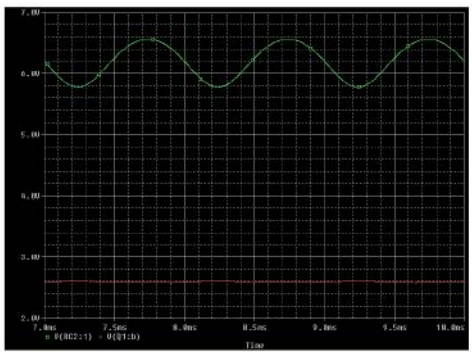
Transistor Parameters				Performance Metrics			
Collector Current (mA)	Transconductance gm (mA/V)	Output Resistance (kOhms)	Minimum DC Collector Voltage (V)	Actual Input-Output Voltage Gain (V/V)	Expected Output Signal Swing (V)	Maximum Available Voltage Swing (V)	Actual Input Resistance (kOhms)
0.100	4.0	1000	2.20	-44.88	0.90	9.800	17.62

Circuit Components						
Resistors				Capacitors		
RB1	RB2	RE	RC	CC1	CC2	CE
(kOhms)	(kOhms)	(kOhms)	(kOhms)	(uF)	(uF)	(uF)
266.0	74.8	20.0	60.0	0.156	2.12	64.46

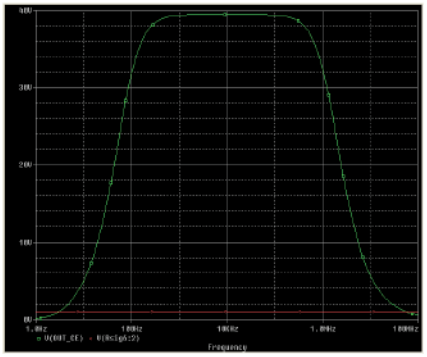
SPICE Test Setup



SPICE Results



Transient Response to 10 mV Input



AC Response to 1 V Input

Gain easily meets spec of -30 V/V (actual -40 V/V).

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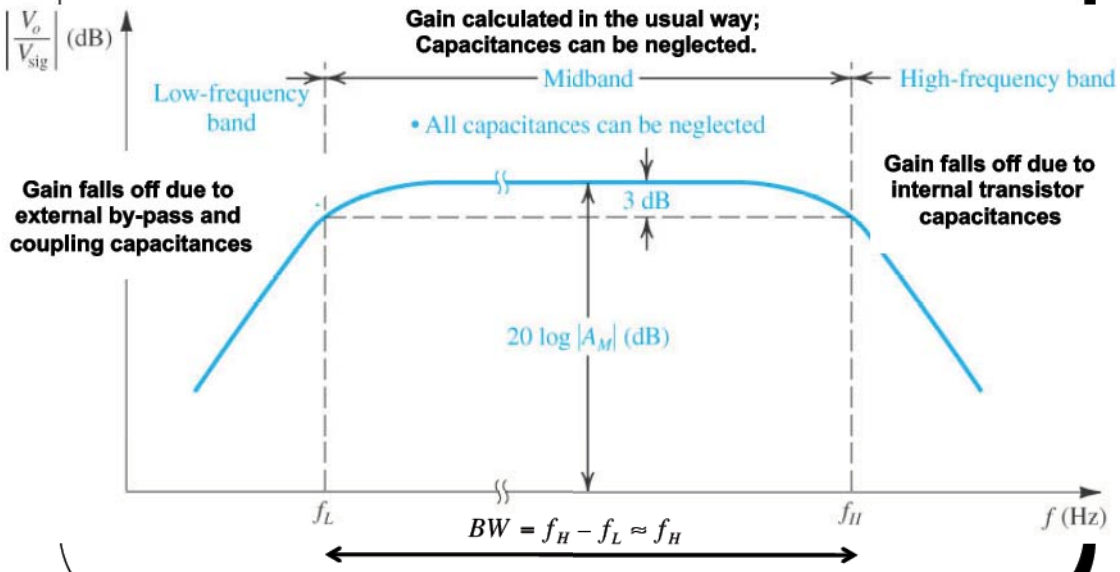
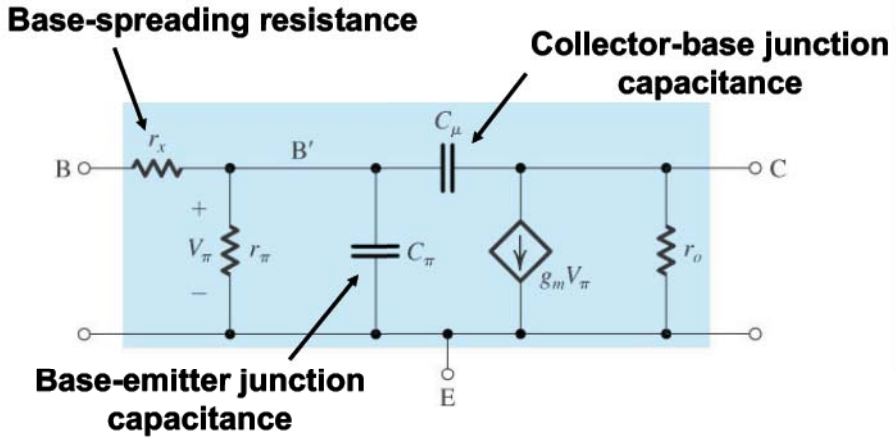
Attributes of a Frequency Response

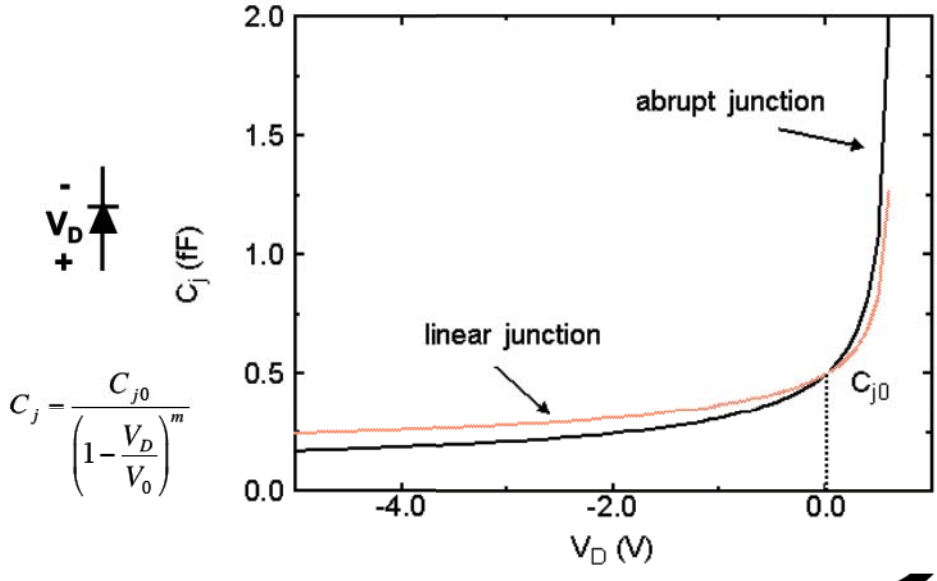


Hybrid-Pi BJT High-Frequency Model



- The hybrid-pi model is extended to higher ranges of frequencies by including the various junction capacitances and a base-spreading resistor.

PN Junction Capacitance



$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{V_0}\right)^m}$$

Capacitances

- ***Base-Collector Junction:***

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m}$$

where $C_{\mu o}$ is the value of C_μ at zero voltage, V_{0c} is the CBJ built-in voltage (typically 0.75 V) and *m* is its grading coefficient (typically, 0.2 – 0.5).

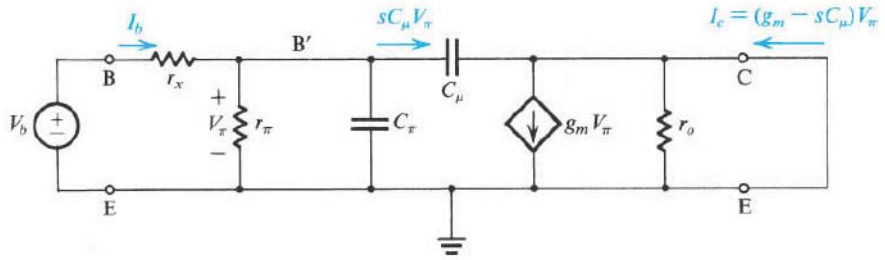
- ***Base-Emitter Junction:***

$$C_\pi = \frac{C_{je0}}{\left(1 - \frac{V_{BE}}{V_{0e}}\right)^m} + \tau_F \frac{I_C}{V_T} \approx 2C_{je0} + \tau_F \frac{I_C}{V_T}$$

EBJ is forward biased in the active mode, so the right most approximation is used as it is more accurate. Here C_{je0} is the value of C_{je} at zero voltage, τ_F is the forward base-transit time accounting for the base charging diffusion capacitance.

Maximum Cut-Off Frequency

Short-Circuit Operation

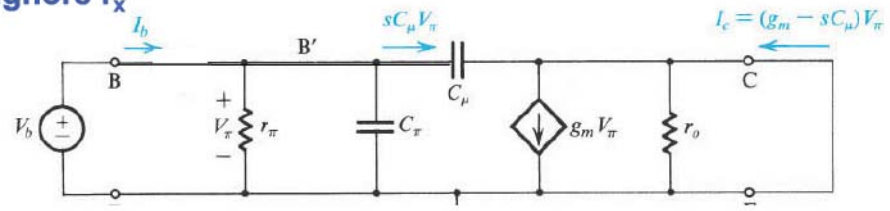


- Generally the value for the C_π is not given on BJT device data sheets, rather an alternative parameter is listed called the cutoff frequency, f_T.
- The cutoff frequency is derived from the short-circuit model of device behavior shown above.

Maximum Cut-Off Frequency

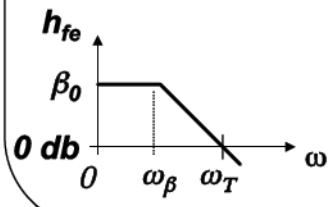
Frequency Analysis

Ignore r_x



$$h_{fe} \equiv \frac{I_c}{I_b} \cong \frac{g_m r_\pi}{1 + s(C_\pi + C_\mu)r_\pi} = \frac{\beta_0}{1 + s(C_\pi + C_\mu)r_\pi}$$

According to one-pole model:



$$\omega_\beta = \frac{1}{(C_\pi + C_\mu)r_\pi}$$

$$\omega_T = \beta_0 \omega_\beta = \frac{g_m}{C_\pi + C_\mu}$$

C_π and r_π parameters are dependent on current level!

Deriving Device Capacitance From f_T

$$\because f_T = \frac{1}{2\pi}\frac{g_m}{C_\pi + C_\mu}$$

- Given the device f_T, we can state that the sum of the internal capacitance are given by

$$\therefore C_\pi + C_\mu = \frac{1}{2\pi}\frac{g_m}{f_T}$$

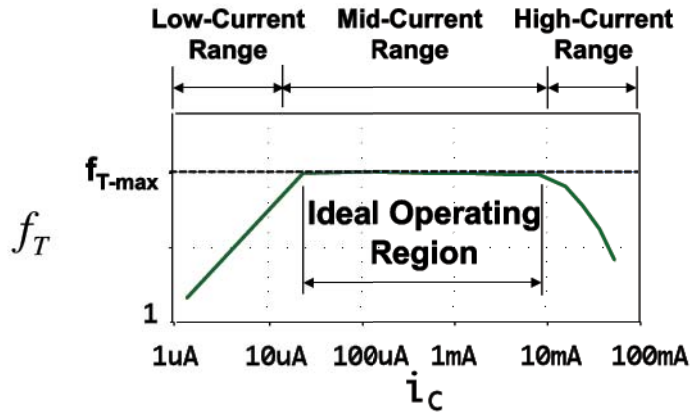
- But we also know that

$$C_\pi \approx 2C_{je0} + \tau_F \frac{I_C}{V_T}$$

- Hence, we can state C_μ as

$$\therefore C_\mu = \frac{1}{2\pi}\frac{g_m}{f_T} - C_\pi = \frac{1}{2\pi}\frac{g_m}{f_T} - \left(2C_{je0} + \tau_F \frac{I_C}{V_T}\right)$$

f_T Frequency Dependence



- Parasitic capacitances, r_π, as well as β, depend on bias levels, hence f_T varies with bias levels.
- Lumped hybrid-p model is valid only to ~0.2 f_T, above this a distributed model is required.

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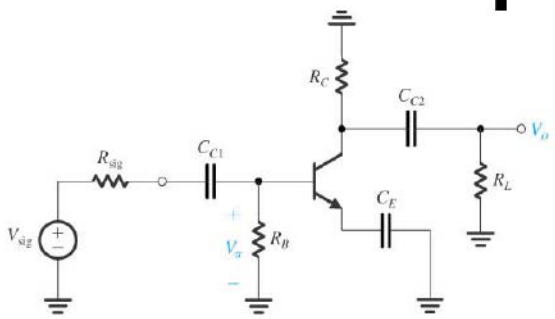
CE Amplifier Low Frequency Response

- The low-frequency frequency behavior is computed by ignoring the internal transistor capacitances)open circuit) and computing the transfer function of the circuit.
- Complicated transfer function analysis, instead make use of the method of **Short-Circuit Time-Constant Method.**



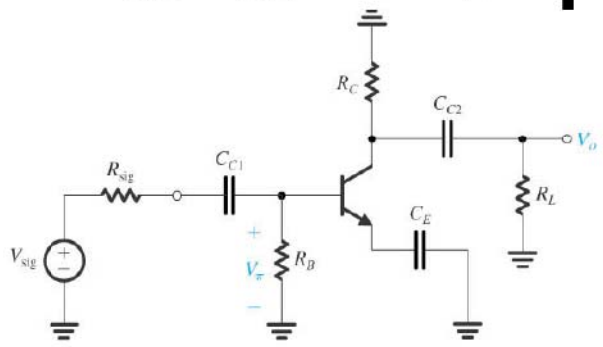
Individual Time Constants Associated With C_{C1}, C_{C2} and C_E

By inspection:

$$R_{1,eq} = R_{sig} + R_B \| r_\pi$$
$$\tau_1 = R_{1,eq} C_{C1} = \left(R_{sig} + R_B \| r_\pi\right) C_{C1}$$

$$R_{2,eq} = R_C + R_L$$
$$\tau_2 = R_{2,eq} C_{C2} = \left(R_C + R_L\right) C_{C2}$$

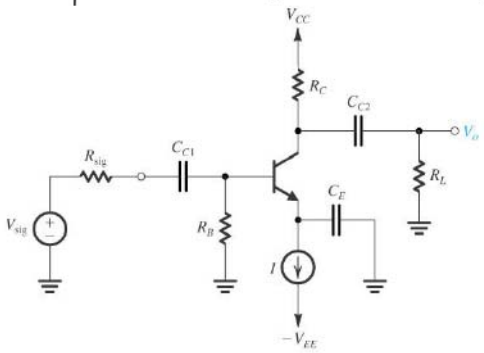
$$R_{3,eq} = r_e + \frac{R_B \| R_{sig}}{\beta + 1}$$
$$\tau_3 = R_{3,eq} C_E = \left(r_e + \frac{R_B \| R_{sig}}{\beta + 1}\right) C_E$$

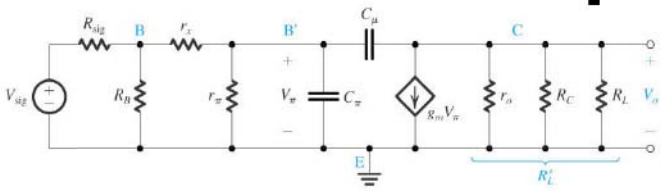


f_L estimation:

$$\omega_L \cong \sum_i \frac{1}{\tau_i} = \frac{1}{\left(R_{sig} + R_B \| r_\pi\right) C_{C1}} + \frac{1}{\left(R_C + R_L\right) C_{C2}} + \frac{1}{\left(r_e + \frac{R_B \| R_{sig}}{\beta + 1}\right) C_E}$$

CE Amplifier High-Frequency Response

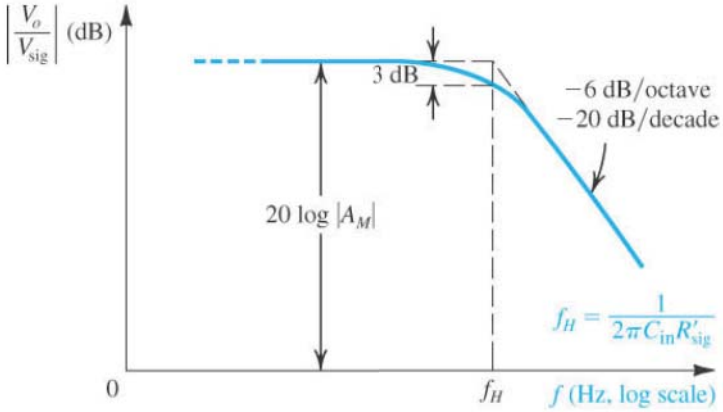




High-Frequency Equivalent Circuit (by-pass capacitors act as shorts)

- The most direct method is to derive the transfer function of the circuit.
  - Typically a very complicated process and leads to complicated expression.
  - Make use of the method of ***open-circuit time constants***.

CE Amplifier High-Frequency Response



- A simplified high-frequency analysis leads to the 3-dB frequency estimate

$$f_H \simeq \frac{1}{2\pi C_{in} R'_{sig}} = \frac{1}{2\pi\left[C_\pi + C_\mu\left(1+g_m R'_L\right)\right]\left[r_\pi \| \left(r_x + R_B \| R_{sig}\right)\right]}$$

Summary

- The BJT is a versatile device that has been around since the late forties.
- Amplification is one of the main applications of this technology; digital logic is another.
- We learned about the nonlinear i-v characteristics of the BJT, how to analyze them in circuits.
- Due to the non-linear behavior, circuit analysis is very complicated and usually needs numerical methods to solve.
- A graphical method was introduced to aid visualization of solution space.
- An approximation method based on Taylor series approximation was introduced:
  - linear small-signal equivalent transistor model
- Linear circuit behavior such as low, mid-band and high-frequency response, was described.