Design of State of Charge and Health Estimation for Li-ion Battery Management System

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Abstract— **Recently, researches on the battery management system(BMS) have been actively conducted due to the increase in various electric vehicles. The main function of the BMS is to predict the state of charge(SOC) and the state of health(SOH) of the battery cell to ensure the stability of the vehicle and to achieve optimal performance. This paper designs block IP for estimating SOC and SOH for lithium-ion batteries up to 15 cells and implements an FPGA testbed to verify the block IP to be mounted in an SoC for BMS to accurately estimate SOC and SOH for multiple battery cells.**

Keywords; State-of-charge (SOC), State-of-health (SOH), Battery management system (BMS), Electric vehicle (EV)

I. Introduction

Due to the rapidly increasing variety of electric vehicles (EVs) in recent years, many automobile manufacturers are investing in the research of electric systems [1]. With increasing battery capacity, the battery management system (BMS) is regarded as a key block of EVs [2]. The main function of the BMS is to monitor the state of a battery composed of several cells, and based on this, determine the state of the battery and ensure system safety. Therefore, in order to provide the optimal performance of the BMS, high-accuracy battery monitoring, especially the estimation of state of charge(SOC) and state of health(SOH), is an essential element, and many studies are being conducted [3].

In this paper, hardware design of SOC and SOH estimation for li-ion batteries up to 15 multi-cells is presented and is implemented to simulate and evaluate the real-time estimation performance by monitoring it based on FPGA.

II. Battery State Estimation

The battery modeling technique based on equivalent circuit model is widely used to estimate battery SOC [4]. Various SOC estimation methods have been studied [5-6]. They can be classified into two methods: 1) Coulomb coefficient based estimation and 2) Voltage based estimation. The Coulomb coefficient-based estimation method simply uses the integral function of the measured current, but shows the accumulated error over time. Voltage-based estimation method calculates SOC based on pre-defined open-circuit voltage (OCV)-SOC model based on the characteristic of the battery cell, and it may show better performance at real-time.

On the other hand, instantaneous SOH estimation is not an simple problem. SOH can be obtained as following equation:

$$\Sigma I = \Delta SOC \, * C * \, SOH, \tag{1}$$

where I represents the current and C represents the capacity of battery.

III. Hardware Design and Verification

A. Hardware Design

The proposed SOC and SOH estimation block IP was designed as shown in Figure 1. The input is 16 bits V, I, T for measured values, and 8 bits N, K for internal parameters. V and T is firstly used in SOC estimation block, and SOC is calculated based on OCV-SOC table with an error range within 2% of a 3.4 to 4.2 V lithium-ion battery in units of 0.002% [7]. The SOC is finally decided by correcting with the Kalman-filter based prediction technique. The correction must be needed because of the its jagged measured values. The SOH estimation is designed with SRAM that accumulates I and SOC, and the size can be selected as K up to 2048. With SRAM, for the given period, ΣI and ΔSOC is obtained and finally SOH can be calculated as (1). The final SOC and SOH is smoothed with 3-depth FIR filter with weight parameter N for stable outputs. The IP was designed to work for 100MHz clock frequency.

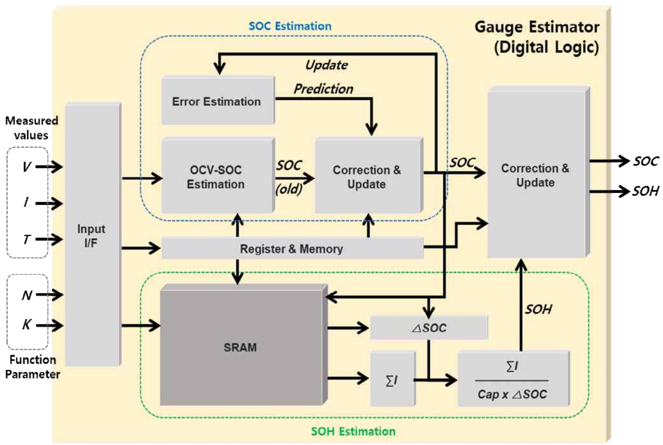

Figure 1. Architecture of the proposed SOC and SOH estimation block

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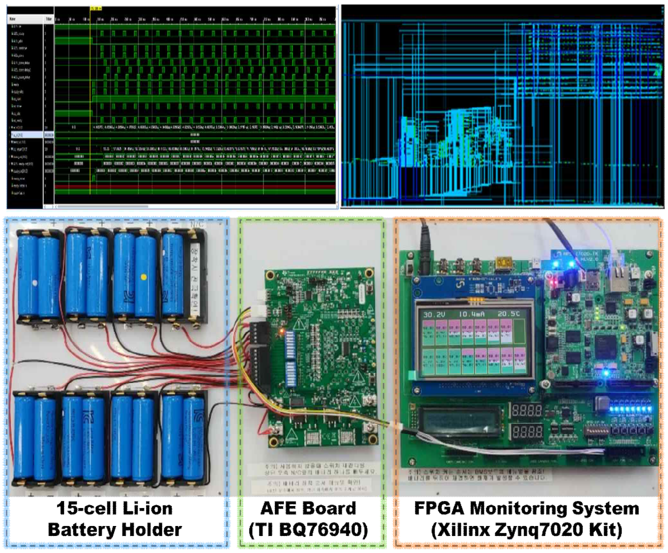

Figure 2. FPGA testbed for battery monitoring system

For the implementation and verification of the designed IP, a real-time multi-cell lithium-ion battery monitoring system was implemented, as shown in Figure 2. The FPGA-implemented system for real-time multi-cell Li-ion battery SOC monitoring is divided into three main parts: the multi-cell battery holder, the analog front end (AFE) board, and the digital FPGA board. The battery holder is designed to cover up to 15 lithium-ion battery cells according to the AFE board, TI BQ76940 module, which can monitor multi-cell battery status in real time. The main algorithm for estimating multi-cell SOC and SOH is implemented on a digital processing board with ZYNQ-7020 FPGA chip and peripherals including TFT-LCD. With the designed system, real-time battery simulation can be performed, and monitoring output including real-time battery status can be expressed in TFT-LCD. The system was implemented to have a delay time within about 100 ms from sensing to LCD power, and it was designed to demonstrate the estimation performance within 5%.

B. *Performance Evaluation*

The performance evaluation results of the SOC and SOH estimation are presented in Figure 3. The current and voltage was set up according to the EV simulation environments as dynamic stress (DST) cycle with 10ms sampled. The simulation was performed for 8x10^5 samples, it is around 2 minutes in real-time. In a given simulation environment, the estimation results of SOC and SOH are shown together with the real answers.

For the SOC estimation performance, the simulation was performed that the SOC was repeatedly decreased or increased. As a long term of simulation, our estimation block can predict the SOC value instantly with an error under 2%. For the SOH estimation performance, the simulation was performed with SOH set to 50%, and initial estimated SOH is 100%. For the stable output, because we adopt the smoothing filter, it takes time to converge about 3x10^5 times, which means 50 minutes for 10ms sampling. But once it converges, the error stays within 5%.

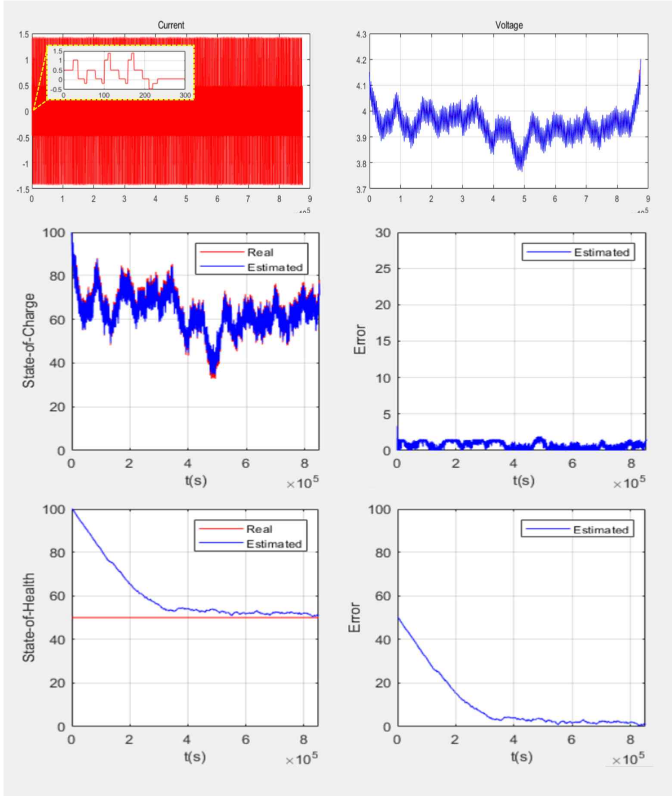

Figure 3. The evaluation result of proposed SOC and SOH estimation block

IV. Conclusion

In this paper, we cover the hardware design and FPGA implementation of block IP for the estimation of SOC and SOH, the main functions of BMS, which have been studied a lot recently. The designed block accurately estimates the SOC and SOH with 2% and 5%, respectively, and was implemented on FPGA testbed with 15 cells to verify the block IP. The real-time estimation result can be shown through display.

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