Report generated on 2023-07-03 13:53 GMT by riscof v

Environment

Riscof Version	1.25.3
Riscv-arch-test Version/Commit Id	-
DUT	pcore
Reference	sail c simulator
ISA	RV32IM
User Spec Version	2.3
Privilege Spec Version	1.10

Yaml

Show all details / Hide all details

Name
/home/user/Work/UETRV-PCore/verif/riscof_work/pcore_isa_checked.yaml *(show details)*
/home/user/Work/UETRV-PCore/verif/riscof_work/pcore_platform_checked.yaml *(show details)*

Please visit YAML specifications for more information.

Summary

☑ 38Passed, ☑ 0Failed

Results

Show all details / Hide all details

Test	Result	Path
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/add-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/add-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/addi-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/addi-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/and-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/and-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/andi-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/andi-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/auipc-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/auipc-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/beq-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/beq-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/bge-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/bge-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/bgeu-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/bgeu-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/blt-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/blt-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/bltu-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/bltu-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/bne-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/bne-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/fence-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/fence-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/jal-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/jal-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/jalr-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/jalr-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/lb-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/lb-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/lbu-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/lbu-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/lh-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/lh-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/lhu-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/lhu-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/lui-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/lui-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/lw-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/lw-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/or-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/or-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/ori-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/ori-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sb-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sb-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sh-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sh-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sll-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sll-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/slli-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/slli-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/slt-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/slt-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/slti-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/slti-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sltiu-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sltiu-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sltu-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sltu-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sra-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sra-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/srai-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/srai-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/srl-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/srl-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/srli-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/srli-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sub-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sub-01.S

Test	Result	Path
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/sw-align-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/sw-align-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/xor-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/xor-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/I/src/xori-01.S	Passed *(show details)*	/home/user/Work/UETRV-PCore/verif/riscof_work/src/xori-01.S