

Report generated on 2023-07-03 13:54 GMT by [riscov](#) v

Environment

Riscof Version	1.25.3
Riscv-arch-test Version/Commit Id	-
DUT	pcore
Reference	sail c simulator
ISA	RV32IM
User Spec Version	2.3
Privilege Spec Version	1.10



Yaml

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Name
/home/user/Work/UETRV-PCore/verif/riscof_work/pcore_isa_checked.yaml <i>(show details)</i>
/home/user/Work/UETRV-PCore/verif/riscof_work/pcore_platform_checked.yaml <i>(show details)</i>

Please visit [YAML specifications](#) for more information.

Summary

 8Passed,  0Failed

Results

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▼ Test	▲ Result	Path
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/div-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/div-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/divu-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/divu-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/mul-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/mul-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/mulh-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/mulh-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/mulhsu-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/mulhsu-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/mulhu-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/mulhu-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/rem-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/rem-01.S
/home/user/Work/Tests/riscv-test-suite/rv32i_m/M/src/remu-01.S	Passed <i>(show details)</i>	/home/user/Work/UETRV-PCore/verif/riscof_work/src/remu-01.S