



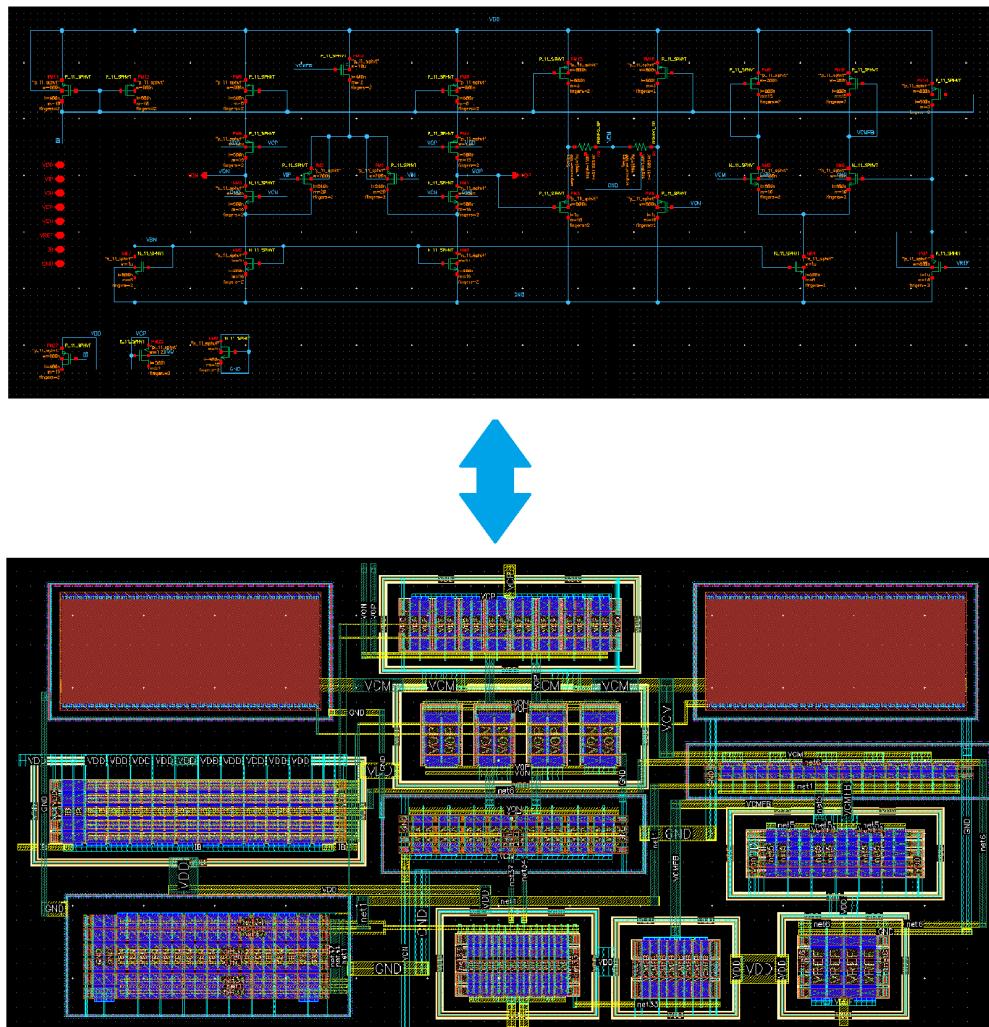
Ministry of Communications
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CENTER OF
NANOELECTRONICS
& DEVICES

Design and Layout of Fully-Differential Folded Cascode OTA with CMFB



*This is the submission of the Final project of the subject:
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1. Introduction

1.1. Circuit theory [1]

In amplifier topologies, the cascade of a CS stage and a CG stage is called cascode topology, as shown in figure 1.1.

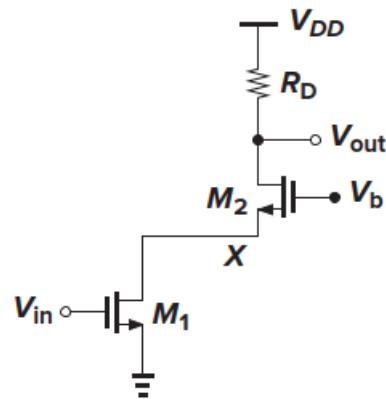


Figure 1.1: Cascode stage

The advantages of cascode topology over a simple CS stage are:

- isolate i/p from o/p, hence reducing the Miller effect and increasing stability in feedback systems.
- increase the gain.

Output Resistance: An important property of the cascode structure is its high output impedance. As illustrated in figure 1.2 below, for the calculation of R_{out} , the circuit can be viewed as a common-source stage with a degeneration resistor equal to r_{O1} .

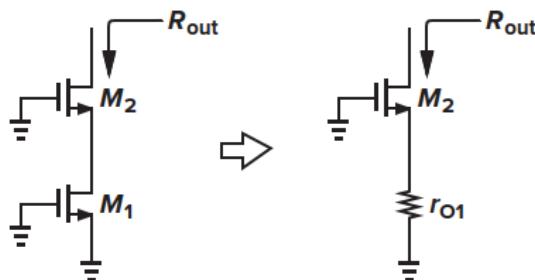


Figure 1.2: Calculation of output resistance of cascode stage

Thus, $R_{out} = [1 + (g_{m2} + g_{mb2}) r_{O2}] r_{O1} + r_{O2}$

Assuming $g_m r_O \gg 1$, we have $R_{out} \approx (g_{m2} + g_{mb2}) r_{O2} r_{O1}$.

That is, M2 boosts the output impedance of M1 by a factor of $(g_{m2} + g_{mb2}) r_{O2}$.

Applying it to differential amplifier, we see that a fully differential telescopic opamp shown in figure 1.3, suffers from limited output swing, then the input CM level and the bias voltages V_{b1} and V_{b2} must be chosen to allow maximum output swings.

The minimum allowable input CM level equals $V_{GS1} + V_{OD9} = V_{TH1} + V_{OD1} + V_{OD9} = 1.4V$. The minimum value of V_{b1} is given by $V_{GS3} + V_{OD1} + V_{OD9} = 1.6V$, placing M1-M2 at the edge of the triode region.

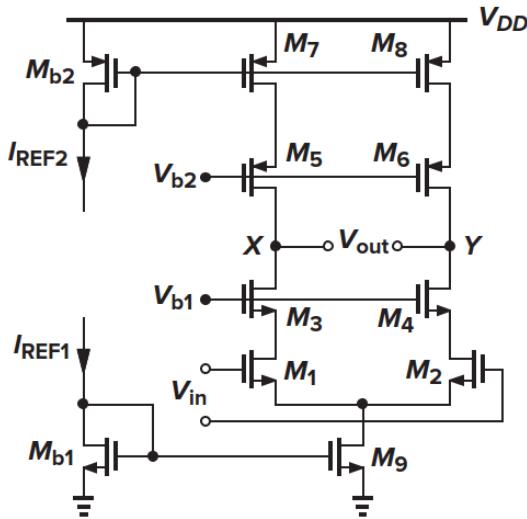


Figure 1.3: Fully Differential Telescopic opamp

Similarly, $V_{b2max} = V_{DD} - (|V_{GS5}| + |V_{OD7}|) = 1.7V$. In practice, some margin must be included in the value of V_{b1} and V_{b2} to allow for process variations. Also, the increase in the threshold voltages due to body effect must be considered.

In order to alleviate the drawbacks of telescopic cascode op amps, namely, limited output swings and difficulty in choosing equal input and output CM levels, a “folded-cascode” op amp can be used. A folded cascode op amp is applied in an NMOS or PMOS cascode amplifier, where the input device is replaced by the opposite type while still converting the input voltage to a current, as shown in figure 1.4.

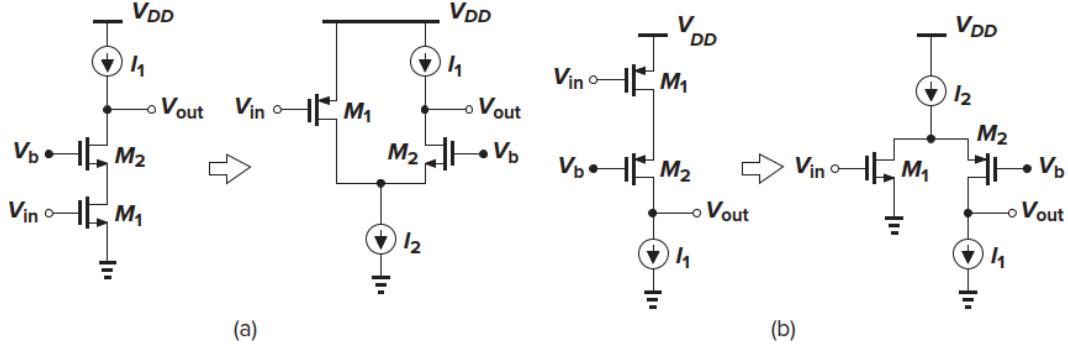
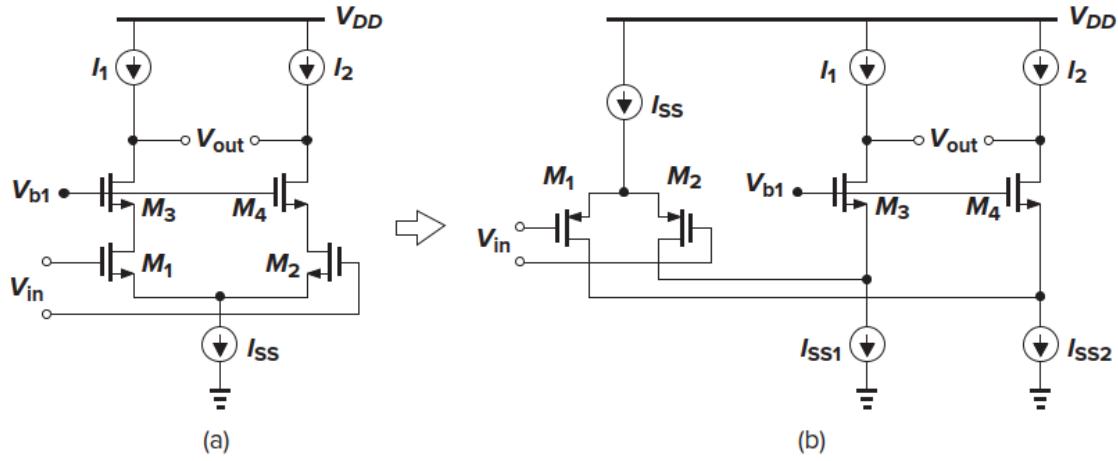


Figure 1.4: Folded-cascode amplifiers

The small-signal current generated by M1 flows through M2 and subsequently the load, producing an output voltage approximately equal to $(g_{m1})(R_{out})(V_{in})$. The primary advantage of the folded structure lies in the choice of the voltage levels because it does not “stack” the cascode transistor on top of the input device.



(a) Telescopic and (b) folded-cascode op amp topologies.

Figure 1.5: Telescopic and Folded Topologies

Note two important differences between the two circuits.

1. In figure 1.5 (a), one bias current, I_{SS} , provides the drain current of both the input transistors and the cascode devices, whereas in (b), the input pair requires an additional bias current. In other words, $I_{SS1} = I_{SS}/2 + I_{D3} = I_{SS}/2 + I_1$. Thus, the folded-cascode configuration generally consumes more power.
2. In (a), the input CM level cannot exceed $V_{b1} - V_{GS3} + V_{TH1}$, whereas in (b), it cannot be less than $V_{b1} - V_{GS3} - |V_{THP}|$. It is therefore possible to design the latter to allow shorting its input and output terminals with negligible swing limitation.

Let us now calculate the maximum output voltage swing of the folded-cascode op amp shown in figure 1.6.

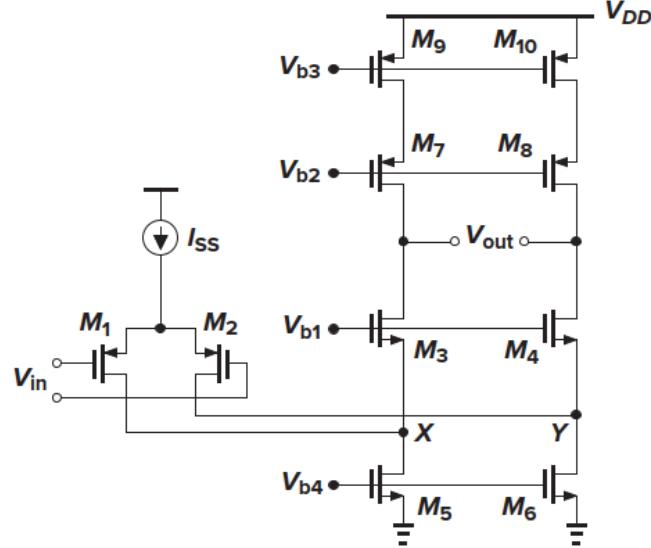
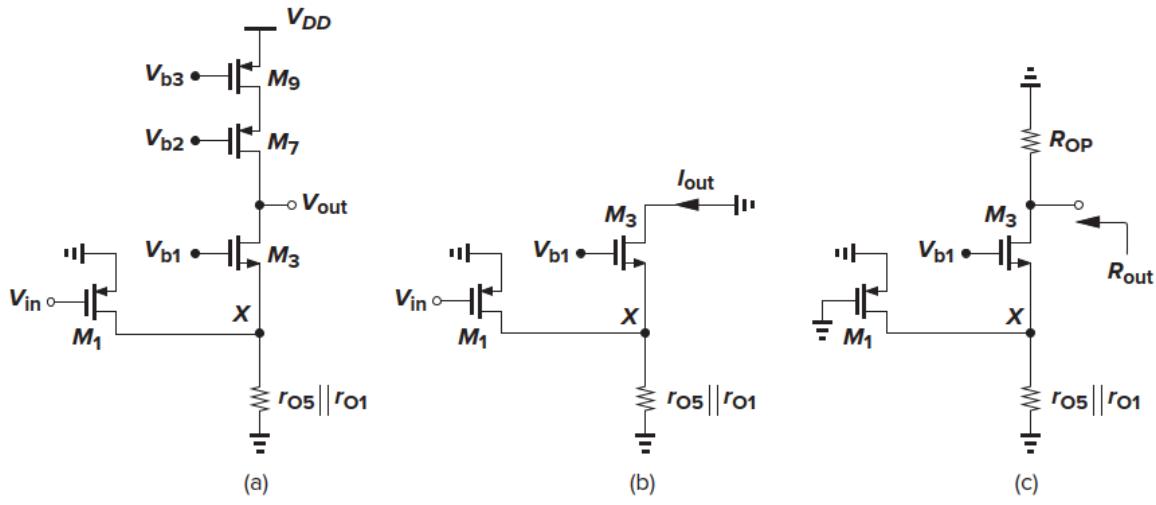


Figure 1.6: Folded-cascode op amp with cascode PMOS loads

Where M5-M10 replace the ideal current sources of the previous figure. With the proper choice of V_{b1} and V_{b2} , the lower end of the swing is given by $V_{OD3} + V_{OD5}$ and the upper end by $V_{DD} - (|V_{OD7}| + |V_{OD9}|)$. Thus, the peak-to-peak swing on each side is equal to $V_{DD} - (V_{OD3} + V_{OD5} + |V_{OD7}| + |V_{OD9}|)$. In the telescopic cascode, on the other hand, the swing is less by the overdrive of the tail current source. We should nonetheless note that carrying a large current, M5 and M6 in the figure above may require a high overdrive voltage if their capacitance contribution to nodes X and Y is to be minimized.

We now determine the small signal voltage gain of the folded-cascode op amp. Using the half circuit depicted in figure 1.7 (a) and writing $|A_v| = (G_m)(R_{out})$, we must calculate G_m and R_{out} .



(a) Half circuit of folded cascode op amp, (b) equivalent circuit for G_m calculation, and (c) equivalent circuit for R_{out} calculation.

Figure 1.7: Calculating small-signal voltage gain of the folded-cascode op amp

As shown in figure 1.7 (b), the output short circuit current is approximately equal to the drain current of M1 because the impedance seen looking into the source of M3, that is, $(g_{m3} + g_{mb3}) - r_{O3}$, is typically much lower than $r_{O1}r_{O5}$. Thus, $G_m = g_{m1}$. To calculate R_{out} , we use (c), with $R_{OP} = (g_{m7} + g_{mb7})r_{O7}r_{O9}$, to write $R_{out} = R_{OP}[(g_{m3} + g_{mb3})r_{O3}(r_{O1}r_{O5})]$.

It follows that $|A_v| = g_{m1}[(g_{m3} + g_{mb3})r_{O3}(r_{O1}r_{O5})][(g_{m7} + g_{mb7})r_{O7}r_{O9}]$

A folded-cascode op-amp may incorporate NMOS input devices and PMOS cascode transistors. Such a circuit potentially provides a higher gain than the op-amp of PMOS input devices and NMOS cascode transistors, because of the greater mobility of NMOS devices, but at the cost of lowering the pole at the folding points.

Summary: Our review thus far suggests that the overall voltage swing of a folded-cascode op amp is only slightly higher than that of a telescopic configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain, lower pole frequencies, and higher noise. Nonetheless, folded-cascode op amps are used more widely for two reasons: (1) their input and output CM levels can be chosen equal without limiting the output swings, and (2) compared to telescopic cascodes, they can accommodate a wider input CM range.

1.2. Required Specifications

Design and simulate:

1. Fully differential folded-cascode OTA
2. Common mode feedback circuit for the FCOTA

achieving the following specifications:

Specifications			
Supply Voltage	1.2 V	Closed Loop Gain	2
Phase Margin	$\geq 70^\circ$	Closed Loop BW	10 MHz
Differential Output Swing	$\geq 0.6 \text{ V pk - to - pk}$	OTA Current Consumption	$\leq 80 \mu\text{A}$
CM Input Range	$0 < \text{CM} \leq 0.6 \text{ V}$	CMFB Current Consumption	$\leq 40 \mu\text{A}$
Capacitance Load	1 pF	DC Loop Gain	50 dB

FCOTA schematic:

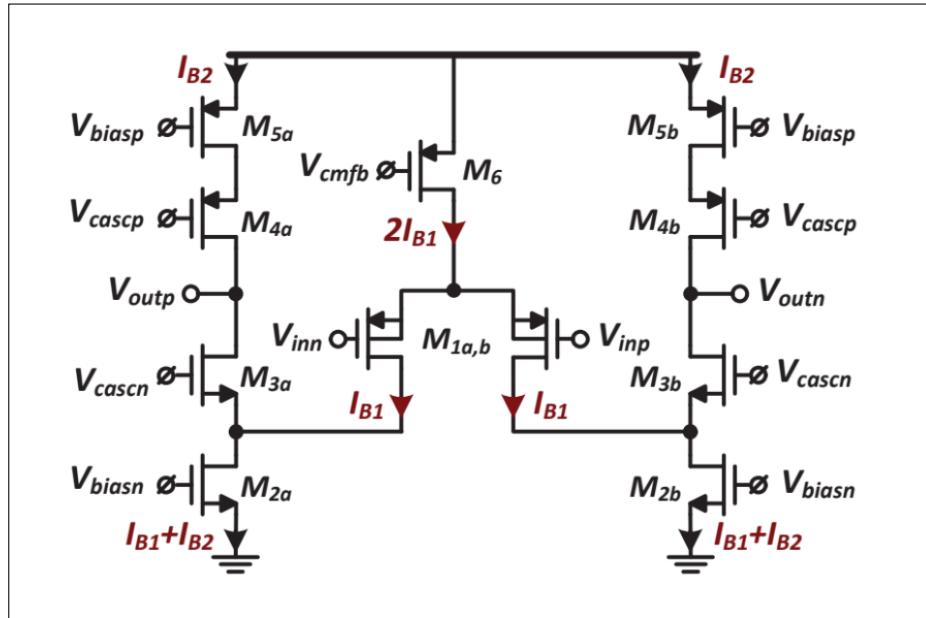


Figure 1.8: FCOTA schematic

CMFB schematic:

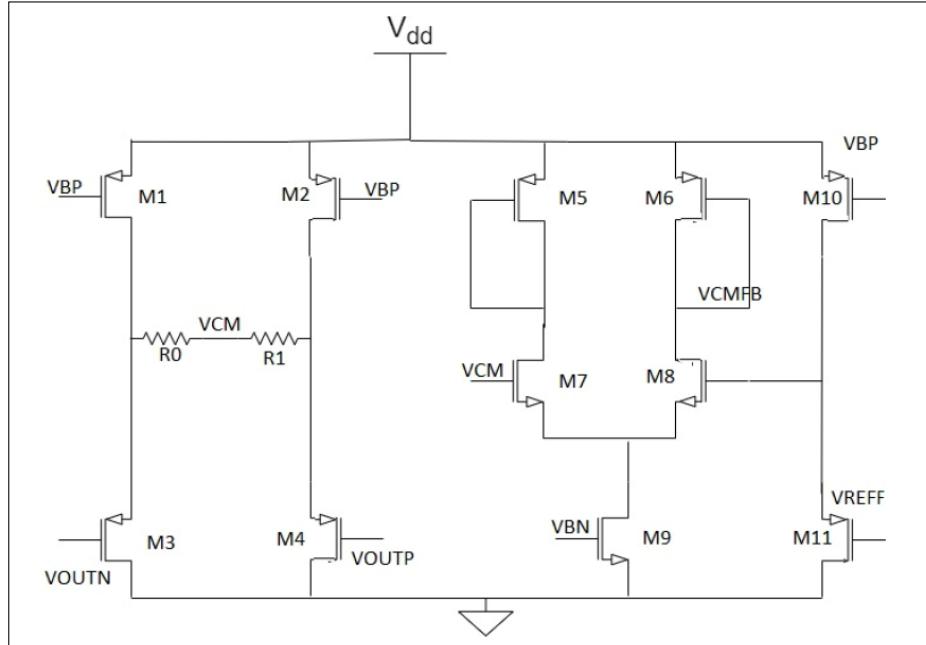


Figure 1.9: CMFB schematic

1.3. Required Deliverables

- Hand analysis calculation from specifications to sizing parameters for FC and CMFB circuits.
- Snap of the final schematic including the optimized dimensions of the proposed devices.
- Table of DC operating points for both designs.
- Snaps of AC results that show the optimized Gain and phase margins.
- Stability result.
- Result for a sinusoidal input signal by plotting the spectrum with comment.
- The floor planning for design with matching patterns for each block.
- Snap of the FCOTA layout.
- The result of verification analyses (clean DRC and LVS).
- Post layout simulations for all pre-layout results with comments on results.
- Library files submission.

1.4. PDK and Tools

- PDK: umc65sp, metal option: 1P10M2T2F0U-option19
- Tools: Cadence (Virtuoso - ADE Explorer) and Calibre.

2. FCOTA Design

2.1. FCOTA sizing

2.1.1. Hand Analysis [2] , [3]

1. Calculating I_d from max power constraint: Since maximum power consumption to the FCOTA is constrained to be $80\mu A$ at most, then we have to have $I_{b1} + I_{b2} \leq 40\mu A$, where I_{b1} is the current passing through the input devices M1 and I_{b2} is the current passing through the cascode devices M5 through M3. (note that this is different from the annotation in the schematic above)

To choose the split ratio between I_{b1} and I_{b2} , we used [5] to assume $S = 1.5$.

As [5] concluded that:

- using $S > 1$ can improve the amplifier DC gain, bandwidth, and noise.
- using $S \approx 2-3$ can lead to an overall significant improvement in bandwidth and settling time, for continuous-time analog signal processing and bias circuits.
- using $S \approx 1.1 - 1.2$ may be optimum, for circuits that suffer from frequent large output excursions, but higher S may cause significant asymmetrical slewing.
- using $S < 1$ does not seem to provide any favorable behavior, aside from a small improvement in PM.

Hence, we chose to go in the middle and choose $S = 1.5$, $I_{b1} = 1.5 I_{b2}$.

Since: max current consumption $\leq 80\mu A$ Therefore: $I_{b1} + I_{b2} \leq 40\mu A$ Therefore: $1.5I_{b2} + I_{b2} \leq 40\mu A$

Therefore: $I_{b1} = 24\mu A$ and $I_{b2} = 16\mu A$

2. Choosing L and gm/ I_d guided by the reference's experience

- For the input pair: we will use short $L = 240nm$ and $gm/ID = 15$. This maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG).
- For the current source transistors use relatively long L and bias them in SI. $L = 600nm$ and $gm/ID = 10$. These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the noise.

- For the cascode transistors use $L = 500\text{nm}$ and $\text{gm}/\text{ID} = 15$. These transistors do not contribute significant offset and noise, so they don't need to be large. A large gm helps the gain and doesn't increase the noise.

3. Calculating V_{CASCN} and V_{CASCP}

- $V_{CASCN} \approx V_{GSN} + V^* = 418m + 200m = 618mV$
- $V_{CASCP} \approx V_{DD} - |V_{GSP}| - V^* = 1.2 - 428m - 200m = 572mV$

2.1.2. FCOTA Schematic

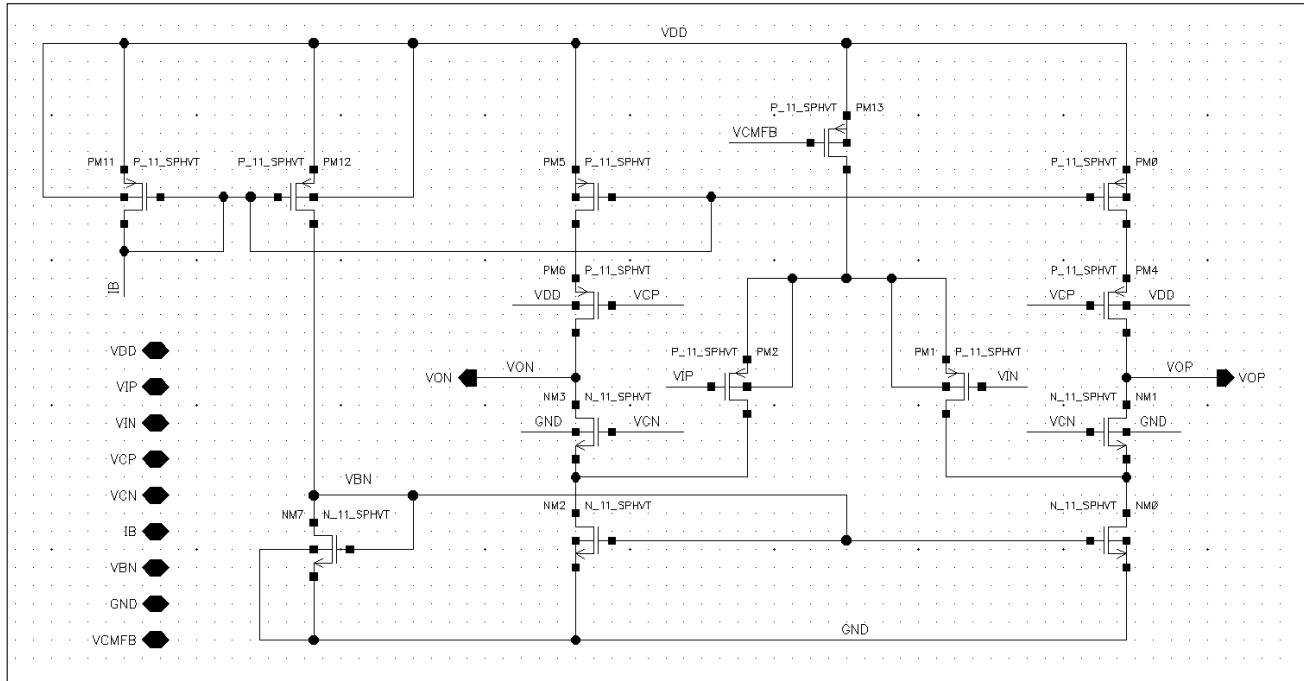


Figure 2.1: FCOTA Schematic

2.1.3. Sizing using the gm/Id methodology

Now we generate the following charts (g_m/g_{ds} - I_d/W - g_m/C_{gg} - V_{gs}) from the simulator for pmos and nmos to size the mosfets through g_m/I_d method: NMOS:

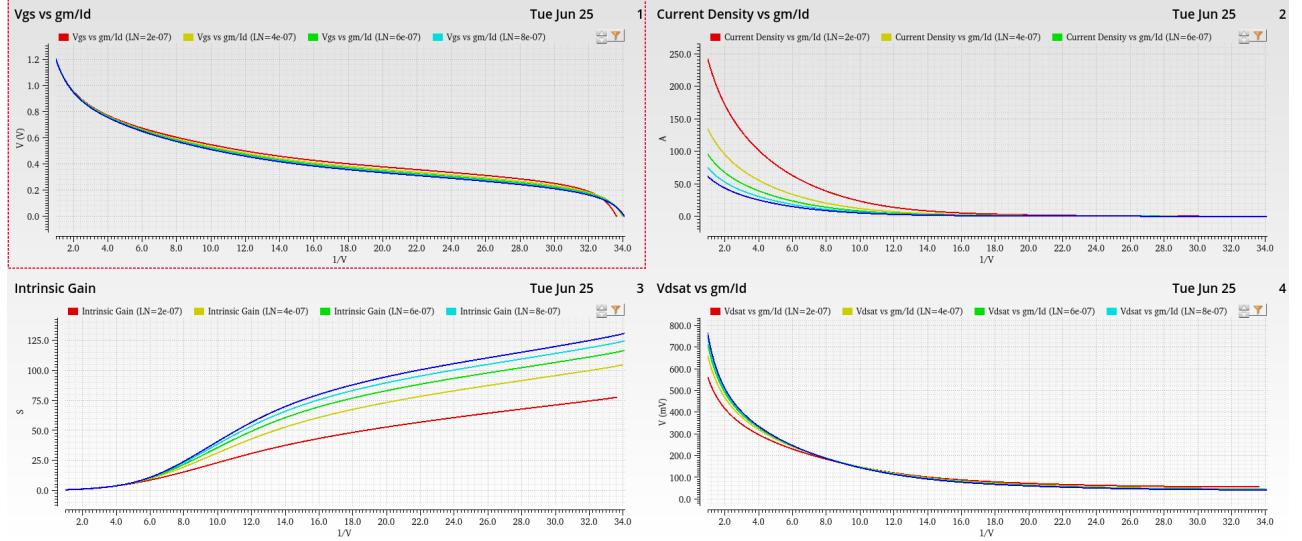


Figure 2.2: nmos g_m/I_d

PMOS:

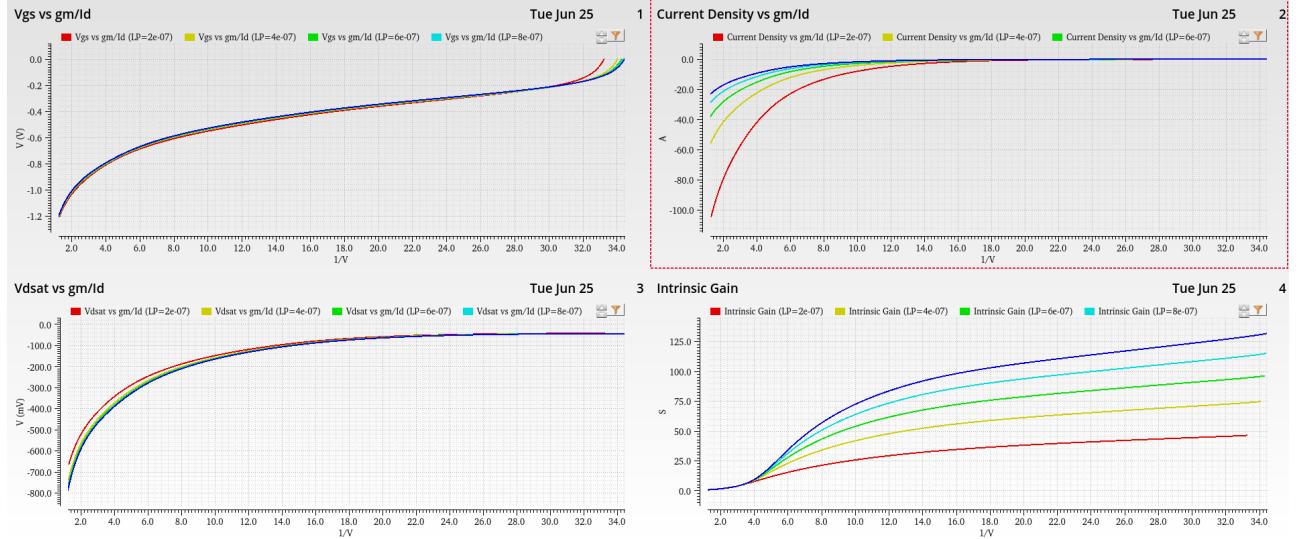


Figure 2.3: pmos g_m/I_d

From the assumed L and g_m/I_d we use the charts to find the widths of all transistors. After running DC analysis, we find some specifications are not met, and some mosfets are out of saturation, so we tune the widths of cascode, input diff pair and diff bias. Also we tune the biasing voltages for the cascodes and g_m/I_d of n biasing, resulting in the final sizes shown below.

2.1.4. Final proposed sizes

I_d and g_m/I_d are assumed, W and L are actual. All devices are in saturation.

#	Name	Function	I_d (uA)	g_m/I_d (s/A)	L (n)	W (u)
1	PM1,2	input diff pair	24	15	240	14
2	NM0,2	n-biasing	40	14	600	15.6
3	NM1,3	n-cascode	16	15	500	5.6
4	PM4,6	p-cascode	16	15	500	17.5
5	PM0,5	p-biasing	16	10	600	6
6	PM13	diff pair biasing	48	10	450	14
7	NM7	n-tail current	20	10	600	8
8	PM12	p-tail current	20	10	600	7
9	PM11	I ref	20	10	600	7

Table 2.1: Sizes - Behav CMFB

2.2. FCOTA Open-Loop Simulation (Behavioral CMFB)

2.2.1. Behavioral CMFB schematic

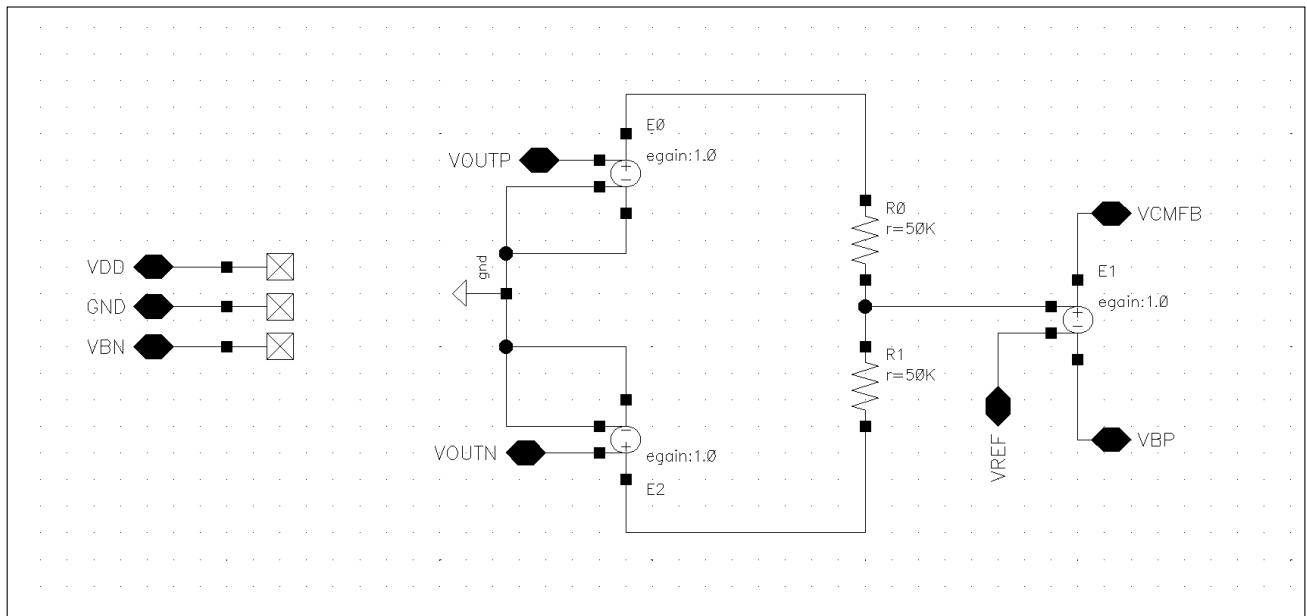


Figure 2.4: Behavioral CMFB schematic

2.2.2. Test Bench assembly

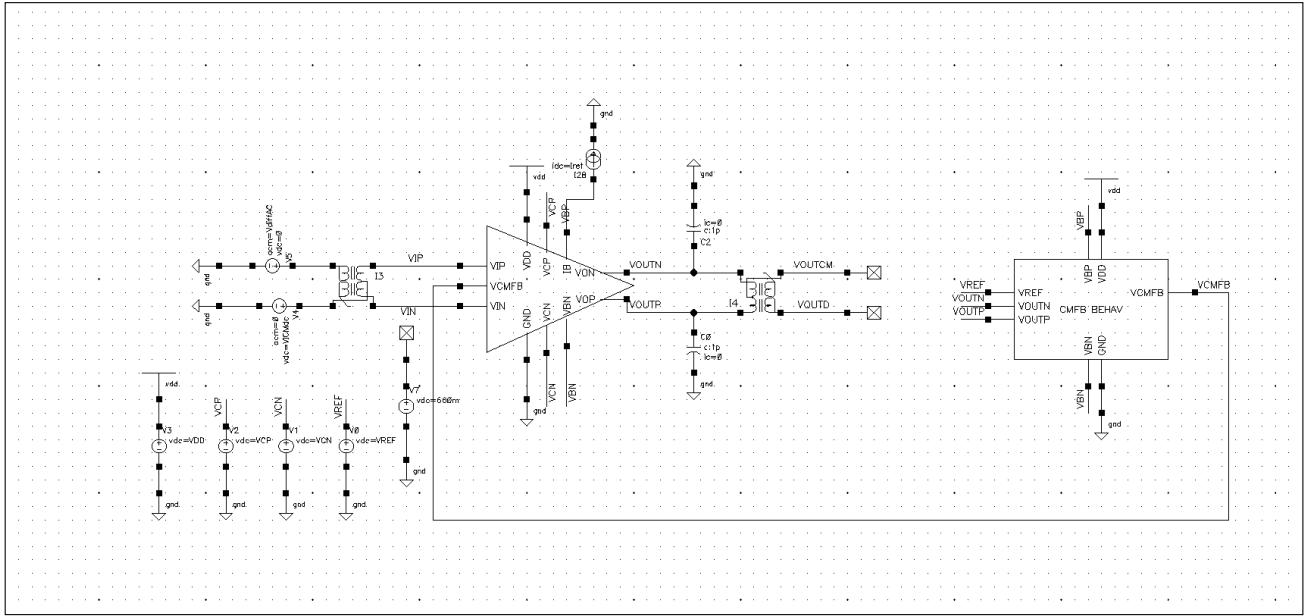


Figure 2.5: Open loop test bench with Behavioral CMFB

With the following variable values:

Design Variables	
Iref	20u
VCN	645m
VCP	545m
VDD	1.2
VREF	500m
VdiffAC	1
VICMdc	300m
Lcm	600n
Lcmfb	600n

Figure 2.6: Open loop test bench with Behavioral CMFB

V_{ICM} is set at the middle of the CMIR. V_{REF} is set to maximize the symmetrical output swing.

Since Max. Swing $\frac{1}{2} \times (V_{dd} - 2V^* - V_{ocm})$ $0.6 = 2 \times (1.2 - 0.4 - V_{ocm})$ $0.3 = 0.8 - V_{ocm}$
 $V_{ocm} = 500mV$ Therefore: $V_{ref} = 500mV$

2.2.3. DC Analysis

Main DC op points (id, vgs, vth, gmoverid, region) annotated:

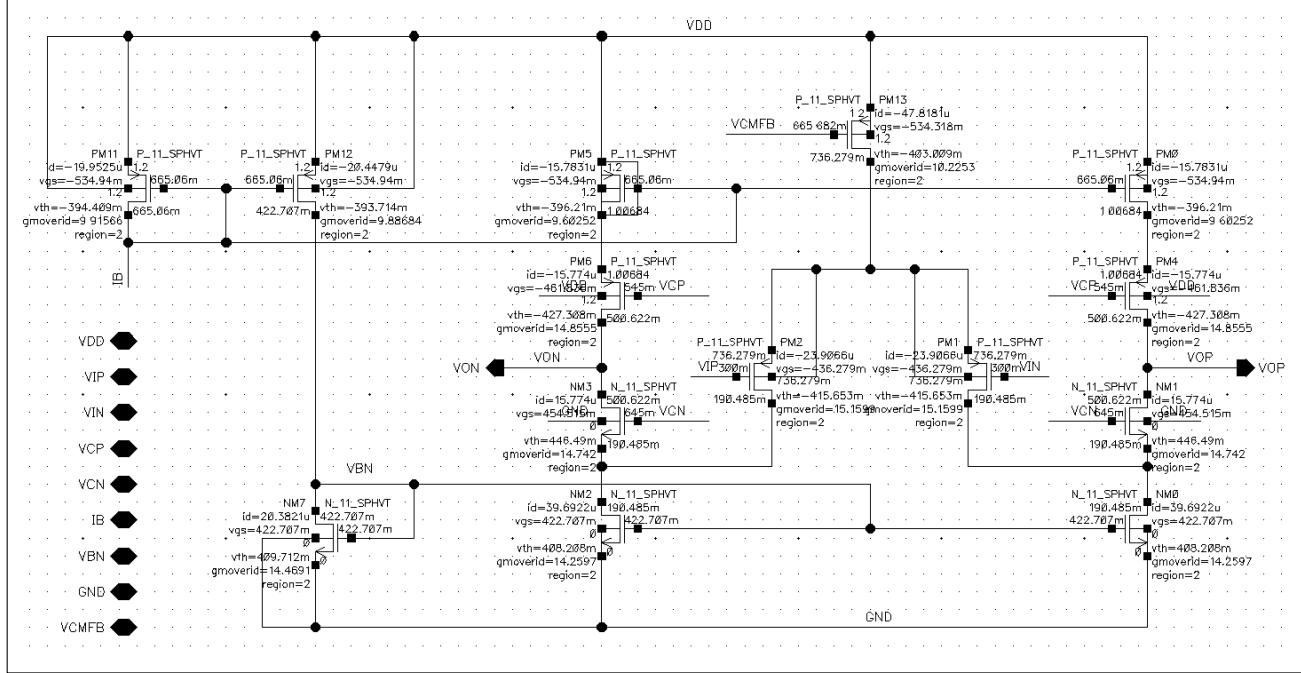


Figure 2.7: FCOTA main dc operating points

All DC op points (id, vgs, vds, vdsat, vth, gm, gds, gmoverid, region) displayed through the info balloons for each device:

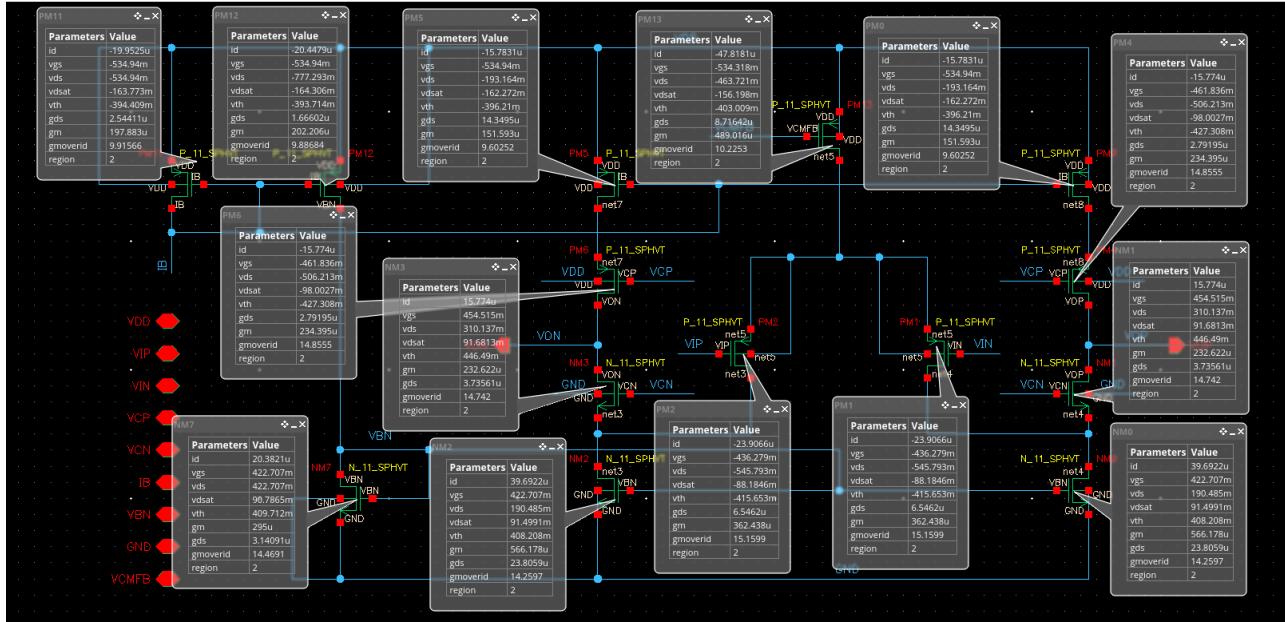


Figure 2.8: FCOTA all dc operating points

Table 2.2: All DC operating points

Comparing assumed Id and gm/Id with actual results:

#	Name	Function	assumed I_d (uA)	actual I_d (uA)	assumed g_m/I_d (s/A)	actual g_m/I_d (s/A)
1	PM1,2	input diff pair	24	23.9	15	15.16
2	NM0,2	n-biasing	40	39.69	14	14.25
3	NM1,3	n-cascode	16	15.77	15	14.74
4	PM4,6	p-cascode	16	15.77	15	14.85
5	PM0,5	p-biasing	16	15.78	10	9.6
6	PM13	diff pair biasing	48	47.81	10	10.22
7	NM7	n-tail current	20	20.38	10	14.46
8	PM12	p-tail current	20	20.44	10	9.88
9	PM11	I ref	20	19.95	10	9.9

Sizes annotated:

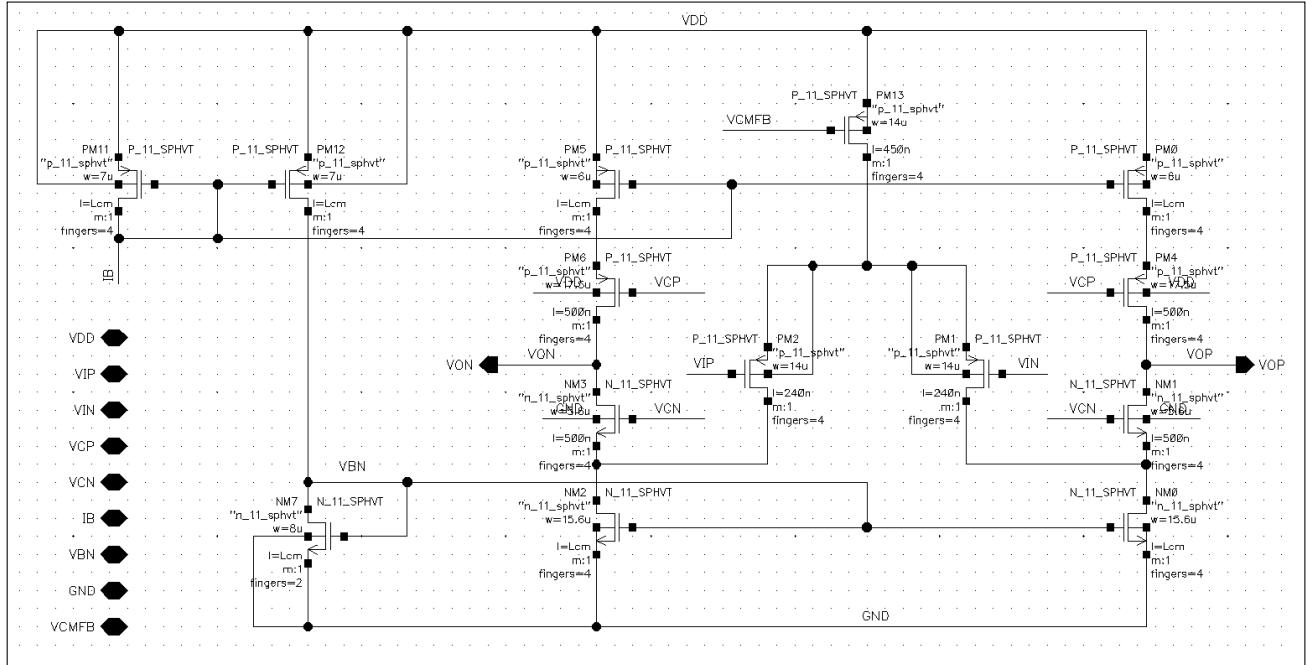


Figure 2.9: FCOTA sizes annotated

Comment:

- We see all results are close with accepted tolerance, except for n-tail current, g_m/I_d was increased from 10 to 14 to meet the specifications.
- Also current consumption is met : $79.38\mu A < \text{max current consumption: } 80\mu A$
- All devices are in saturation.

2.2.4. AC Analysis

Settings: 1Hz:10GHz, logarithmic, 10 points/decade. with the same test bench.

Name	Type	Details	Value
Ao_dB	expr	dB20(ymax(mag(VF"/VOUTD"))))	56.13
Ao	expr	ymax(mag(VF"/VOUTD"))))	640.4
BW	expr	bandwidth(VF"/VOUTD") 3 "low")	80.16K
GBW	expr	(Ao * BW)	51.33M
fu	expr	unityGainFreq(VF"/VOUTD")	51.64M

Figure 2.10: AC Analysis calculations

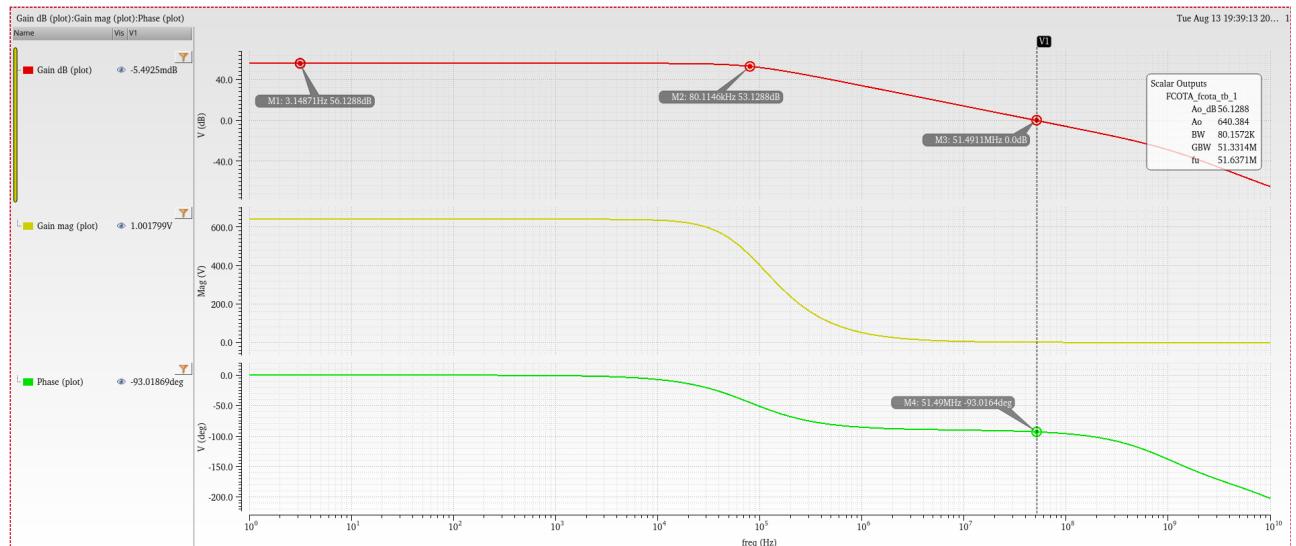


Figure 2.11: Plotting Open-loop Gain and phase margin

We see that: The Open loop gain meets the requirement $> 56\text{dB}$ The Phase margin meets the requirement > 70 degree

3. CMFB Design

3.1. CMFB Sizing

3.1.1. CMFB Practical Design Aspects

Since the CMFB tunes 20% of the diff pair, then there is no need for high accuracy in the value of the CMFB control signal. Hence the error signal is not required to have high accuracy. Also, since error signal is inversely proportional to the DC Loop Gain, then the DC LG doesn't need to be high.

Ideally, the CMFB bandwidth should be close to the OTA bandwidth to recover quickly from the common mode disturbance, however this means high power consumption.

Here, the power budget for the CMFB circuit is 40uA. We choose to distribute them unequally among the branches, where the differential pair transistors were designed to get higher current to increase the differential input range and avoid full-steering of the current [11 uA was chosen for each branch of the differential pair and 6 uA in the other branches].

Lengths of all bias devices are set to 600n as they are connected to the same current mirror. Lengths of sensing devices and the buffer are assumed 1u. g_m/I_d is assumed to be 15 for the current sensor input, Diff pair bias and the Buffer. Rest devices are assumed to have $g_m/I_d = 10$. This was based on reference experience + trial to reach saturation for all devices.

The sensing resistors are chosen such that the max current flowing through them (when diff signal is max) is less than the CD bias current. This avoids starving the CD when the diff output signal has its maximum excursion.

The value of sensing resistors were chosen to sink at most 33% of the buffer bias current:
 $0.6/2 \times R_{sen} < 1/3 \times 6 \times 10^{-6} \rightarrow R_{sen} = 150k\Omega$

Using previous gm/Id charts and the assumed Length and Id we get the widths for all devices as in the table below.

3.1.2. Final proposed sizes

I_d and g_m/I_d are assumed, W and L are actual. All devices are in saturation.

#	Name	Function	I_d (uA)	g_m/I_d (s/A)	L (n)	W (u)
1	PM0,1	Current Sensor Bias	6	10	600	2
2	PM2,3	Current Sensor Input	6	15	1000	8
3	PM4,5	Diff Pair Load	11	10	600	3
4	NM0,1	Diff Pair	11	10	600	1.5
5	NM2	Diff Pair Bias	22	15	600	8.4
6	PM8	Buffer Bias	6	10	600	2
7	PM7	Buffer	6	15	1000	8

Table 3.1: CMFB final proposed sizes

3.2. FCOTA Open-Loop Simulation (Actual CMFB)

3.2.1. CMFB Schematic

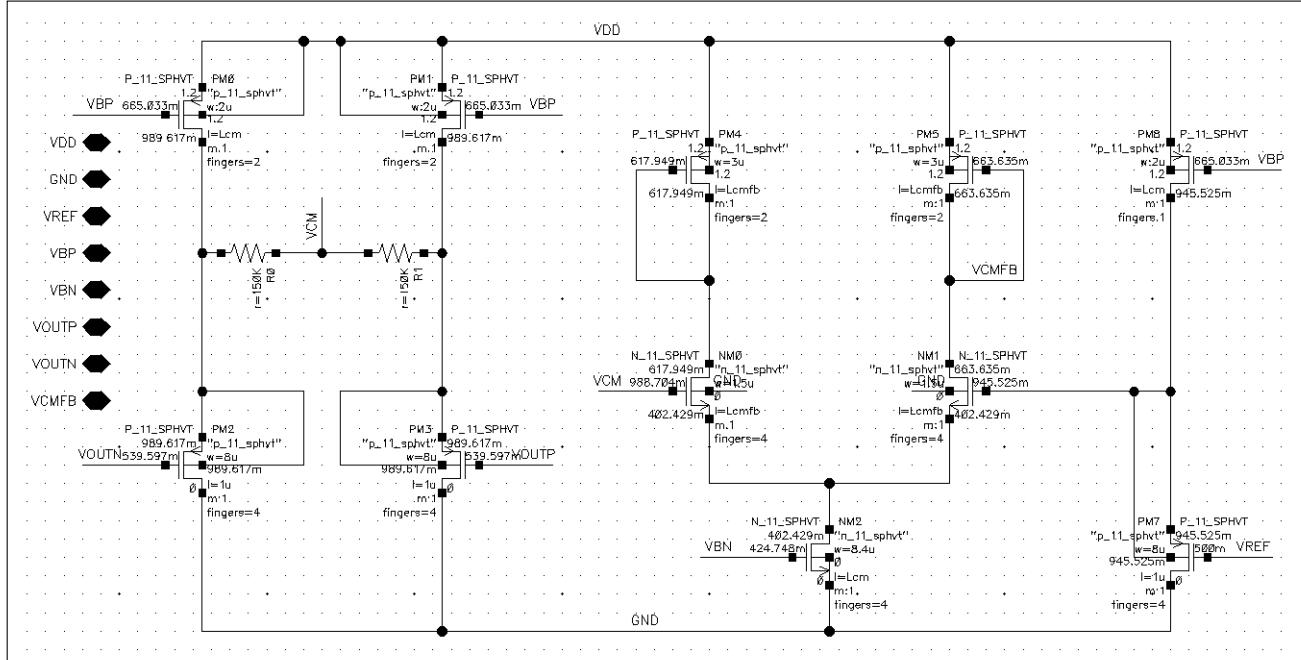


Figure 3.1: FCOTA sizes annotated

3.2.2. Test Bench

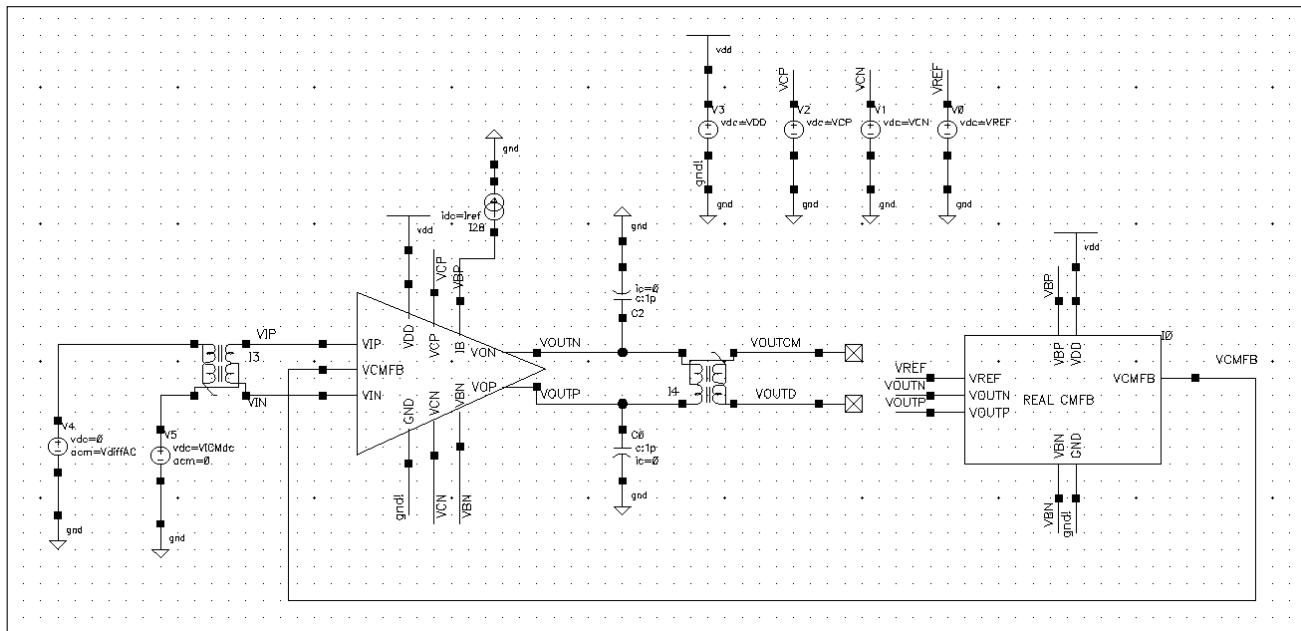


Figure 3.2: FCOTA sizes annotated

3.2.3. DC Analysis

Main DC op points (id, vgs, vth, gmoverid, region) annotated:

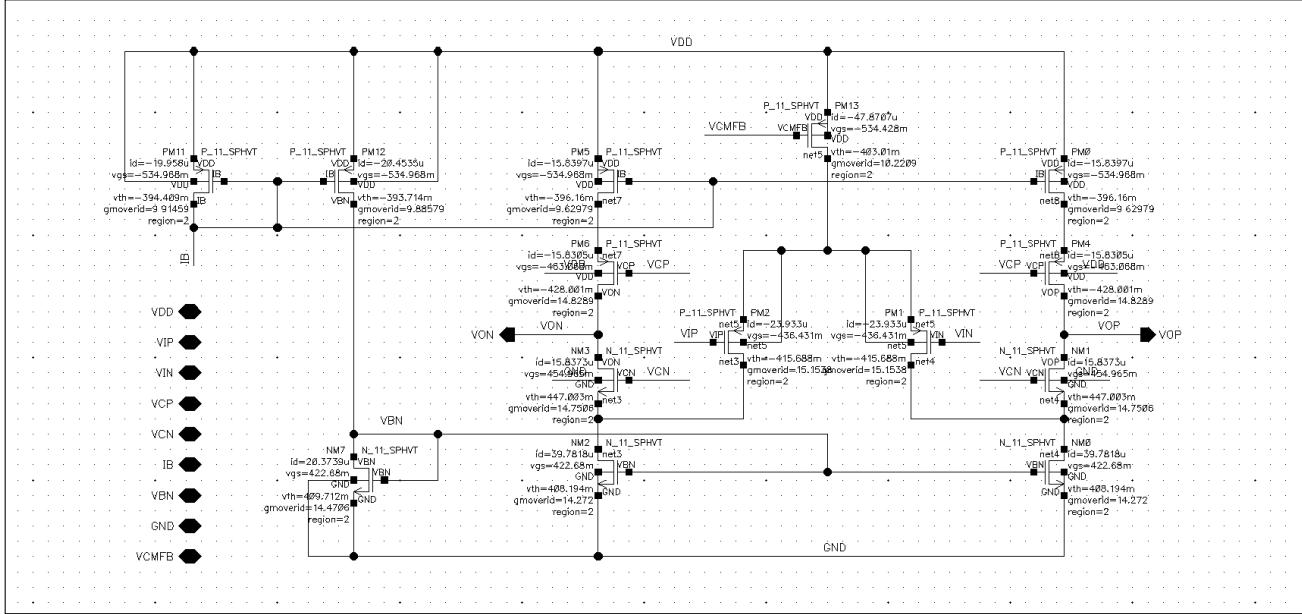


Figure 3.3: FCOTA main DC operating points after adding real CMFB

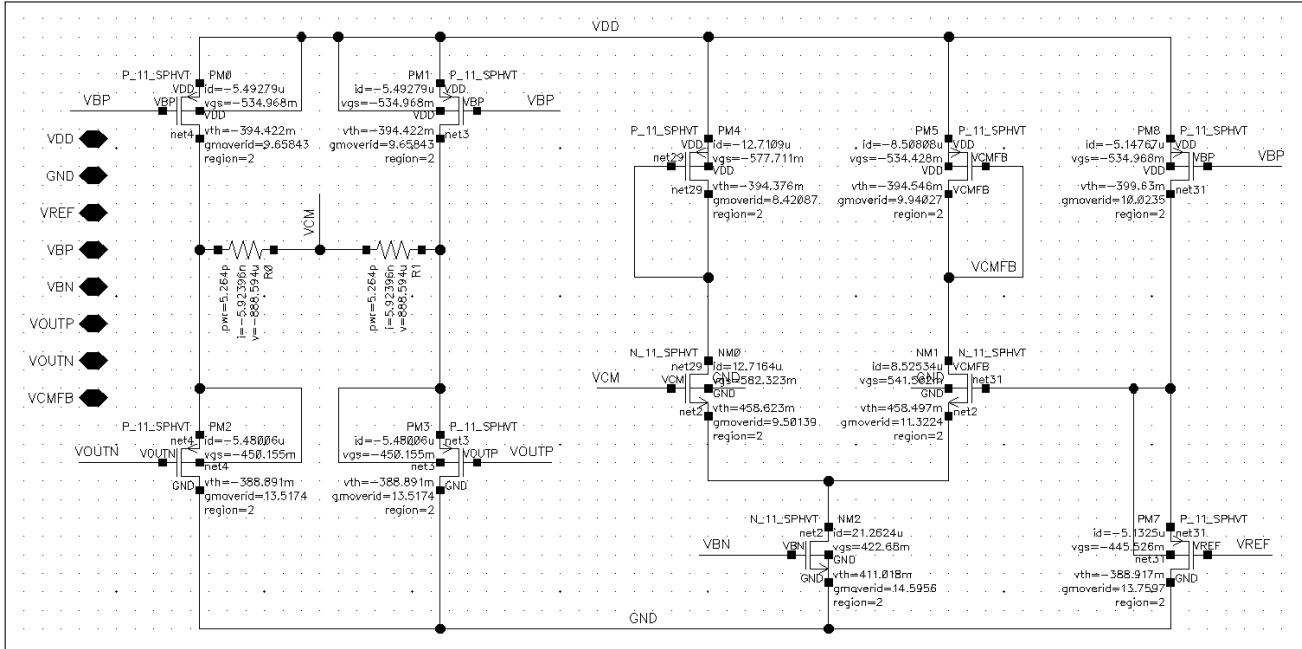


Figure 3.4: CMFB main DC operating points

All DC op points (id, vgs, vds, vdsat, vth, gm, gds, gmoverid, region) displayed through the info balloons for each device:

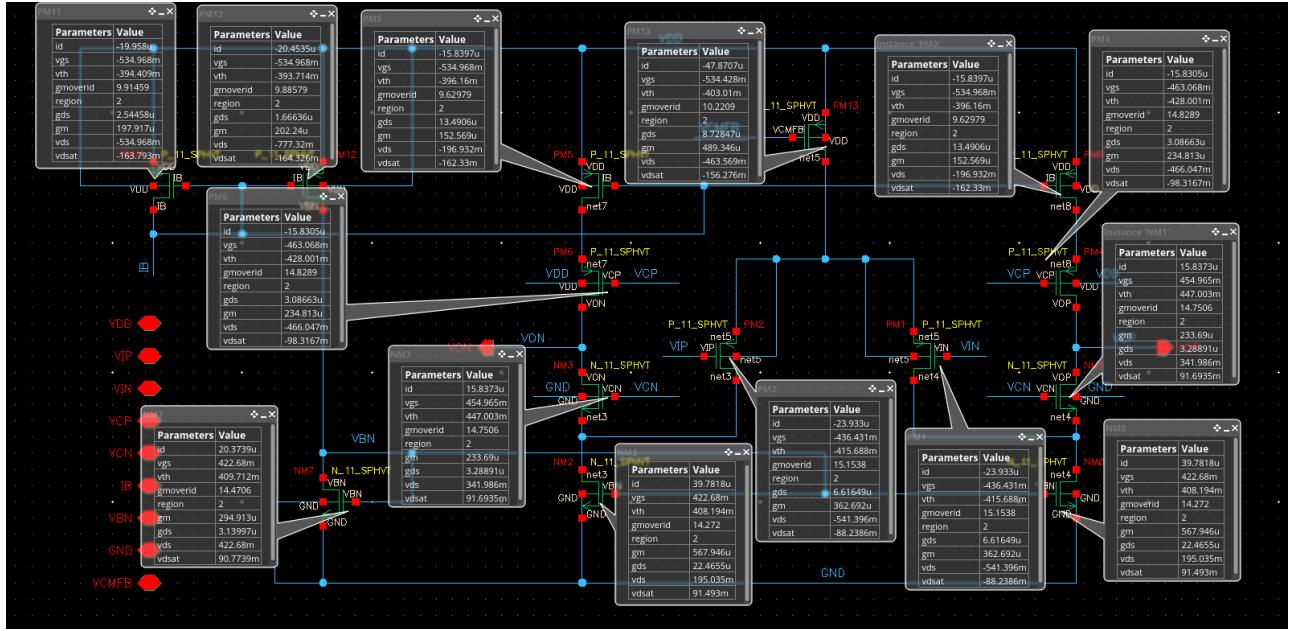


Figure 3.5: FCOTA all DC operating points after adding real CMFB

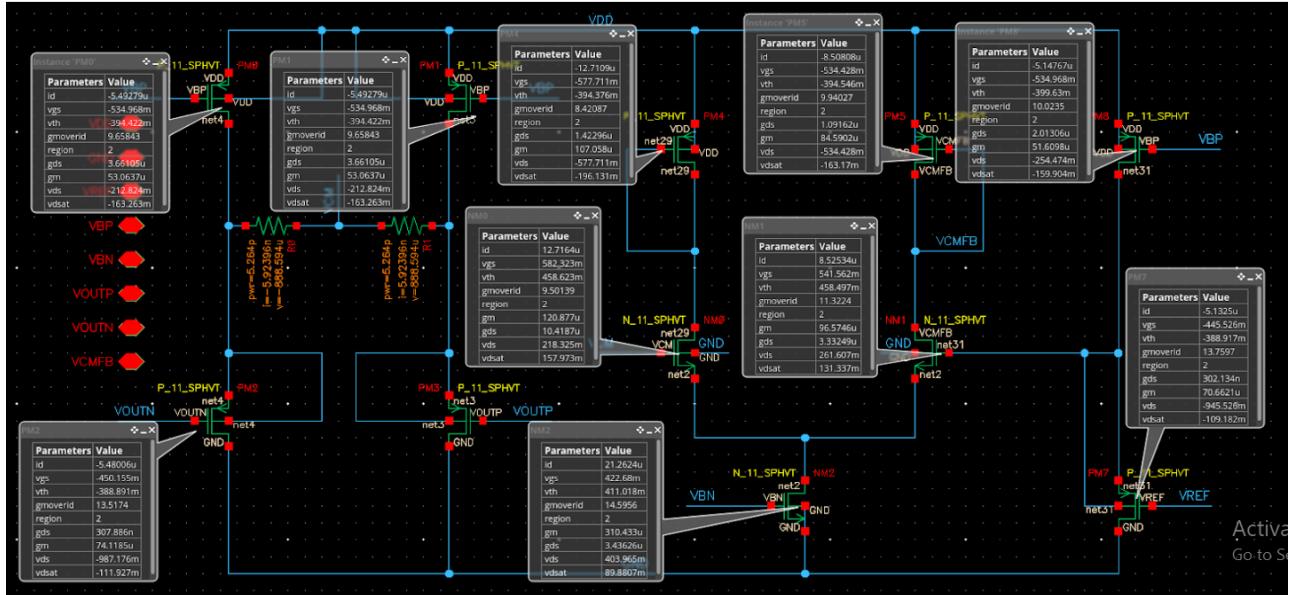


Figure 3.6: CMFB all DC operating points

Displaying all DC operating points in tabular form:

Name	NM7	NM2	NM0	NM1	NM3	PM4	PM6	PM5	PM0	PM12	PM13	PM1	PM2	PM11
Function:	n-tail current	n-biasing	n-biasing	n-cascode	n-cascode	p-cascode	p-cascode	p-biasing	p-biasing	p-tail current	diff bias	ip diff pair	ip diff pair	I ref
id (u):	20.37	39.78	39.78	15.84	15.84	-15.83	-15.83	-15.84	-15.84	-20.45	-47.87	-23.93	-23.93	-19.96
vgs (m):	422.68	422.68	422.68	454.97	454.97	-463.07	-463.07	-534.97	-534.97	-534.97	-534.43	-436.43	-436.43	-534.97
vds (m):	422.68	195.04	195.04	341.99	341.99	-466.05	-466.05	-196.93	-196.93	-777.32	-463.57	-541.4	-541.4	-534.97
vdsat (m):	90.77	91.49	91.49	91.69	91.69	-98.32	-98.32	-162.33	-162.33	-164.33	-156.28	-88.24	-88.24	-163.79
vth (m):	409.71	408.19	408.19	447	447	-428	-428	-396.16	-396.16	-393.71	-403.01	-415.69	-415.69	-394.41
gm (u):	3.14	22.47	22.47	3.29	3.29	234.81	234.81	152.57	152.57	202.24	489.35	362.69	362.69	197.92
gds (u):	294.91	567.95	567.95	233.69	233.69	3.09	3.09	13.49	13.49	1.67	8.73	6.62	6.62	2.54
gmoverid:	14.47	14.27	14.27	14.75	14.75	14.83	14.83	9.63	9.63	9.89	10.22	15.15	15.15	9.91
region:	2	2	2	2	2	2	2	2	2	2	2	2	2	2

Table 3.2: FCOTA all DC operating points after adding real CMFB

Name	PM0	PM1	PM2	PM3	PM4	PM5	NM0	NM1	NM2	PM8	PM7
Function:	Current Sensor Bias	Current Sensor Bias	Current Sensor Input	Current Sensor Input	Diff Pair Load	Diff Pair Load	Diff Pair	Diff Pair	Diff Pair Bias	Buffer Bias	Buffer
id (u):	-5.49	-5.49	-5.48	-5.48	-12.71	-8.51	12.72	8.53	21.26	-5.15	-5.13
vgs (m):	-534.97	-534.97	-450.16	-450.16	-577.71	-534.43	582.32	541.56	422.68	-534.97	-445.53
vds (m):	-212.82	-212.82	-987.18	-987.18	-577.71	-534.43	218.33	261.61	403.97	-254.47	-945.53
vdsat (m):	-163.26	-163.26	-111.93	-111.93	-196.13	-163.17	157.97	131.34	89.88	-159.9	-109.18
vth (m):	-394.42	-394.42	-388.89	-388.89	-394.38	-394.55	458.62	458.5	411.02	-399.63	-388.92
gm (u):	53.06	53.06	74.12	74.12	107.06	84.59	10.42	3.33	3.44	51.61	70.66
gds (u):	3.66	3.66	0.307	0.307	1.42	1.09	120.88	96.57	310.43	2.01	0.302
gmoverid:	9.66	9.66	13.52	13.52	8.42	9.94	9.5	11.32	14.6	10.02	13.76
region:	2	2	2	2	2	2	2	2	2	2	2

Table 3.3: CMFB all DC operating points

Comparing assumed Id and gm/Id with actual results:

#	Name	Function	assumed I_d (uA)	actual I_d (uA)	assumed g_m/I_d (s/A)	actual g_m/I_d (s/A)
1	PM0,1	Current Sensor Bias	6	5.48	10	9.64
2	PM2,3	Current Sensor Input	6	5.47	15	13.5
3	PM4,5	Diff Pair Load	11	12.7, 8.5	10	8.4 , 9.9
4	NM0,1	Diff Pair	11	12.7, 8.5	10	9.5 , 11.3
5	NM2	Diff Pair Bias	22	21.26	15	14.59
6	PM6	Buffer Bias	6	5.14	10	10
7	PM7	Buffer	6	5.13	15	13.75

We see the diff pair branches are not identical in current consumption and gm/Id. This is due to the difference in the gate voltage as one has the sensed common mode voltage and the other has the reference voltage. Total current consumption meets the design requirement <40uA: Total consumed current = $5.48 \times 2 + 21.26 + 5.14 = 38\text{uA}$

3.2.4. AC Analysis

Settings: 1Hz:10GHz, logarithmic, 10 points/decade.

Name	Type	Details	Value
Ao_dB	expr	dB20(ymax(mag(VF("/VOUTD"))))	56.64
Ao	expr	ymax(mag(VF("/VOUTD")))	679.1
BW	expr	bandwidth(VF("/VOUTD") 3 "low")	74.8K
GBW	expr	(Ao * BW)	50.8M
fu	expr	unityGainFreq(VF("/VOUTD"))	50.93M

Calculating main specs using the calculator:

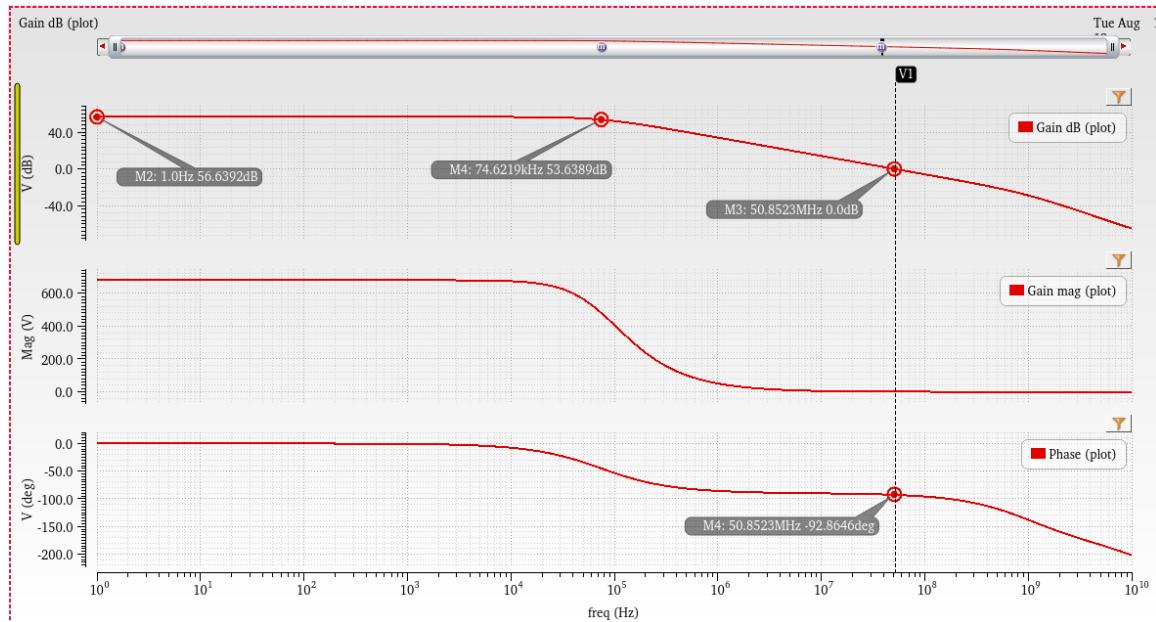
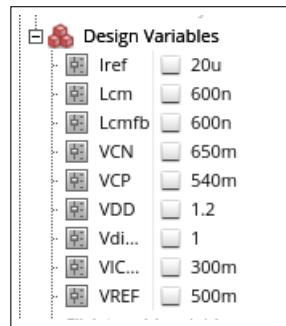


Figure 3.7: FCOTA with real CMFB Open loop Gain and Phase margin

We see that: The Open loop gain meets the requirement $>56\text{dB}$.

The Phase margin meets the requirement >70 degree.

4. Closed Loop Simulation Results

Now we set the FCOTA in a closed loop with the configuration shown to have the gain equals 2 as specified, this is established through a feedback resistor of 1M ohm and input resistor of 500k ohm. Those values were chosen to reach the maximum gain possible. We added two zero V DC sources at the output for the stability analysis, therefore we added another balun afterward to feedback the output and close the loop.

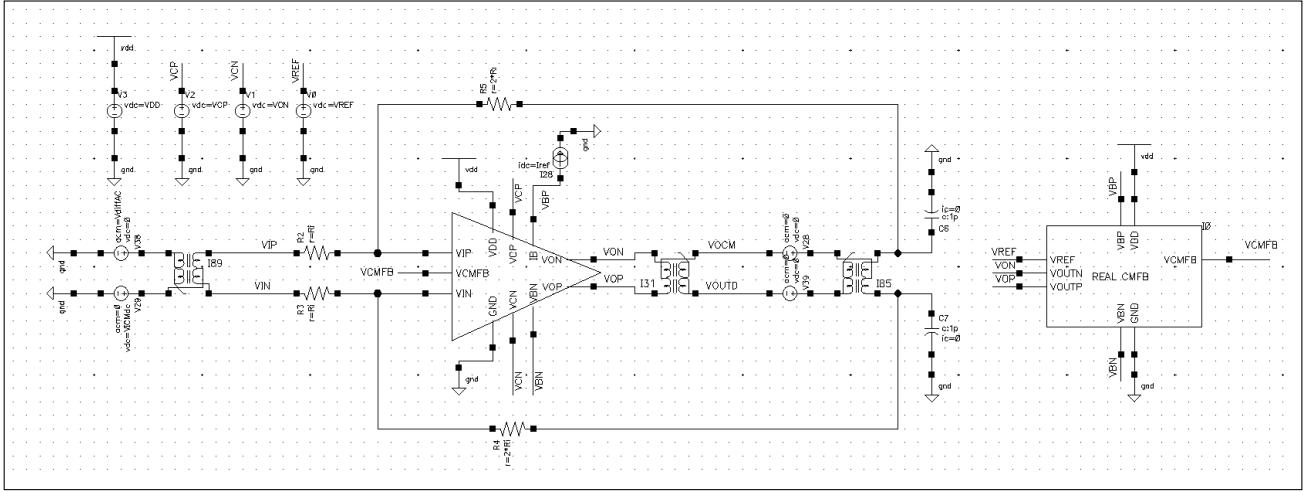


Figure 4.1: FCOTA with real CMFB Closed loop Test bench

4.1. DC operating points

OTA circuit: All devices are in saturation having same dc op points as previous analysis

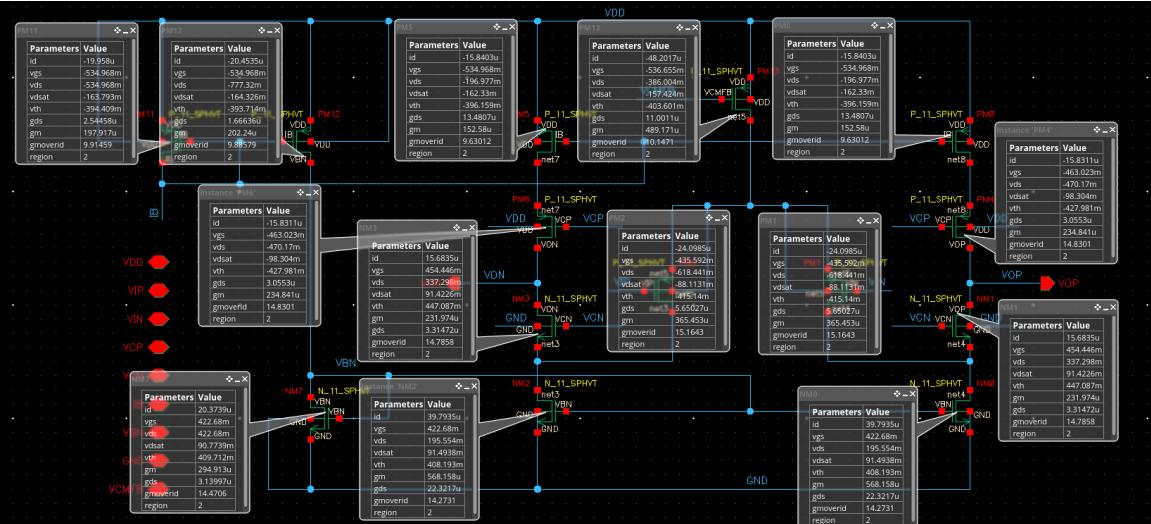


Figure 4.2: FCOTA with real CMFB Closed loop - DC Operating points

CMFB circuit: All devices are in saturation having same dc op points as previous analysis

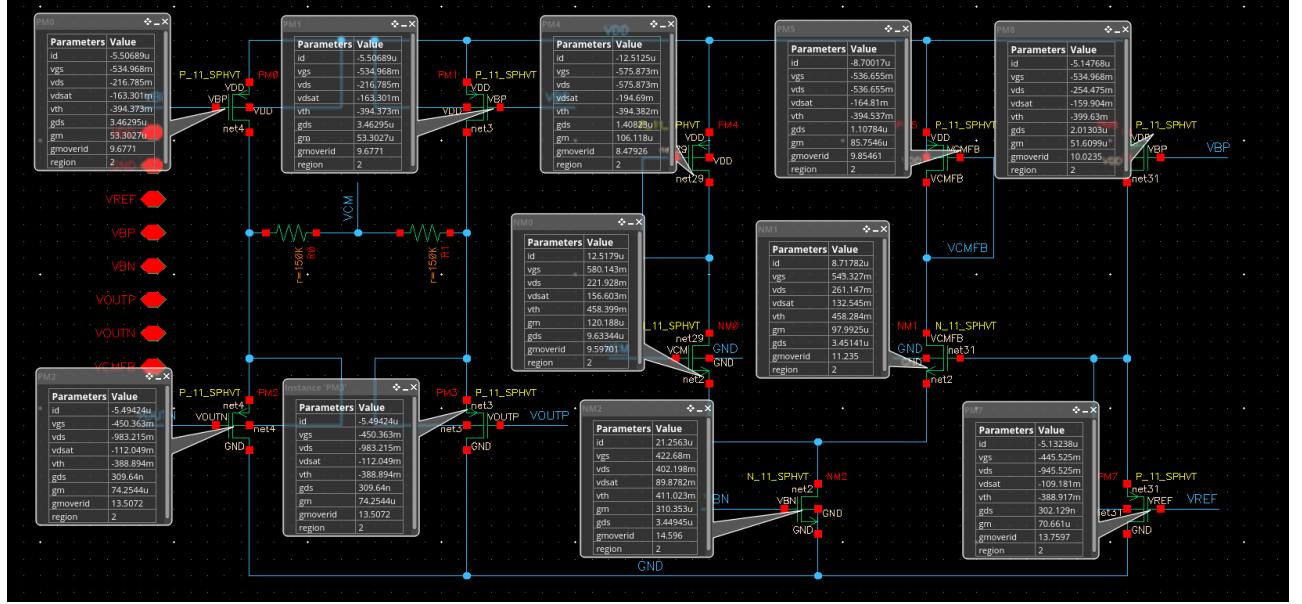


Figure 4.3: FCOTA with real CMFB Closed loop - DC Operating points

4.2. AC Analysis

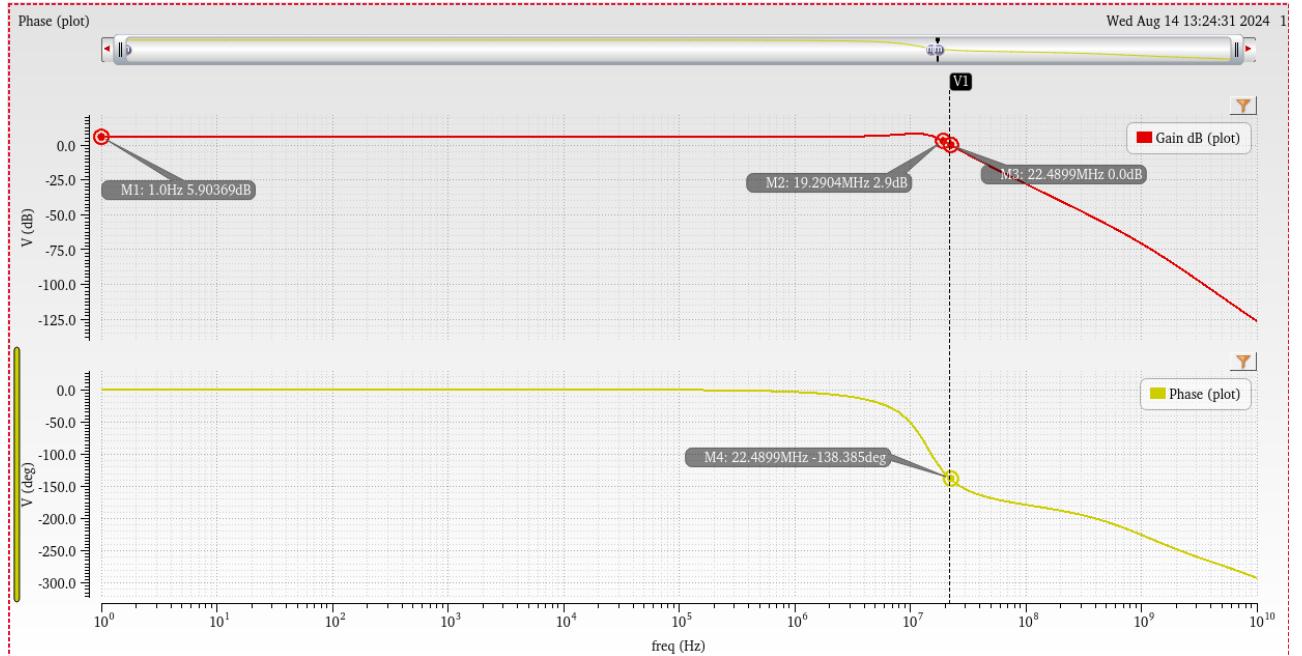


Figure 4.4: FCOTA with real CMFB Closed loop - Gain and Phase margin

Name	Type	Details	Spec	Value
Ac_db	expr	dB20(value(mag(VF("/VOUTD")) 0))	> 6.02	5.904
Ac	expr	value(mag(VF("/VOUTD")) 0)	> 2	1.973
BW	expr	bandwidth(VF("/VOUTD") 3 "low")	> 10M	19.41M
GBW	expr	(Ac * BW)	> 20M	38.3M
fu	expr	unityGainFreq(VF("/VOUTD"))	> 20M	22.83M

Comment: All specs are met. We know that closed loop gain cloud reach 2 at infinity dc open loop gain, since closed loop gain = $A_{ol}/(1 + A_{ol} * \beta)$. We see also that the gain is decreased compared to the open loop, however the BW is maximized.

4.3. Stability Analysis

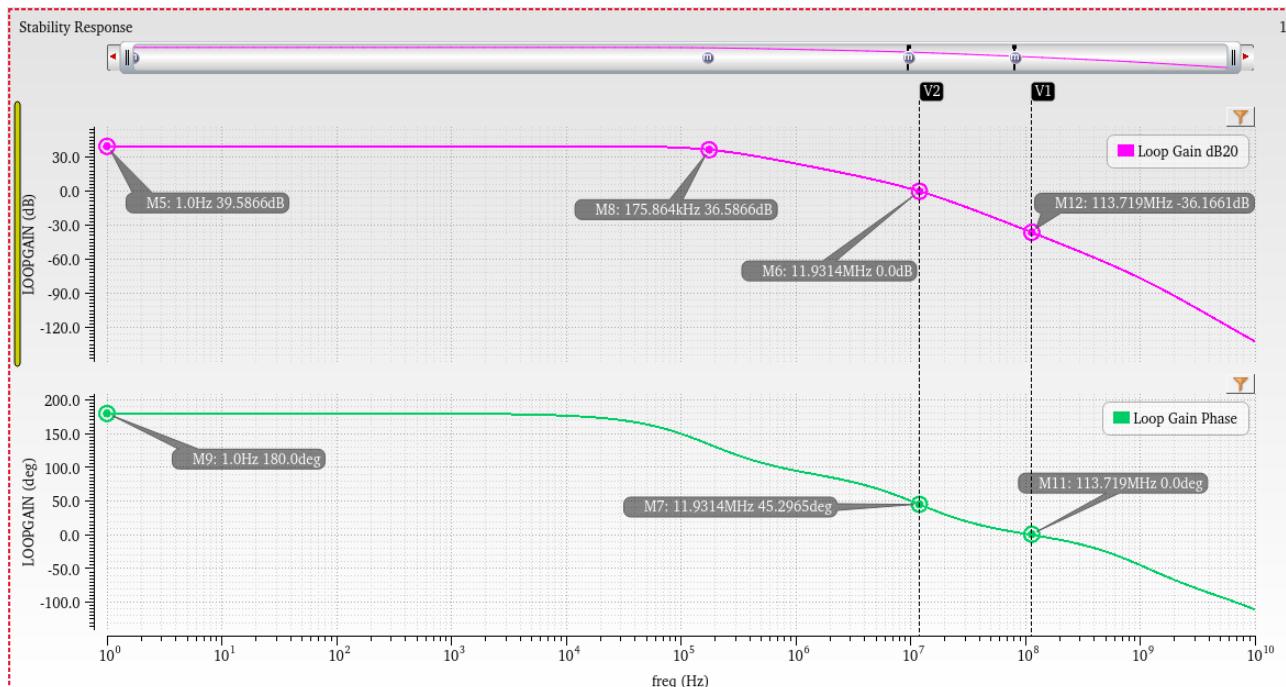


Figure 4.5: Stability plot

Comment: we see from the plot above that the loop is stable since:

- The phase margin is 45 degrees, this is an adequate value.
- The gain at 180 phase shift is $\ll 1 = -36$ dB

4.4. Transient Analysis

4.4.1. Discovering loop stability - using Pulse input

Applying an input pulse (initial value = 0, pulse value = 100mV, delay = 1us, period = 2us, pulse width = 1us, rise = fall = 10ns). Running transient analysis for 3us with 10ns max step.

-1 Applying the pulse at differential input:

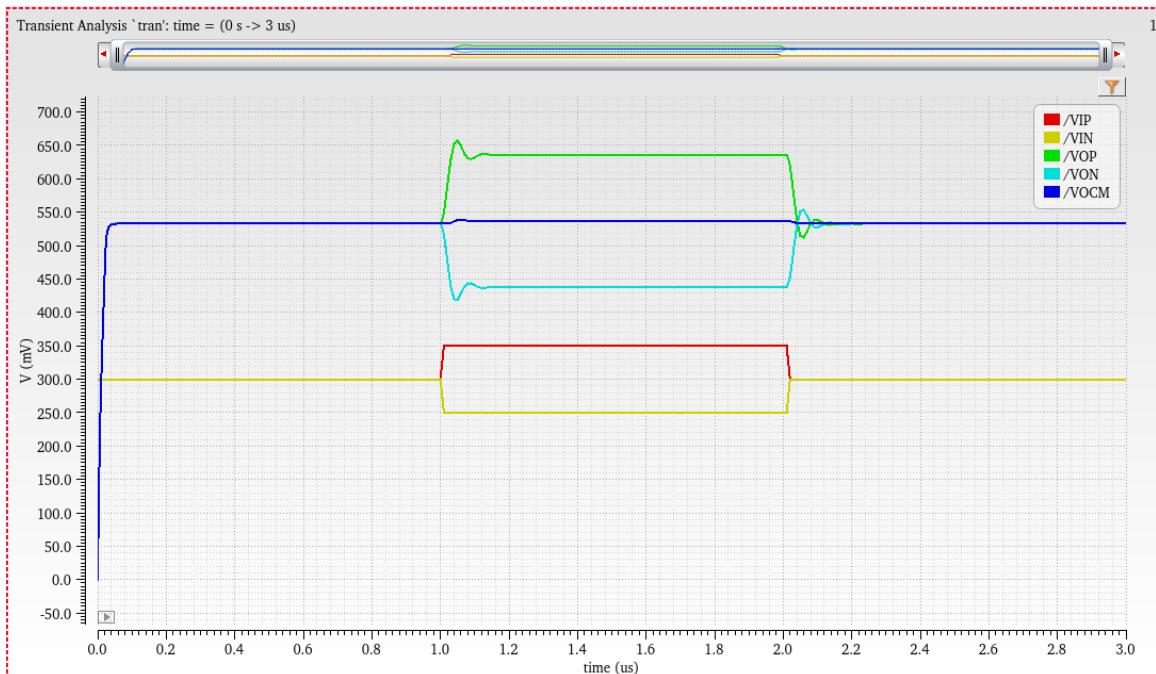


Figure 4.6: Transient plot - with ringing

Comment: by looking at the Vocm signal we see no ringing or oscillation at the cmfb loop. By looking at Vop and Von we see no oscillation at differential outputs, however there is ringing. This is due to a degradation in phase margin caused by an unwanted pole created by the large feedback resistor and the input capacitance of the OTA. To avoid this pole we will add a shunt capacitor to the feedback resistor with a very small value ($= 10\text{f F}$) that will shunt the resistor at high frequencies. This is shown in the figure 4.7.

Closed loop Test bench adjusted:

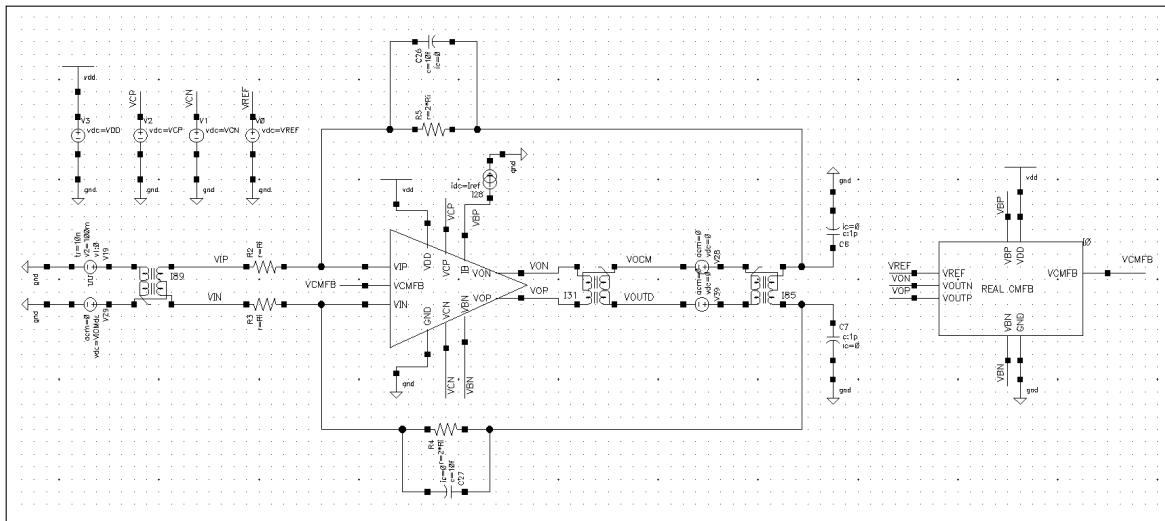


Figure 4.7: Closed loop Test bench adjusted

Plotting the signals: we see the ringing disappear.

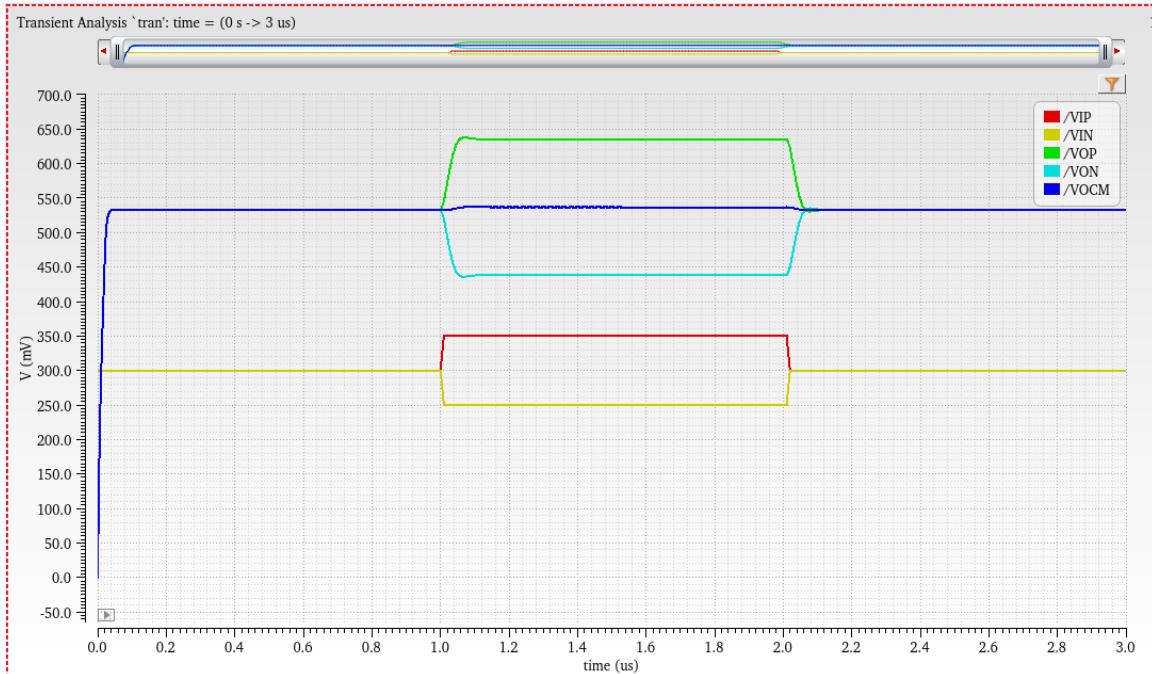
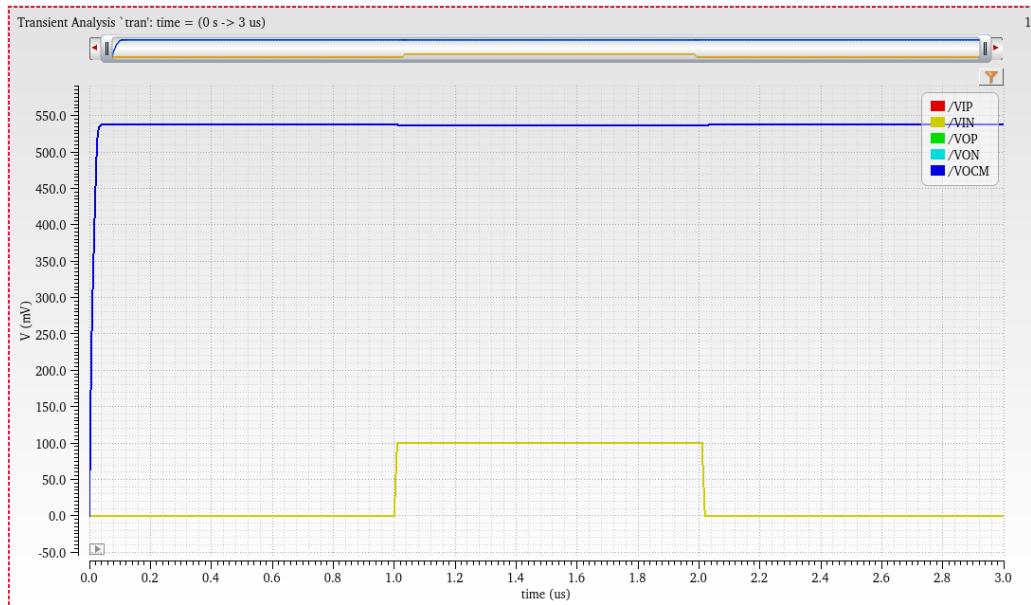


Figure 4.8: Transient plot - with no ringing

-2 Applying the pulse at the common input:



Comment: we see no ringing nor oscillation at the output. The loop is stable.

4.4.2. Discovering output swing - using Sinusoidal input

Applying a differential sinusoidal input with freq = 100kHz and amplitude = 150mV. Running transient analysis for three periods (30us) with 0.1us max time step.

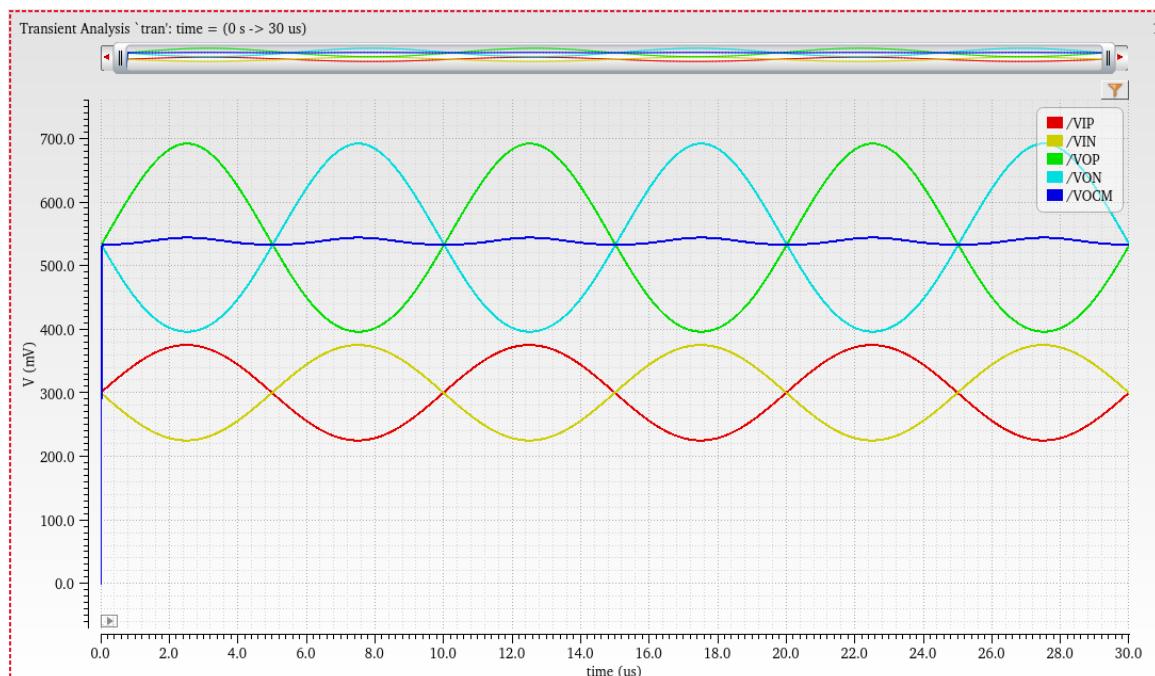


Figure 4.9: Plotting input and output signals

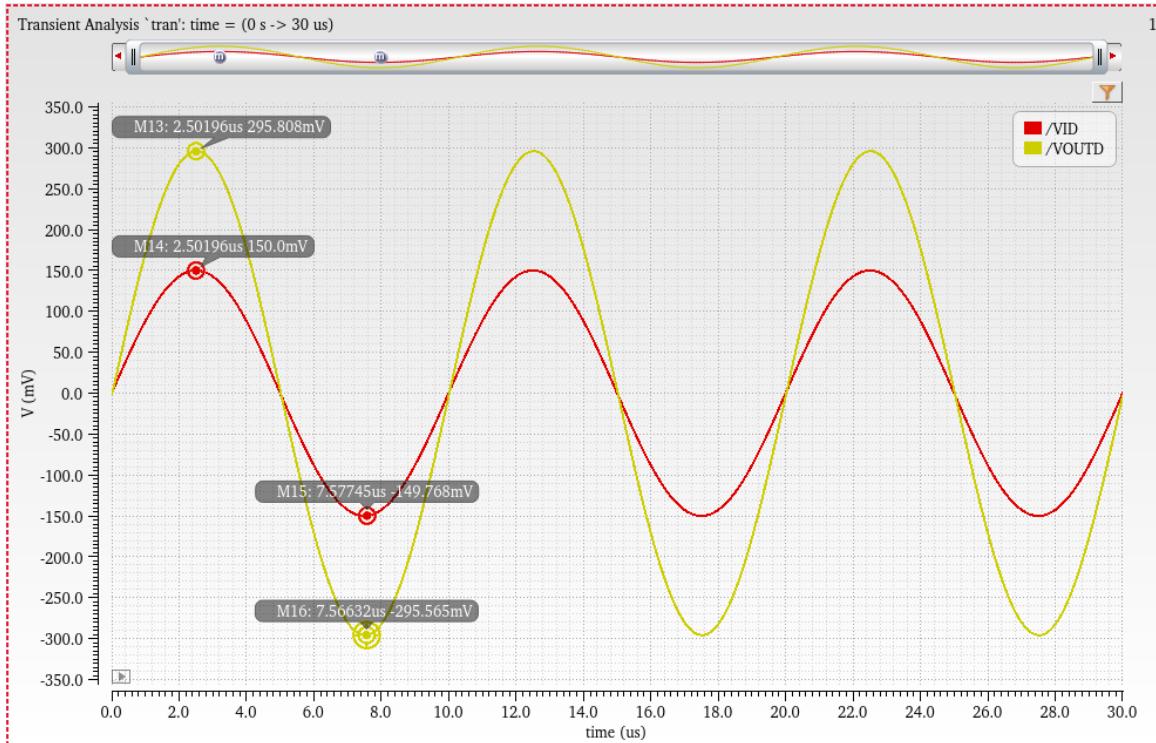


Figure 4.10: Plotting V_{id} and V_{od}

Calculating the output swing using the calculator:

Input_Swing	expr	<code>peakToPeak(v("/VID" ?result "tran"))</code>		300m
Output_Swing	expr	<code>peakToPeak(v("/VOUTD" ?result "tran"))</code>	> 600m	591.6m
Gain from swing	expr	<code>(Output_Swing / Input_Swing)</code>	> 2	1.972

Comment: the result of the gain is equal to the one calculated from the AC analysis.

Now we proceed to the floorplan and layout . . .

5. Floorplan and Layout

Before floorplanning the devices we will adjust the multipliers and number of fingers for each device to apply the best matching pattern possible. This will define the perimeter of each block so we can floorplan once. So we will begin by preparing the matching patterns. But first we will merge the cmfb and ota in one symbol to layout them together since they have the same current mirror references, as shown in figure 5.1.

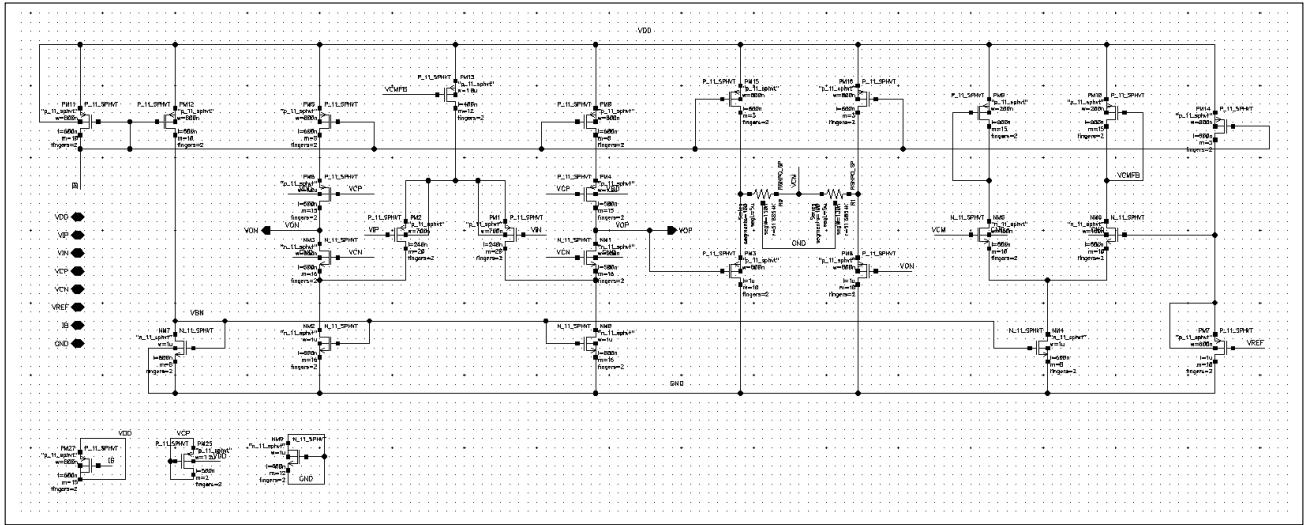
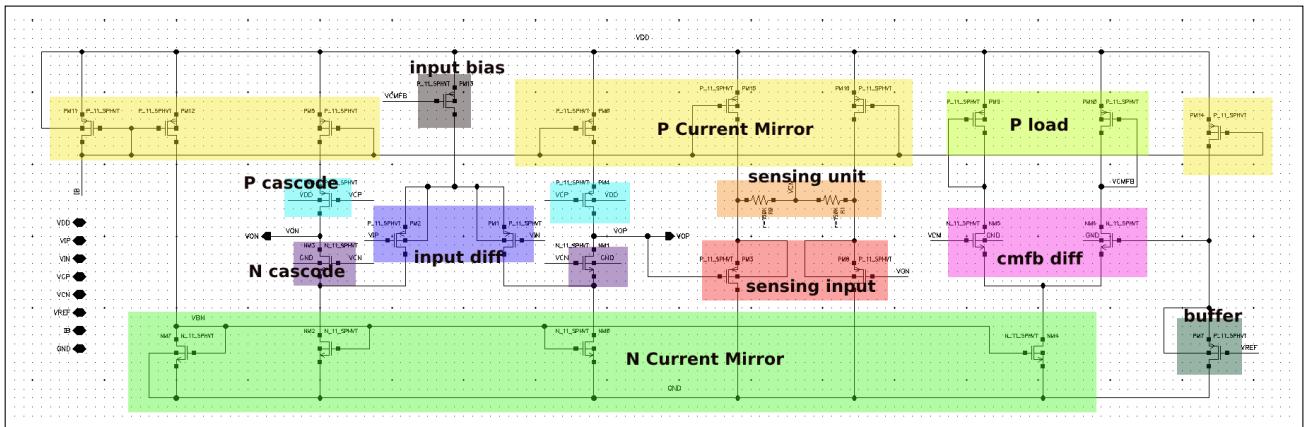


Figure 5.1: FCOTA with CMFB final Sizes

We label each block by different color to organize the floorplan and layout each block separately then rout them together.



We see 6 main blocks:

1. **P Current Mirror**
2. **N Current Mirror**
3. **Input Diff, Input Bias**
4. **P Cascode, N Cascode**
5. **Sensing Unit, Sensing Input**
6. **CMFB Diff, P load, Buffer**

We will use the interdigitate pattern for all diff pairs as we aim to have the least difference on the diff signals and this is achieved in interdigitate routing. For current mirrors we will use the common centroid pattern to enhance the matching with the reference diode connected device for all current mirrors devices. For the resistor we will use: poly resistor cell.

We had to modify some devices widths to fit with the new sizing distribution and floorplan, they are:

- PM11,12 : 7u → 8u
- PM0,5 : 6u → 6.4u
- PM14,15,16: 2u → 2.4u
- NM0,2 : 15.6u → 16u
- NM4 : 8.4u → 8u
- PM4,6 : 17.5u → 18u
- PM13 : 14u → 21.6u
- NM5,6 : 3u → 3.2u

At each modification, we ran the simulation to make sure all devices are still in saturation and no major changes happened on the dc op points.

Reporting all updated devices dimensions:

Block	Instance	Function	L(n)	W/F	Fingers	Multipliers	W/M	Total W (u)
P Current Mirror	PM11	I ref	600	0.4	2	10	0.8	8
	PM12	p-tail current	600	0.4	2	10	0.8	8
	PM0,5	p-biasing	600	0.4	2	8	0.8	6.4
	PM15,16	current Sensor Bias	600	0.4	2	3	0.8	2.4
	PM14	buffer Bias	600	0.4	2	3	0.8	2.4
	PM27	P-CM dummy	600	0.4	2	15	0.8	12
N Current Mirror	NM7	n-tail current	600	0.5	2	8	1	8
	NM0,2	n-biasing	600	0.5	2	16	1	16
	NM4	diff Pair sensing Bias	600	0.5	2	8	1	8
	NM9	N-CM dummy	600	0.5	2	8	1	8
I/P Diff Pair	PM1,2	input diff pair	240	0.35	2	20	0.7	14
	PM13	diff pair biasing	400	0.9	2	12	1.8	21.6
Folded Cascode	NM1,3	n-cascode	500	0.175	2	16	0.35	5.6
	PM4,6	p-cascode	500	0.6	2	15	1.2	18
	PM25	P-CASC dummy	500	0.6	2	2	1.2	2.4
Sensing Unit	PM3,8	Sensing Unit Input	1000	0.4	2	10	0.8	8
CMFB	PM9,10	diff Pair Load	600	0.1	2	15	0.2	3
	NM5,6	diff Pair sensing	600	0.16	2	10	0.16	3.2
	PM7	buffer	1000	0.4	2	10	0.8	8

Table 5.1: FCOTA with CMFB final proposed sizes

5.1. Floorplan

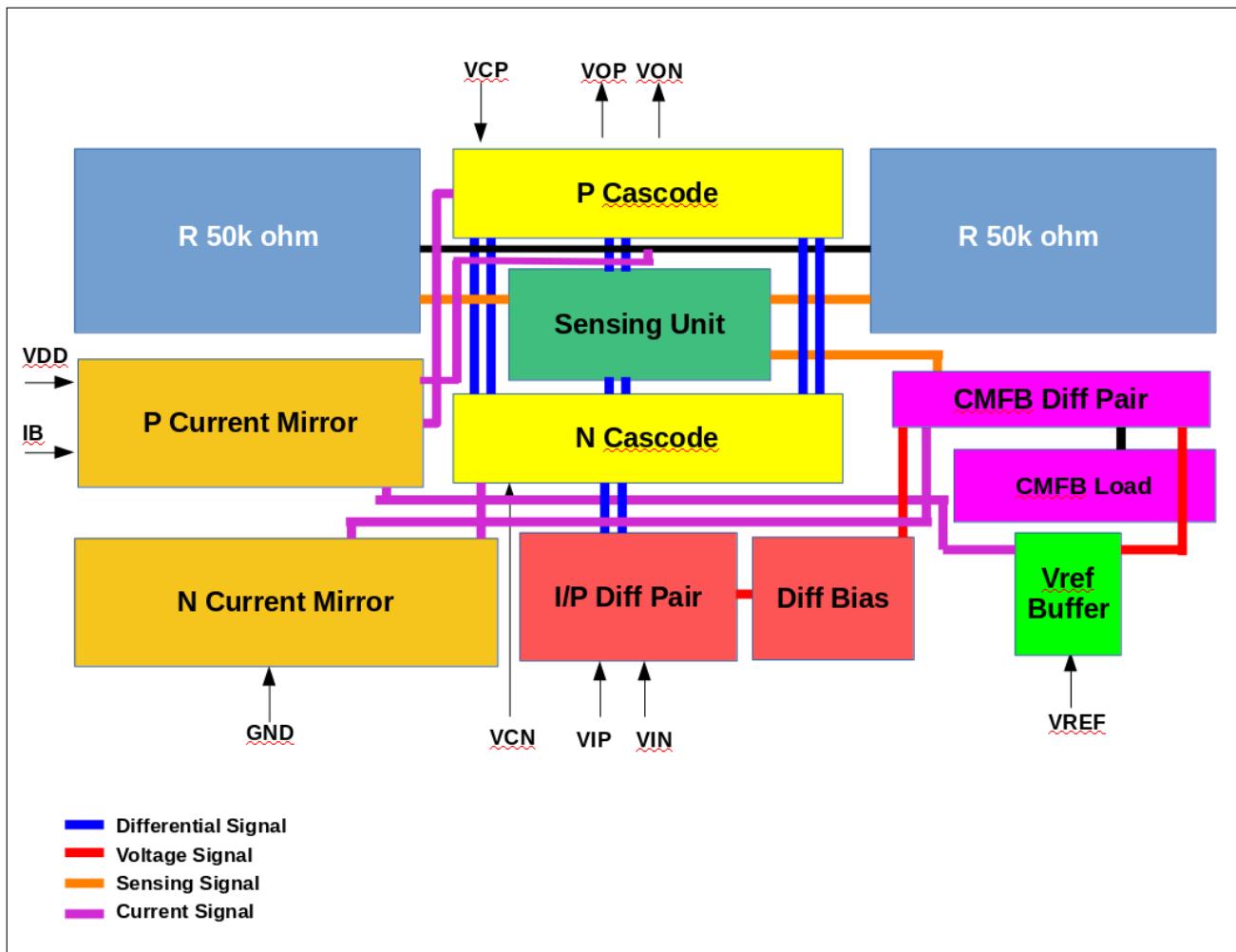
After laying out all blocks, now we can proceed to floorplan easily as we have defined outer dimensions for each block. In the floorplan we tried the best to achieve the following concepts:

- Apply symmetry in floorplan as much as possible, specially for differential blocks.
- Place related blocks side by side, like: loads of cmfb diff pair and diffpair, i/p diff pair and cascode devices, i/p diff pair and its bias device.
- Place the blocks that have inputs or outputs at the edges.
- Make the aspect ratio close to 1.5
- Maintain single gate orientation for the sake of matching.
- Keep enough safe for routing between blocks while not wasting area.
- For voltage signals make the path as short as possible to avoid IR drop.
- For diff signals place the blocks so that the routes will be symmetric.

- Customize the resistor area to fit the floorplan.
- Add guard rings to all blocks to isolate noise.

We reached the below result:

Floorplan Block diagram:



Floorplan after initial layout without routing:

5.2. Layout

5.2.1. Matching Concepts [4]

The purpose of matching is to eliminate relative parameter deviations, by aiming to identical parameter deviations. Parameter variations are caused by:

- Manufacturing tolerances such as; inhomogeneous photoresist coating, variations in the dimensional stability of masks due to thermal expansion; mask alignment tolerances, distortions in optical mapping, and different inhomogeneities occurring across the wafer during layer growth, doping, etching, and CMP.
- Layout design non-linearity.
- Application effects; as heat and mechanical stress.

Those parameter variations has one of the following effects:

- Fringe effects: internal or external.
- Gradient effects: known or unknown.
- Orientation dependent effects.

Matching Concepts:

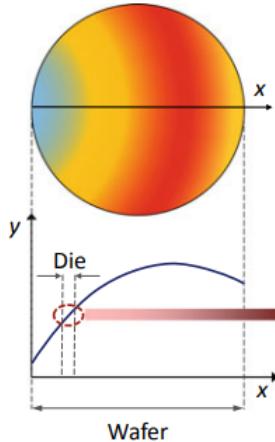
1) Matching concepts for Internal fringe effects:

- Fringe effects are effects that occur at the edges of the structures, they impact the electrical parameters non-linearly especially at stretching, and they can be stochastic or deterministic.
- We resolve this issue by splitting the device to multiples of a suitable “main device” and then we reconnect those devices in parallel or series to reach the desired parameter ratio.

Resistors: Matching resistors must always have the same width and the same length. Also, we can improve resistor matching by stretching w and l evenly, as the relative impact of fringe effects is reduced by enlarging devices.

MOS-FETs: Matching MOS-FETs always have a uniform channel length. The w/l ratios are set by folding, such that the channel widths of the single transistors are all the same.

2) Matching concepts for Unknown gradients:



- Location-dependent variations in parameter settings on the wafer are caused by tolerances in the fabrication steps, which impact the devices' electrical properties.
- Those variations are plotted as in the figure. The parameters determining them are indeterminate as the fabrication tolerances are stochastic.
- To solve this; matching devices should always be placed as close as possible to each other in the layout.
- Matching is improved if the devices are interdigitated into each other, as the distance between them is shortened.
- An effective “zero distance” can be obtained with the common centroid approach, where the geometries always feature an axis or point symmetry.
- The ideal case is a common centroid configuration with no effective distance.

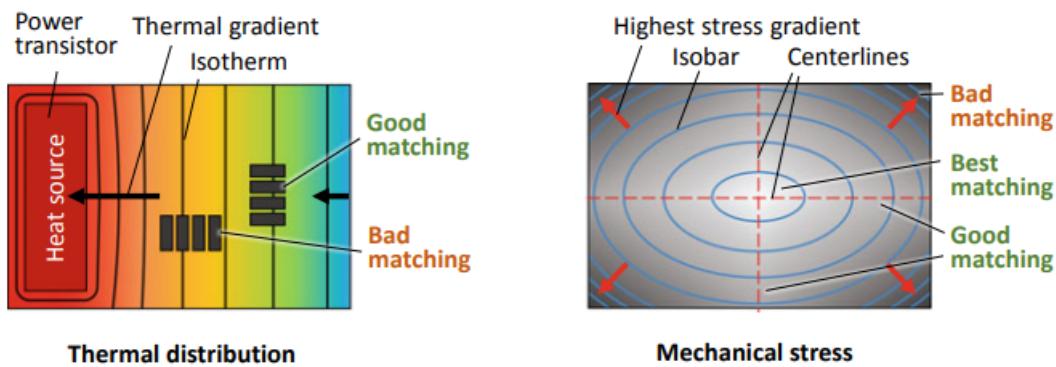


3) Matching concepts for External fringe effects:

- The elements of a matched group that lie in the group center have the same surroundings, however, the elements at the group boundary doesn't.
- So they suffer from mismatching if local inhomogeneities arise in fabrication steps.
- Trench-isolation stress: is a mechanical pressure that trench isolations exert on the directly adjacent silicon. It is temperature-dependent due to the different coefficients of thermal expansion of silicon and oxide. The pressure increases the carrier mobility of holes and lowers it for electrons, causing large mismatches.
- To resolve all the above, dummy elements that are identical to the devices in the matching group but have no electrical function, are added to surround the matching group.
- By surrounding with dummies we counter the trench stress, increase the distance between matched devices and the well boundaries and avoid discontinuity with the matched group.
- Well Proximity Effect: A high dopant concentration outside the boundary of the wells results due to the scattering during the well implantation. This severely alters the threshold voltage of a MOS-FET, causing large mismatches.

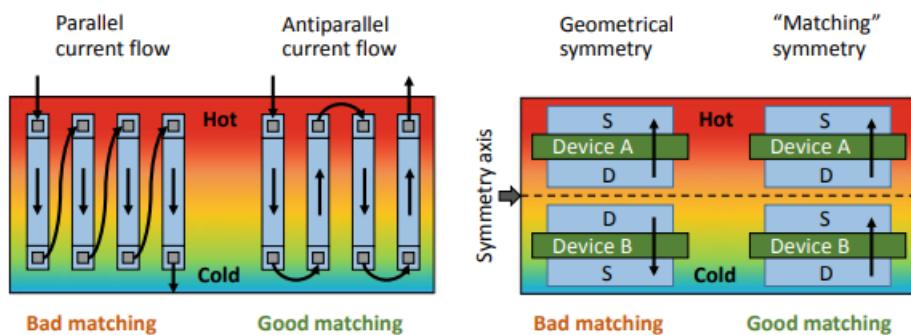
4) Matching concepts for Known gradients:

- The conditions associated with a chip's use case produce known gradients like heat distribution and mechanical stress.
- Matching concepts for unknown gradients apply here, but we can optimize more for the known gradients.
- Heat generated from thermal loss of high power density circuits or power devices as DMOS, is not distributed uniformly. Hence to avoid temperature difference, matching devices are placed along the “isotherms”, which are lines with the same temperature.
- When a chip is packaged, the injected mold mass exerts pressure on the die, permanently deforming it, causing mechanical stress in the silicon crystal, which affects the mobility of the charge carriers and thus the devices' electrical properties.
- We see that the lowest stress gradient is at the center of the chip, and it's good at the centerlines of the chip, while the corners have the highest stress, so they should be avoided for matching.



5) Matching concepts for Orientation dependant effects:

- To match all devices (except capacitors), they should always be aligned parallel to one another, to avoid alignment tolerances and carrier mobility differences due to the difference in crystal lattice alignment.
- Contact surface between two different materials produces a potential difference called Seebeck voltage in the range of 0.1 to 1 mV/K, which greatly impacts the device matching.
- Those voltages are material dependent, depending on the Seebeck coefficient.
- Currents in the segments of split devices should be aligned antiparallel, if possible, to offset Seebeck voltages.
- If this cannot be realized, the currents in matched devices should flow in the same direction.
- A layout designer should not rely on the geometrical symmetry axis. This can mirror the currents in the associated devices which should be avoided.



Summary of Matching Concepts:

Table 6.2 Summary of matching concepts (T = transistor in general, M = MOS-FET, R = resistor, C = capacitor)

	Devices	Effect/Explanation
<i>(a) Matching for normal requirements</i>		
Same device type	All	Prerequisite for matching!
Same size and shape (splitting in identical basic elements)	All	Internal device fringe effects (Sect. 6.6.1)
Minimum distance	All	Unknown gradients (Sect. 6.6.2)
Same orientation	R, T	Alignment tolerances, carrier mobility (Sect. 6.6.5)
Same ratio of area to perimeter as an alternative to splitting	C	Internal device fringe effects (Sect. 6.6.1)
<i>(b) Matching for higher requirements</i>		
Interdigitation 1- or 2-dimensional	All	Unknown gradients (Sect. 6.6.2)
Same temperature (placing along isotherms)	All	Thermal gradient (known gradient) (Sect. 6.6.4)
Same environment (dummy elements)	All	External device fringe effects (Sect. 6.6.3)
Consider current flow direction	R, T	Thermoelectric effect (Sect. 6.6.5)
Increase dimensions	R, T	Internal device fringe effects (Sect. 6.6.1)
Distance to well border $>1 \mu\text{m}$	M	Well proximity effect (Sect. 6.6.3)
<i>(c) Matching for highest requirements</i>		
Common centroid layout	All	Unknown gradients (Sect. 6.6.2)
Placement in low stress chip regions	All	Carrier mobility (Sect. 6.6.5)
Symmetrical routing	All	Depending on circuit function

5.2.2. Blocks Layout

(Matching Patterns & Local Routing)

Now, after resizing we prepare the matching patterns for each block and lay it out:

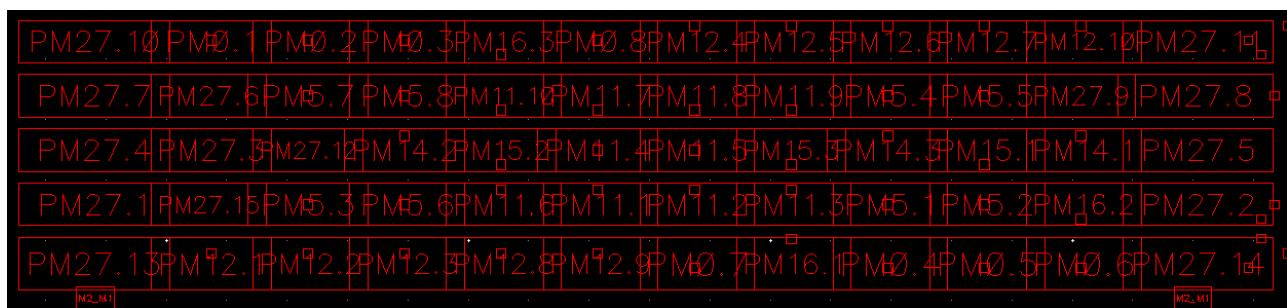
5.2.2.1. P Current Mirror

Instance	Symbol	Function	L(n)	W/F	F	M	W/M	Total W (u)
PM11	A	I ref	600	0.4	2	10	0.8	8
PM12	B	p-tail current	600	0.4	2	10	0.8	8
PM0	C	p-biasing	600	0.4	2	8	0.8	6.4
PM5	D	p-biasing	600	0.4	2	8	0.8	6.4
PM15	E	current Sensor Bias	600	0.4	2	3	0.8	2.4
PM16	F	current Sensor Bias	600	0.4	2	3	0.8	2.4
PM14	G	buffer Bias	600	0.4	2	3	0.8	2.4
PM27	dummy	dummy	600	0.4	2	15	0.8	12

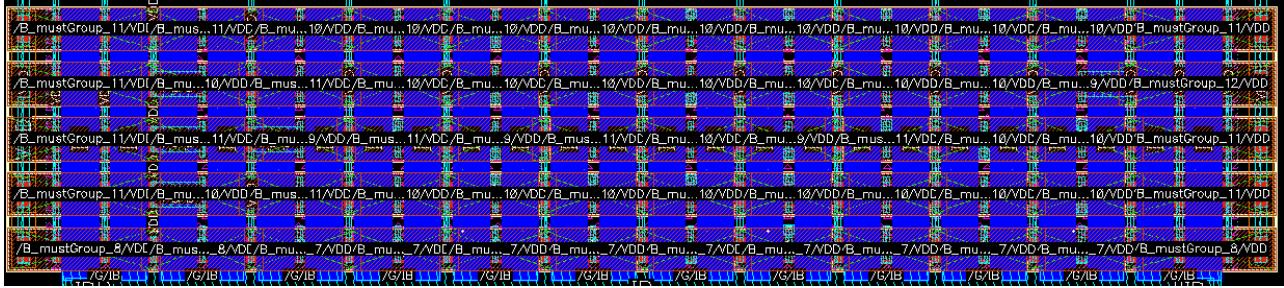
Pattern (common centroid) :

dummy	C	C	C	F	C	B	B	B	B	B	dummy
dummy	dummy	D	D	A	A	A	A	D	D	dummy	dummy
dummy	dummy	dummy	G	E	A	A	E	G	E	G	dummy
dummy	dummy	D	D	A	A	A	A	D	D	F	dummy
dummy	B	B	B	B	B	C	F	C	C	C	dummy

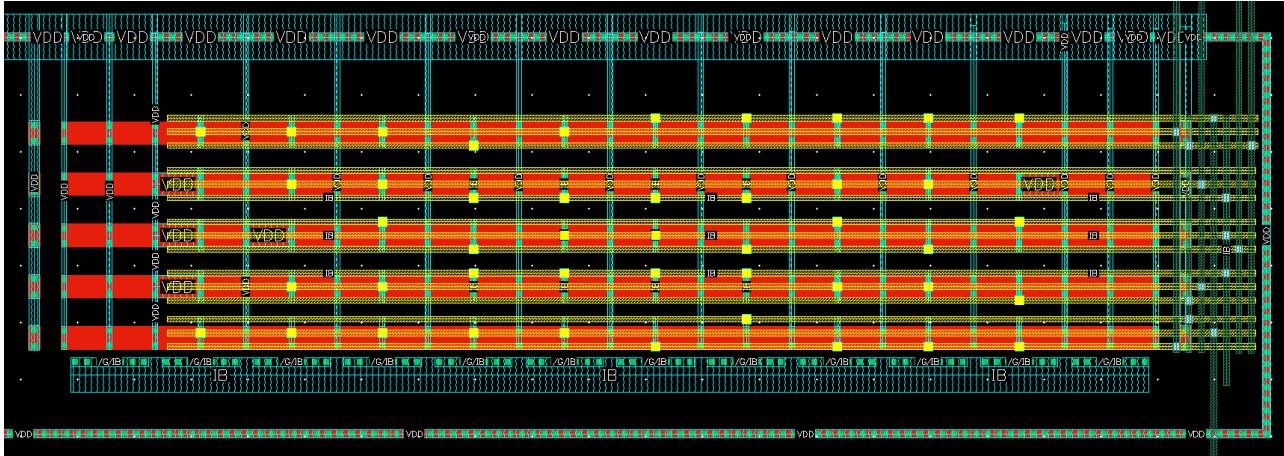
Sharing Diffusion Area (sources):



Initial Block Layout:

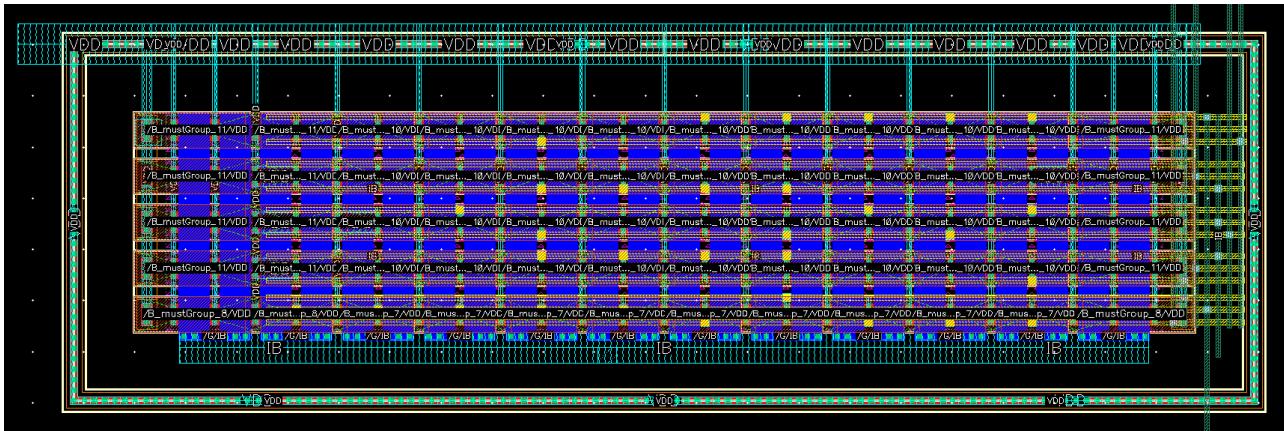


Routing:



- Drains: connect them horizontally on 3 nets per row using metal 2 and combine them vertically on metal 3 on the side of the block.
 - Sources: connect them vertically on metal 1
 - Gates: connect them vertically on poly and connect the bottom row gates on metal 1.
 - Body: through the body of the left and right dummies.

Final Block Layout:



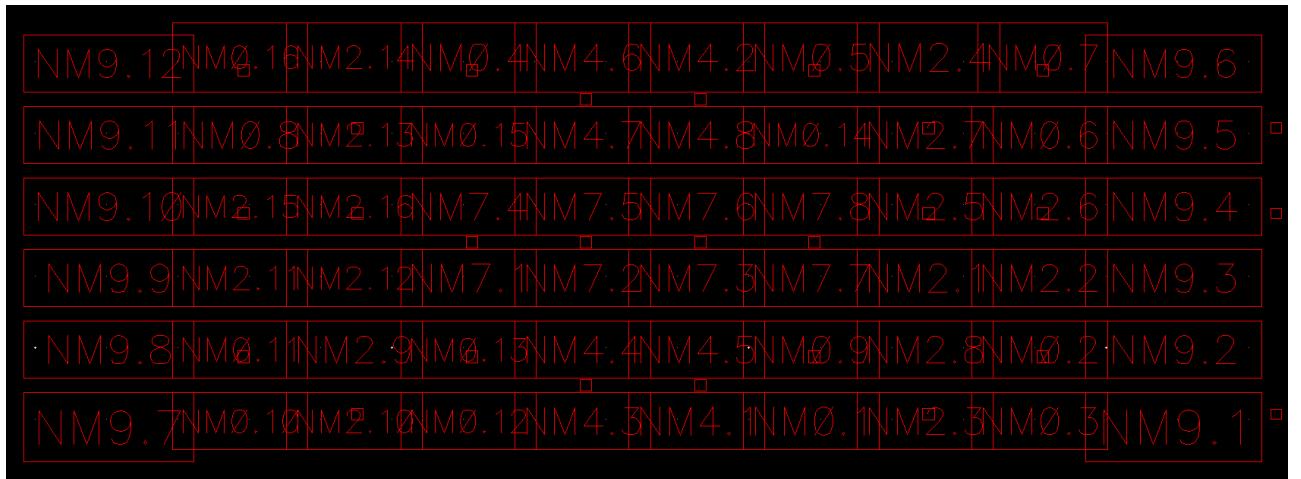
5.2.2.2. N Current Mirror

Instance	Symbol	Function	L(n)	W/F	F	M	W/M	Total W (u)
NM7	A	n-tail current	600	0.5	2	8	1	8
NM0	B	n-biasing	600	0.5	2	16	1	16
NM2	C	n-biasing	600	0.5	2	16	1	16
NM4	D	diff Pair sensing Bias	600	0.5	2	8	1	8
NM9	dummy	dummy	600	0.5	2	8	1	8

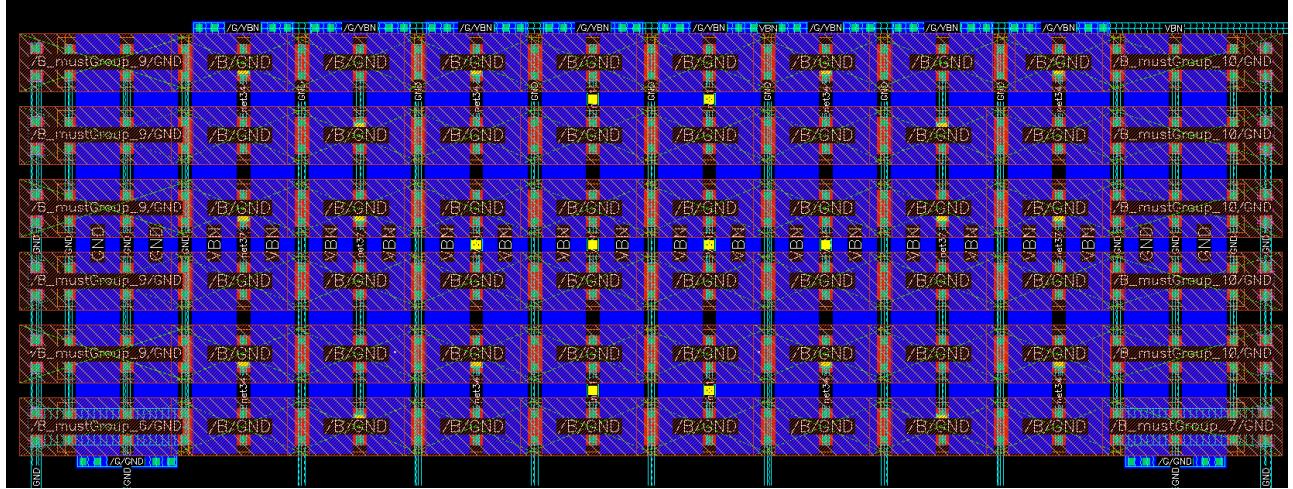
Pattern (common centroid) :

dummy	B	C	B	D	D	B	C	B	dummy
dummy	B	C	B	D	D	B	C	B	dummy
dummy	C	C	A	A	A	A	C	C	dummy
dummy	C	C	A	A	A	A	C	C	dummy
dummy	B	C	B	D	D	B	C	B	dummy
dummy	B	C	B	D	D	B	C	B	dummy

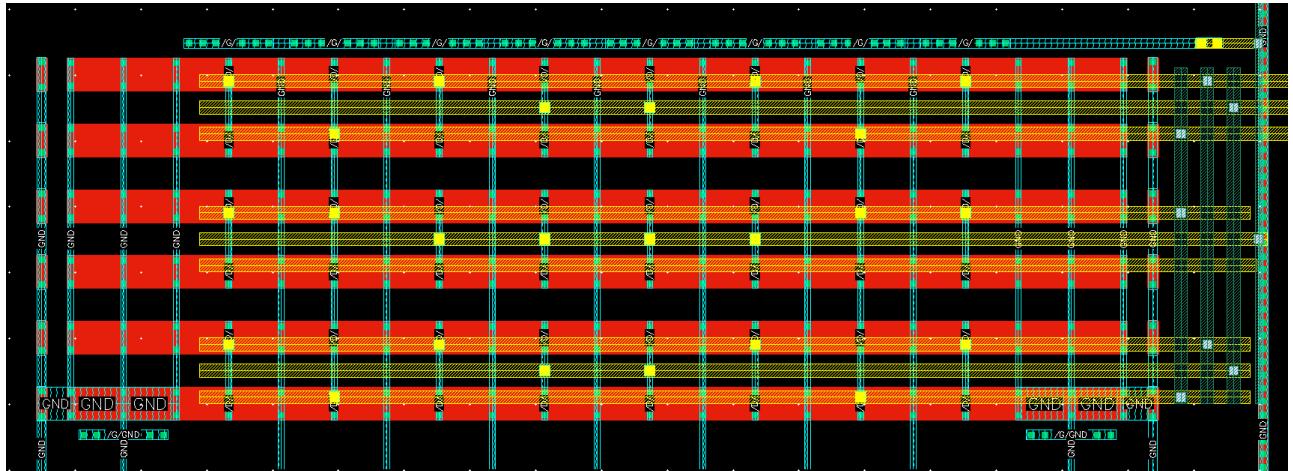
Sharing Diffusion Area (sources):



Initial Block Layout:

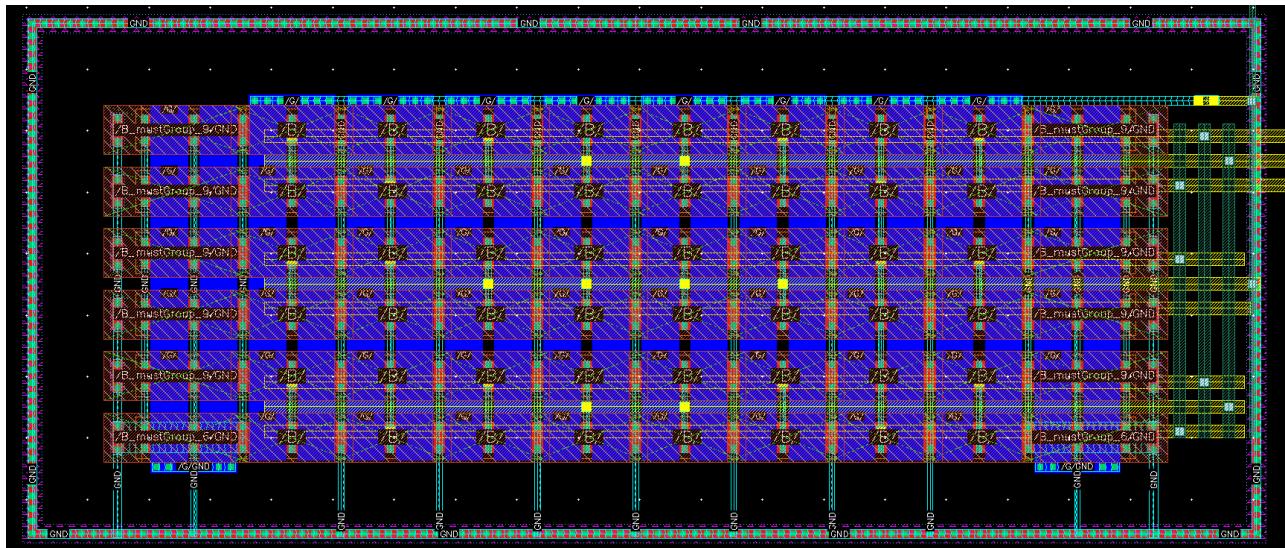


Routing:



- Drains: connect them horizontally on 3 nets per 2 rows and the middle rows (A,C) will have one dummy net and combine them vertically on metal 3 on the side of the block.
- Sources: connect them vertically on metal 1.
- Gates: connect them vertically on poly, and combine horizontally on metal 1 on the top row for main devices, and the bottom row for dummies as they are on different nets.
- Body: through the body of the left and right dummies.

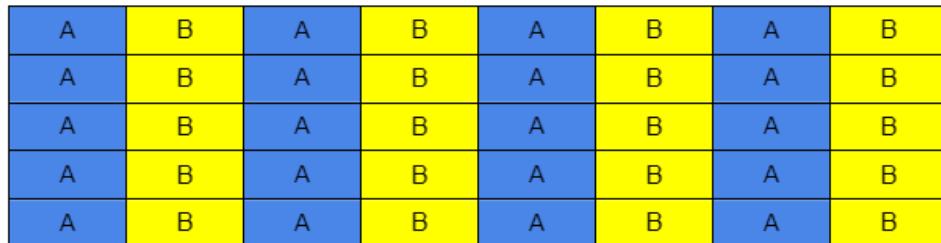
Final Block Layout:



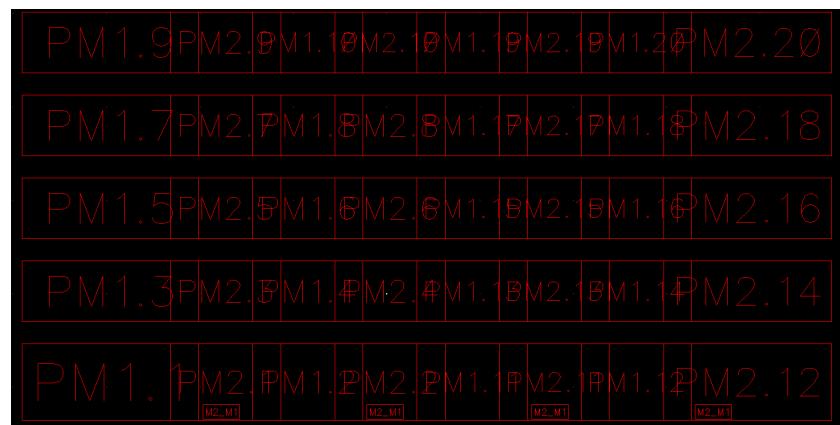
5.2.2.3. Input Diff Pair

Instance	Symbol	Function	L(n)	W/F	F	M	W/M	Total W (u)
PM1	A	input diff pair	240	0.35	2	20	0.7	14
PM2	B	input diff pair	240	0.35	2	20	0.7	14

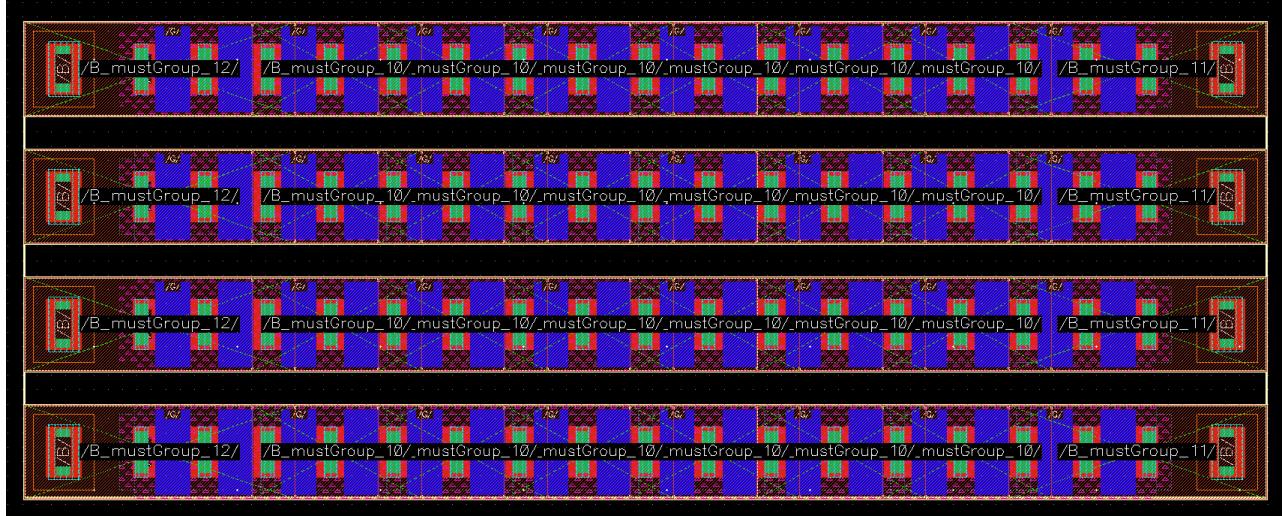
Pattern (interdigitate) :



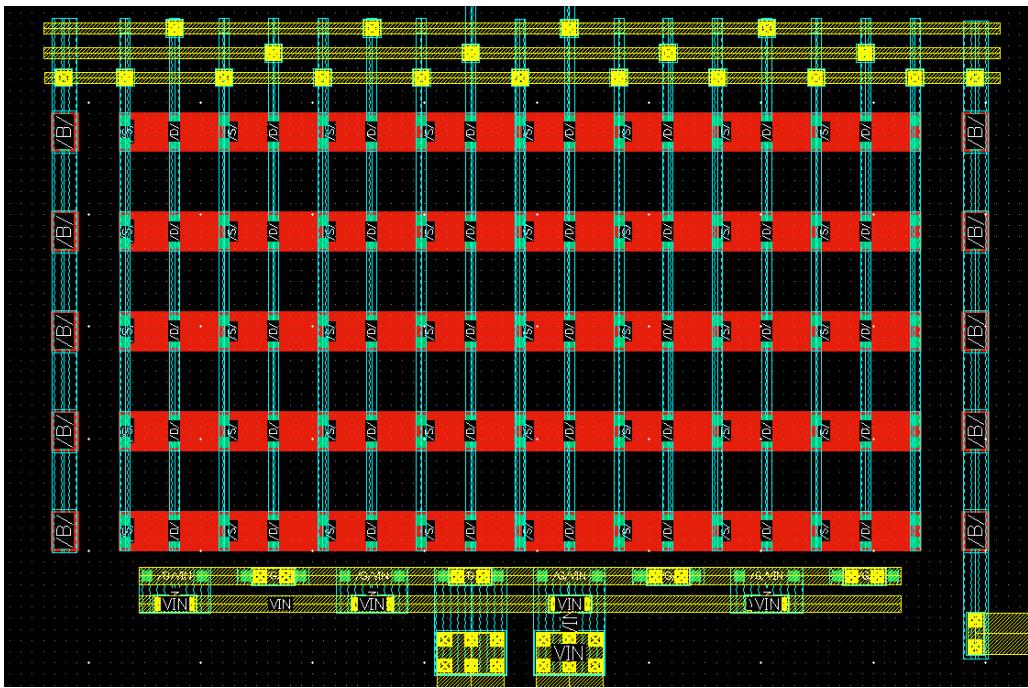
Sharing Diffusion Area (sources):



Initial Block Layout:

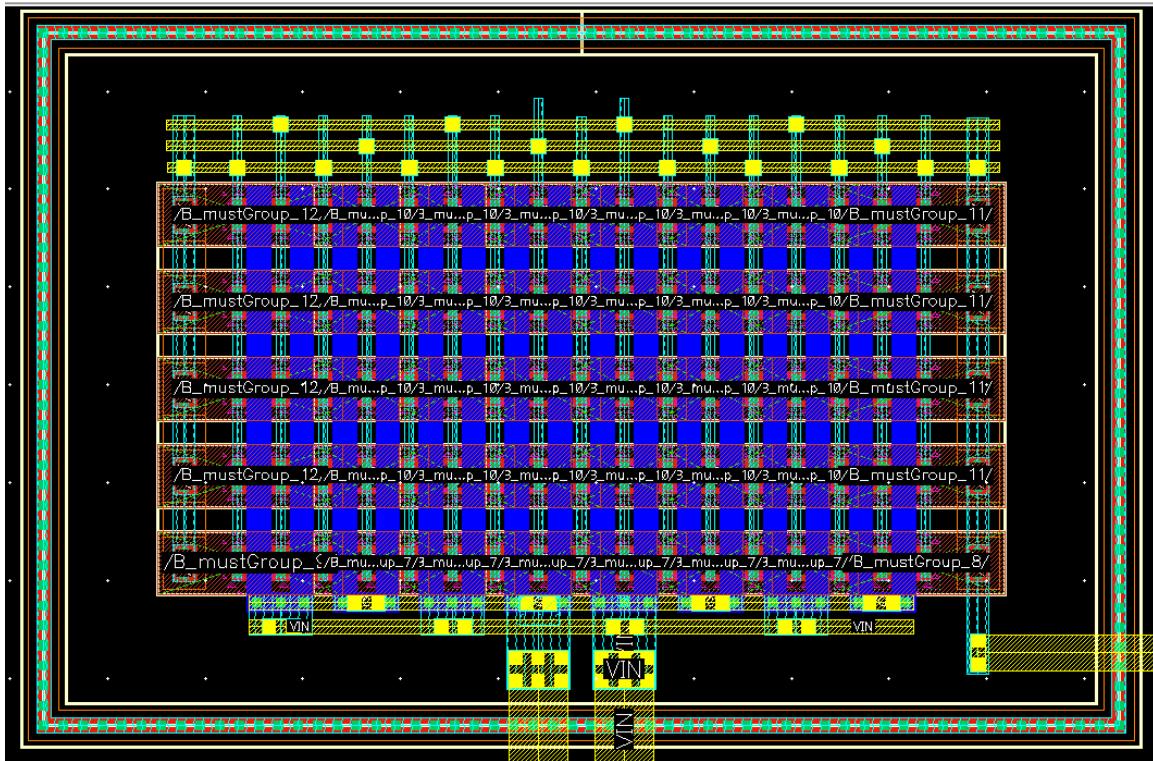


Routing:



- Drains and Sources: connect them vertically on metal 1 and combine horizontally on metal 2 above the block.
- Gates: connect them horizontally on two nets of metal 2 at the bottom row.
- Body: through the body of the left and right devices.

Final Block Layout:



5.2.2.4. Cascode devices

Instance	Symbol	Function	L(n)	W/F	F	M	W/M	Total W (u)
NM1,3	A	n-cascode	500	0.175	2	16	0.35	5.6
NM1,3	B	n-cascode	500	0.175	2	16	0.35	5.6
PM4,6	C	p-cascode	500	0.6	2	15	1.2	18
PM4,6	D	p-cascode	500	0.6	2	15	1.2	18
PM25	dummy	p-cascode dummy	500	0.6	2	2	1.2	2.4

Pattern (interdigitate) :

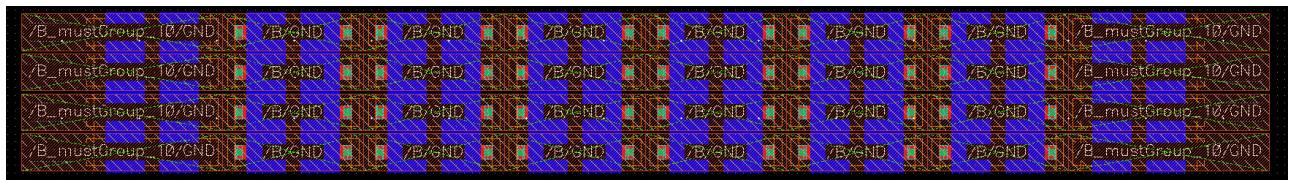
A	B	A	B	A	B	A	B
A	B	A	B	A	B	A	B
A	B	A	B	A	B	A	B
A	B	A	B	A	B	A	B
C	D	C	D	C	D	C	D
C	D	C	D	C	D	C	D
C	D	C	D	C	D	C	D
C	D	C	D	C	D	dummy	dummy

N Cascode:

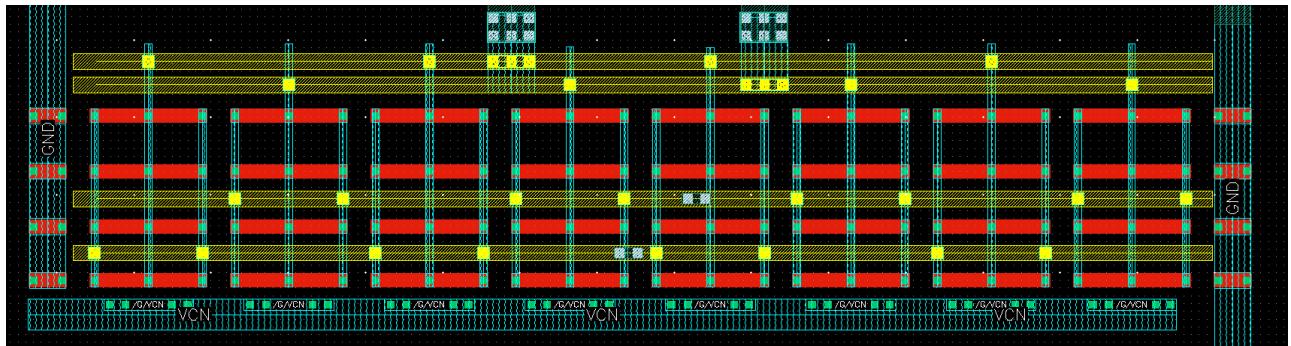
No Sharing for Diffusion Area:

NM1.13	NM3.13	NM1.15	NM3.15	NM1.14	NM3.14	NM1.16	NM3.16
NM1.9	NM3.9	NM1.11	NM3.11	NM1.10	NM3.10	NM1.12	NM3.12
NM1.5	NM3.5	NM1.7	NM3.7	NM1.6	NM3.6	NM1.8	NM3.8
NM1.1	NM3.1	NM1.3	NM3.3	NM1.2	NM3.2	NM1.4	NM3.4

Initial Block Layout:

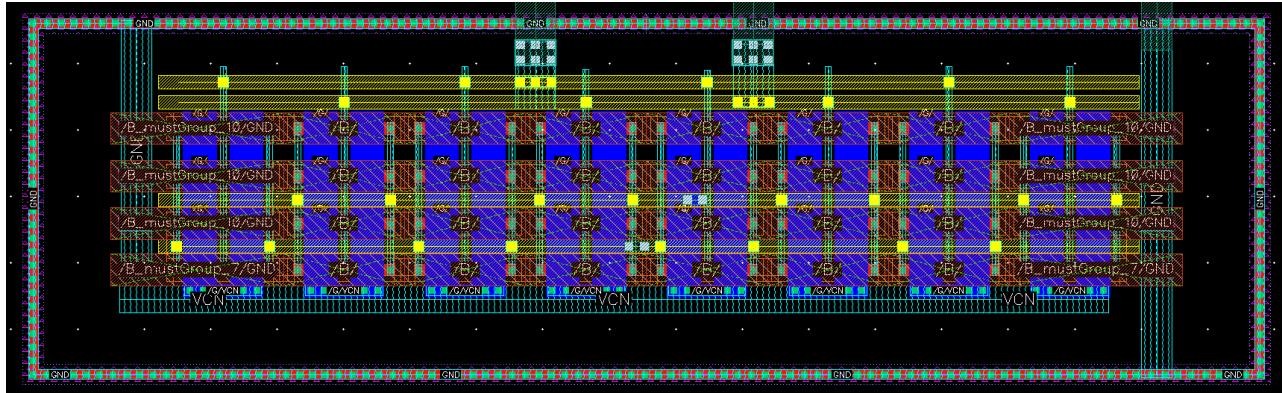


Routing:



- Drains: connect them vertically on metal 1 and combine them horizontally on two nets of metal 2 upside the block.
- Sources: connect them vertically on metal 1 and combine them horizontally on two nets of metal 2 above the block.
- Gates: connect them vertically on poly, and combine them horizontally on metal 1 on the bottom row.
- Body: through the body of the left and right devices.

Final Block Layout:

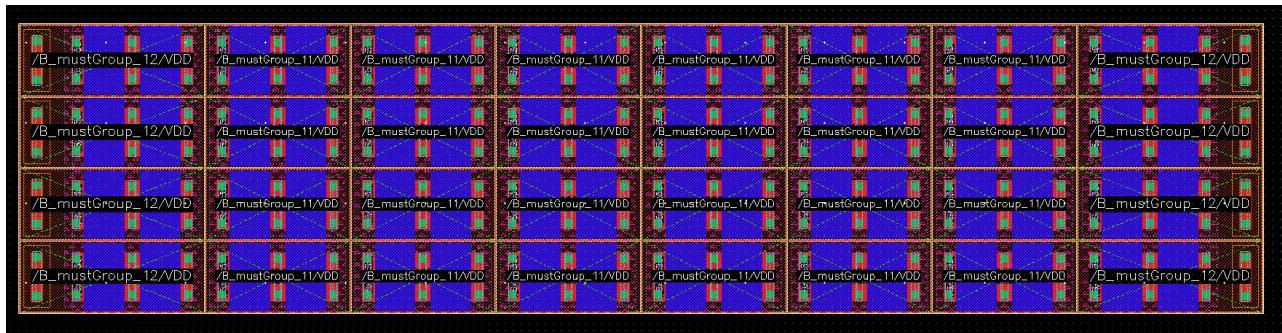


P Cascode:

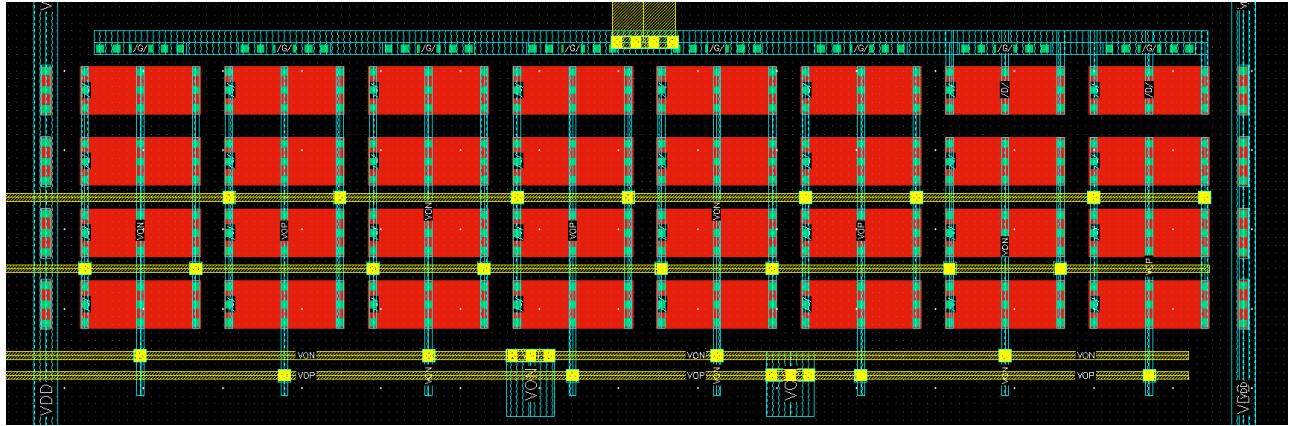
No Sharing for Diffusion Area:

PM4.13	PM6.13	PM4.15	PM6.15	PM4.14	PM6.14	PM25.1	PM25.2
PM4.9	PM6.9	PM4.11	PM6.11	PM4.10	PM6.10	PM4.12	PM6.12
PM4.5	PM6.5	PM4.7	PM6.7	PM4.6	PM6.6	PM4.8	PM6.8
PM4.1	PM6.1	PM4.3	PM6.3	PM4.2	PM6.2	PM4.4	PM6.4

Initial Block Layout:

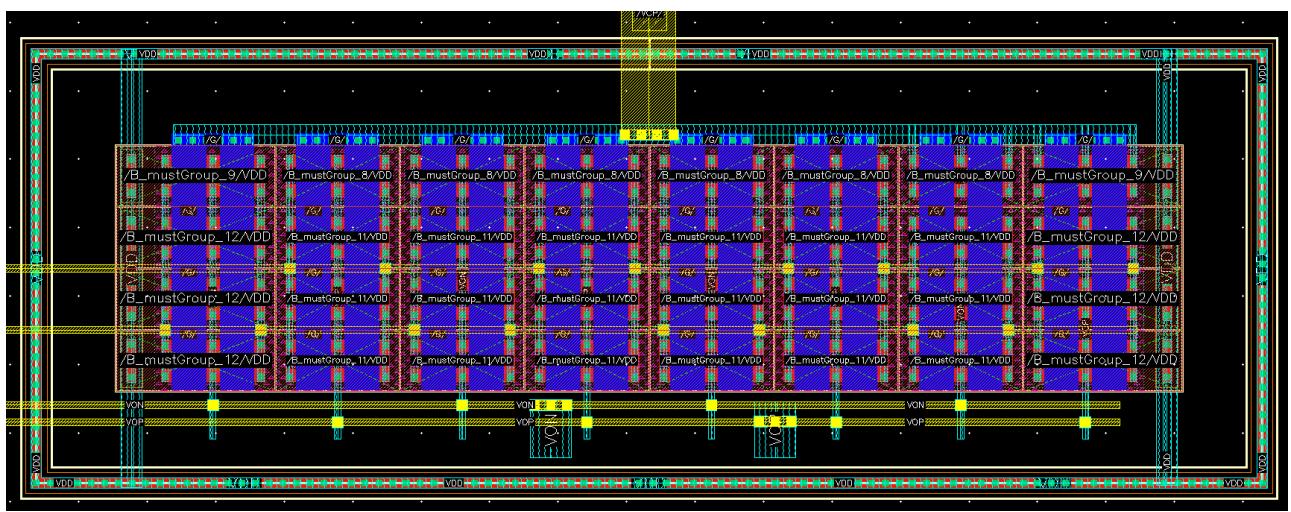


Routing:



- Drains: connect them vertically on metal 1 and combine them horizontally on two nets of metal 2 down sideside the block.
- Sources: connect them vertically on metal 1 and combine them horizontally on two nets of metal 2 above the block.
- Gates: connect them vertically on poly, and combine them horizontally on metal 1 on the top row.
- Body: through the body of the left and right devices.

Final Block Layout:



5.2.2.5. CMFB

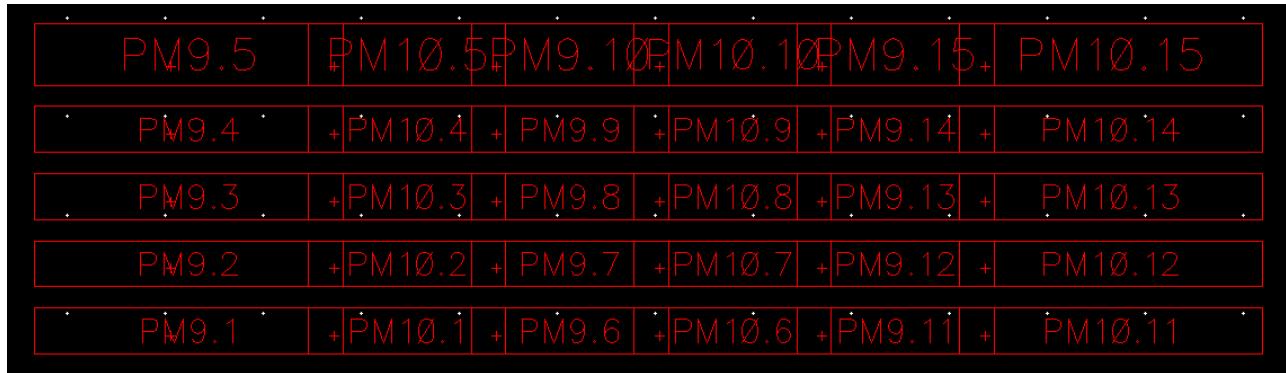
Instance	Symbol	Function	L(n)	W/F	F	M	W/M	Total W (u)
PM9	A	diff Pair Load	600	0.1	2	15	0.2	3
PM10	B	diff Pair Load	600	0.1	2	15	0.2	3
NM5	C	diff Pair sensing	600	0.16	2	10	0.16	3.2
NM6	D	diff Pair sensing	600	0.16	2	10	0.16	3.2

Pattern (interdigitate) :



diff Pair Load

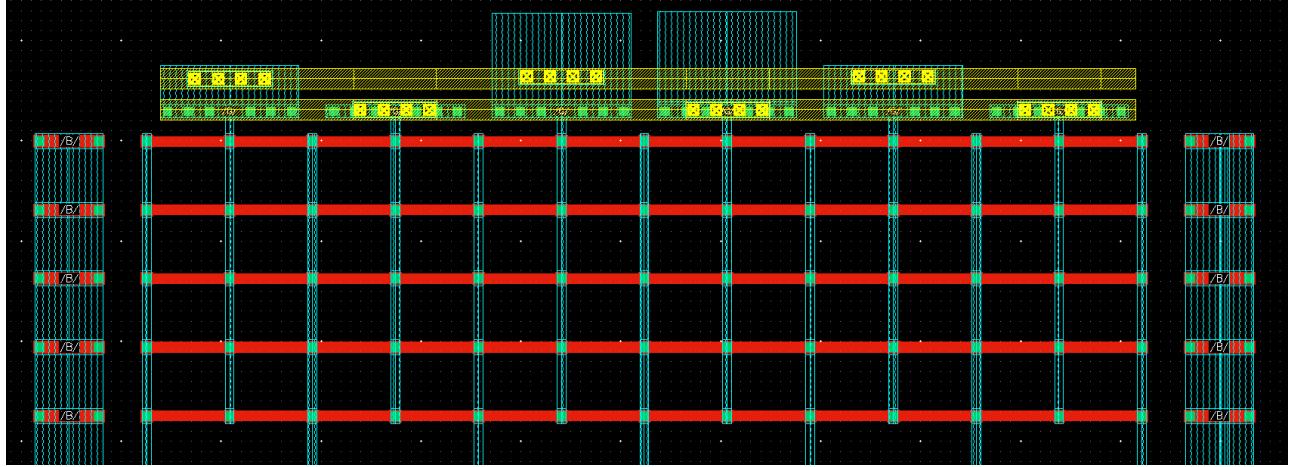
Sharing Diffusion Area (sources):



Initial Block Layout:

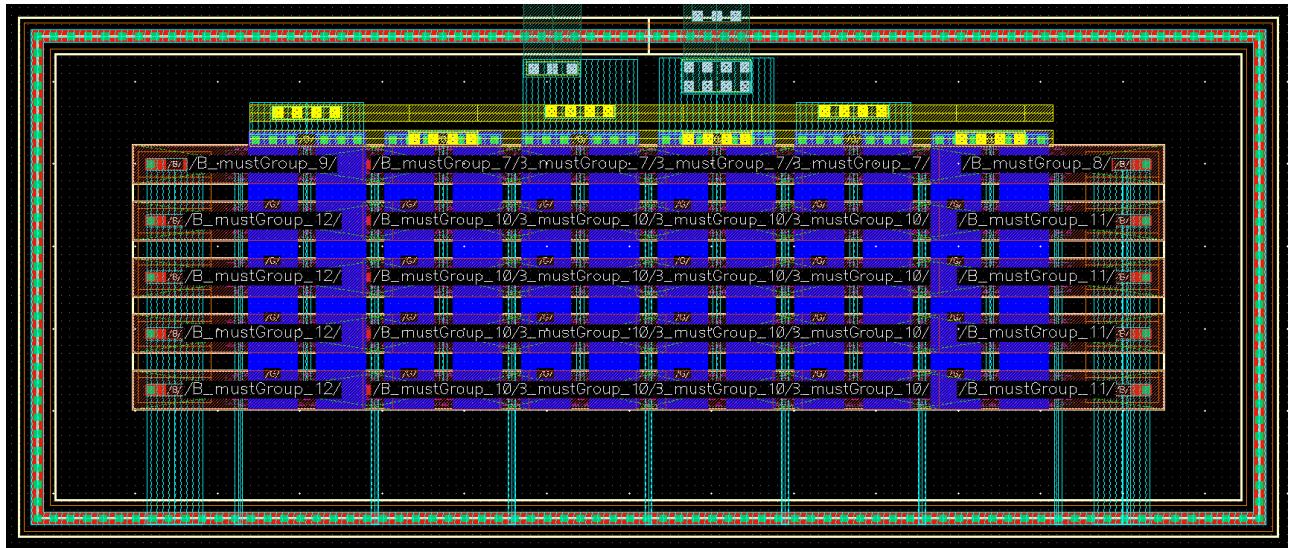


Routing:



- Drains: connect them vertically on metal 1 on the top gates.
- Sources: connect them vertically on metal 1
- Gates: connect them vertically on poly, and combine them horizontally on two nets of metal 2 on the top row.
- Body: through the body of the left and right devices.

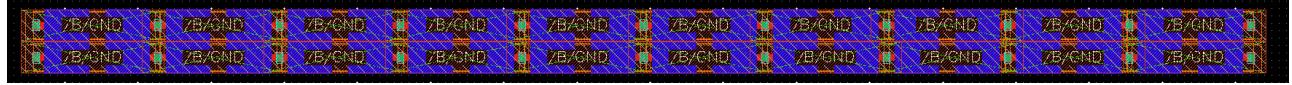
Final Block Layout:



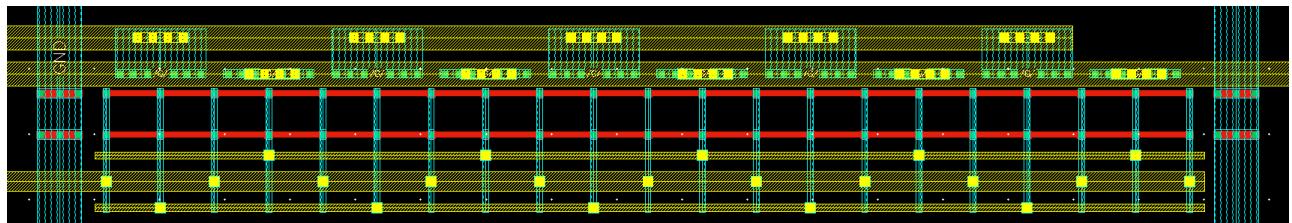
diff Pair sensing: Sharing Diffusion Area:

+ NM5.10	+ NM6.10	+ NM5.4	+ NM6.4	+ NM5.5	+ NM6.5	+ NM5.1	+ NM6.3	+ NM5.8	+ NM6.6
+ NM5.7	+ NM6.7	+ NM5.9	+ NM6.1	+ NM5.2	+ NM6.2	+ NM5.3	+ NM6.9	+ NM5.6	+ NM6.8

Initial Block Layout:

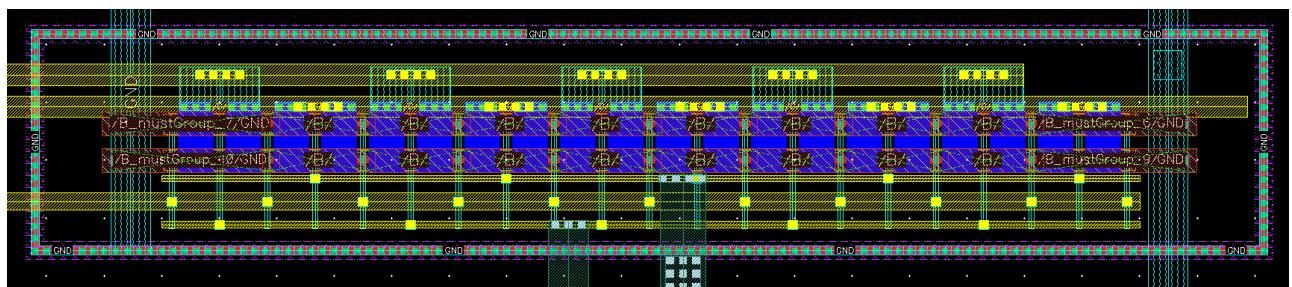


Routing:



- Drains: connect them vertically on metal 1 and combine them on two nets of metal 2 down the block.
- Sources: connect them vertically on metal 1 and combine them on one net of metal 2 down the block.
- Gates: connect them vertically on poly, and combine them horizontally on two nets of metal 2 on the top row.
- Body: through the body of the left and right devices.

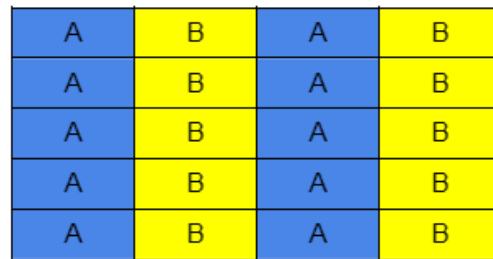
Final Block Layout:



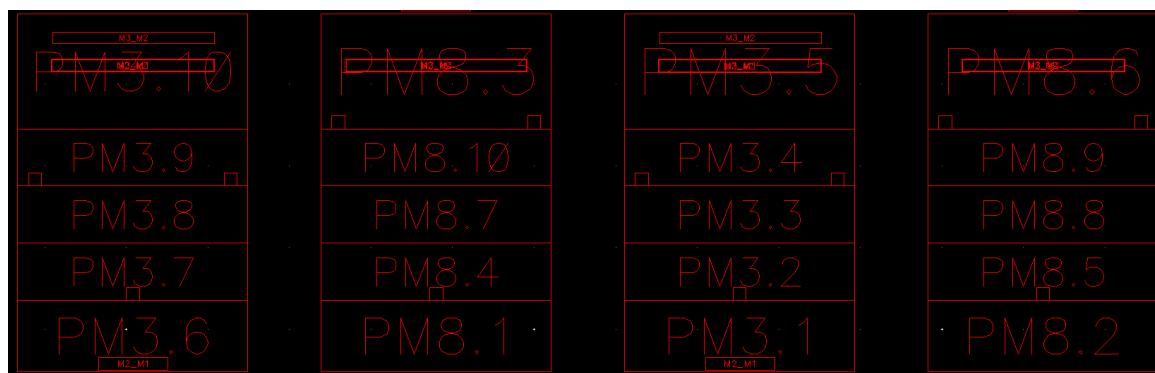
5.2.2.6. Sensing Unit

Instance	Symbol	Function	L(n)	W/F	F	M	W/M	Total W (u)
PM3	A	current Sensor Input	1000	0.4	2	10	0.8	8
PM8	B	current Sensor Input	1000	0.4	2	10	0.8	8

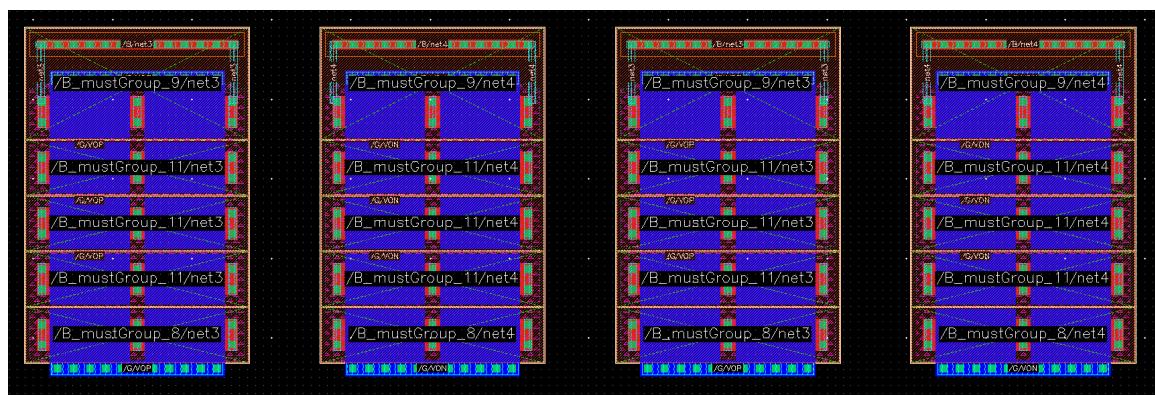
Pattern (interdigitate) :



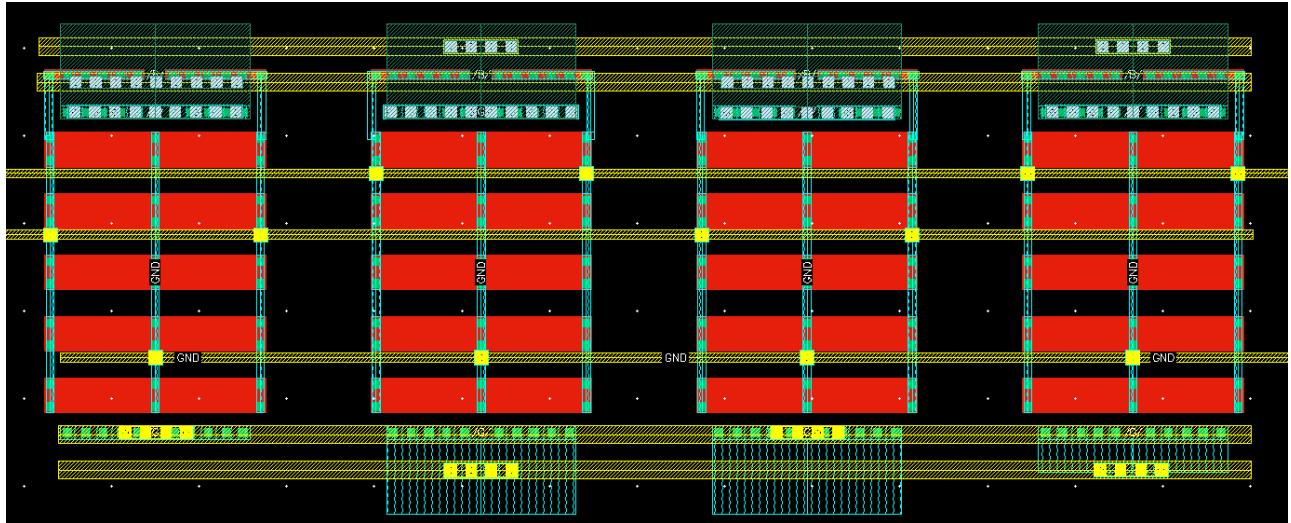
No Sharing for Diffusion Area:



Initial Block Layout:

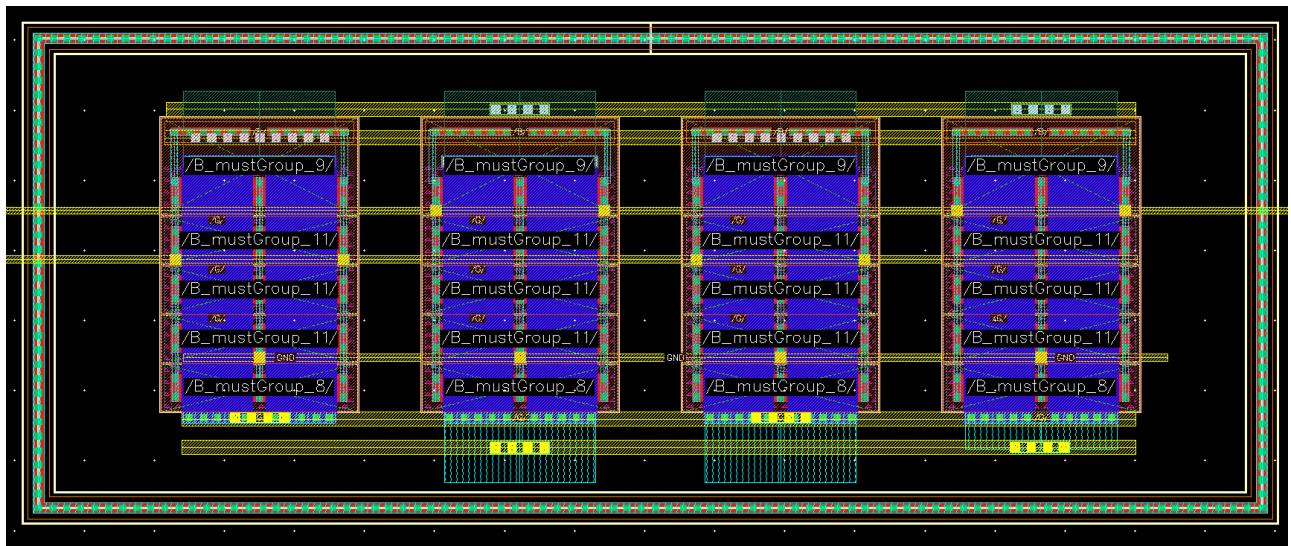


Routing:



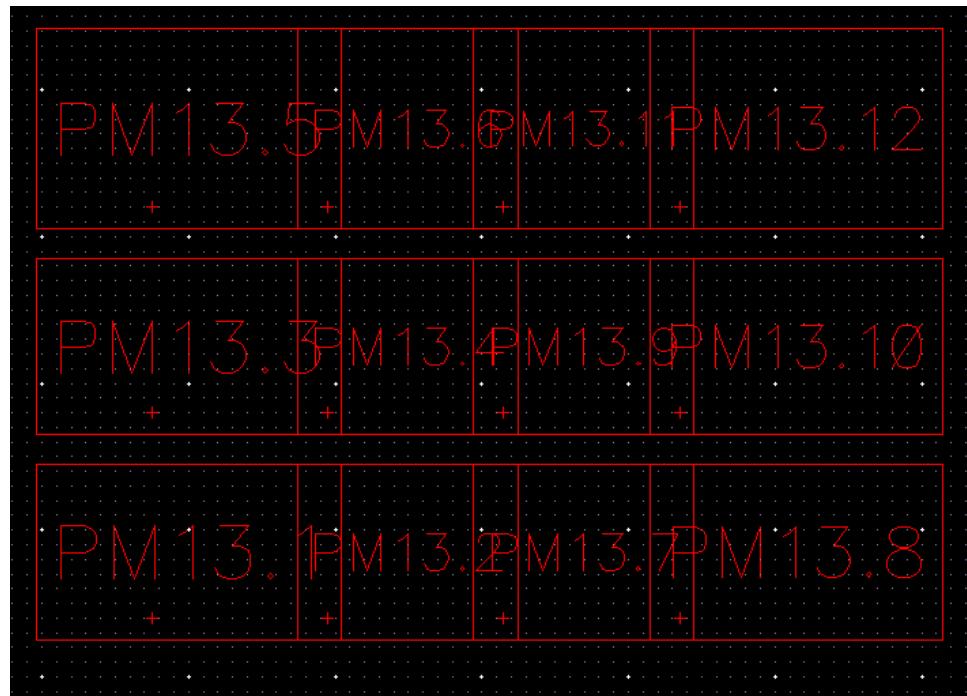
- Drains: connect them vertically on metal 1 and combine them on one net of metal 2 above the block.
- Sources: connect them vertically on metal 1 and the body, and combine them using two nets : metal 2 horizontally and metal 3 vertically, upside the block.
- Gates: connect them on the bottom row and combine them on two nets of metal 2.
- Body: connect the body from top to the sources on metal 1.

Final Block Layout:

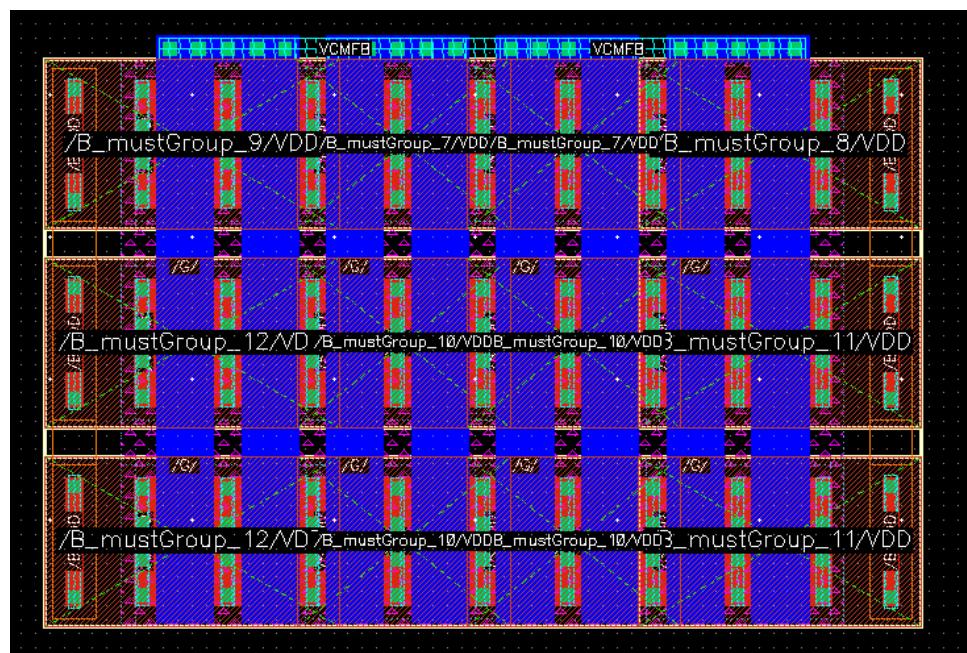


5.2.2.7. Diff Pair Bias

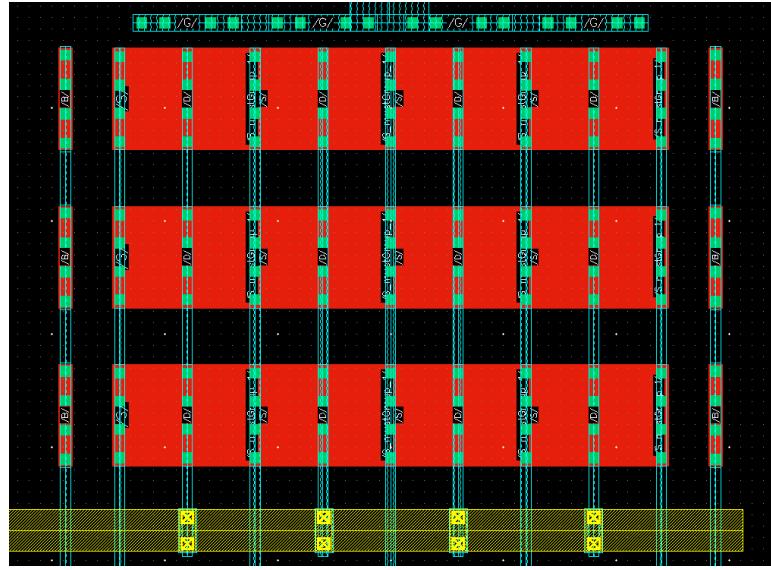
Sharing Diffusion Area:



Initial Block Layout:

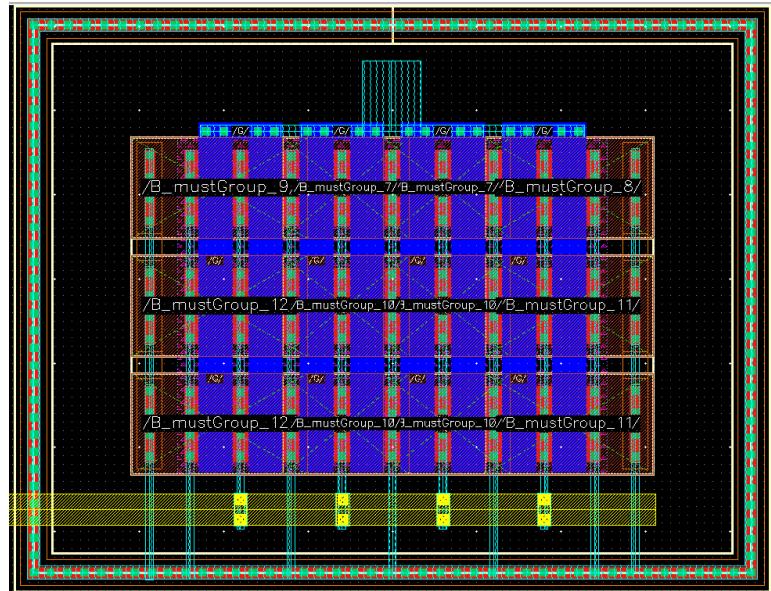


Routing:



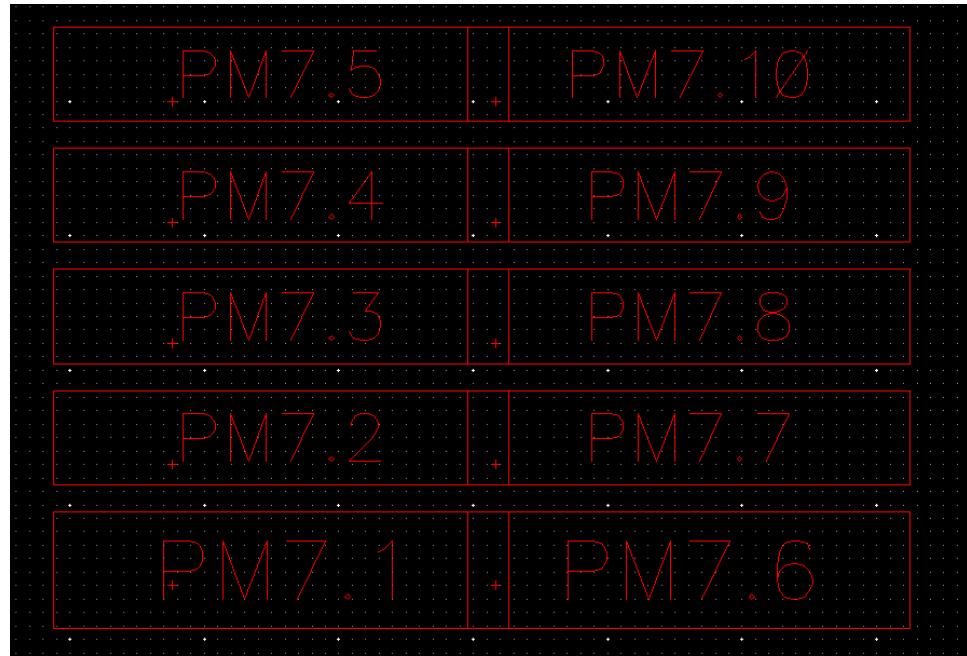
- Drains: connect them vertically on metal 1 and combine them on one net of metal 2 downside the block.
- Sources: connect them vertically on metal 1 and combine them on the guard ring.
- Gates: connect them on the top row on metal 1.
- Body: use the body of the right and left devices.

Final Block Layout:



5.2.2.8. Vref buffer

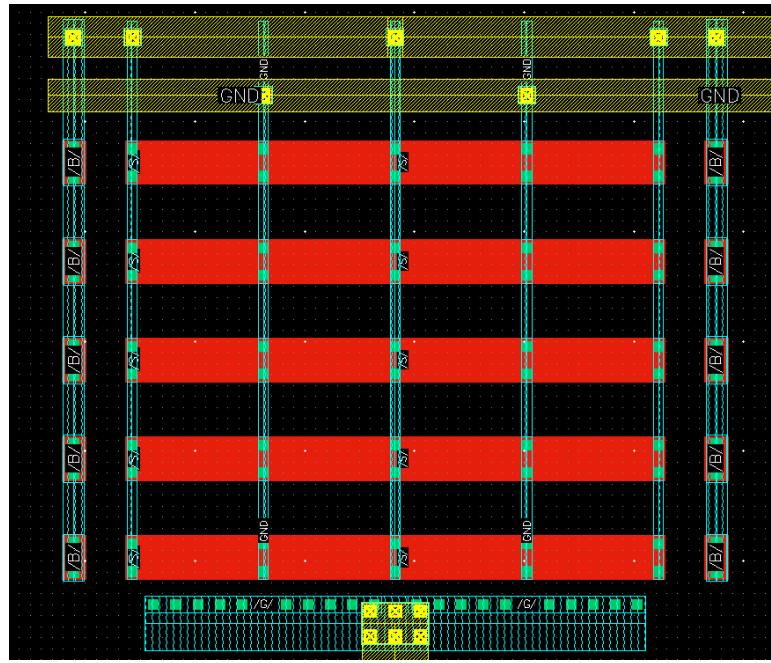
Sharing Diffusion Area:



Initial Block Layout:

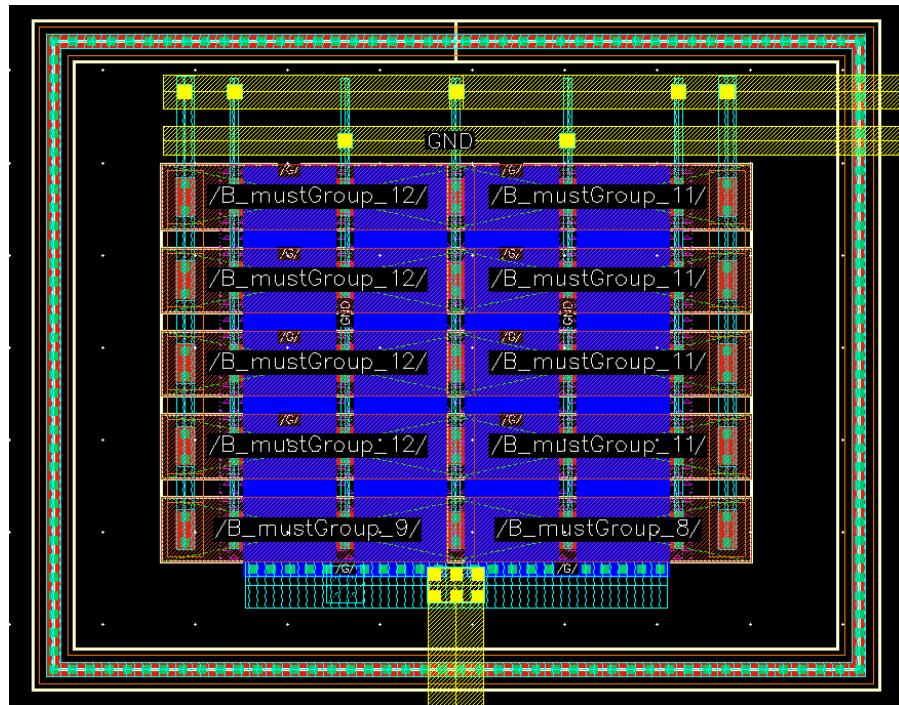


Routing:



- Drains and Sources: connect them vertically on metal 1 and combine them on one net of metal 2 above the block.
- Gates: connect them on the bottom row on metal 1.
- Body: use the body of the right and left devices.

Final Block Layout:



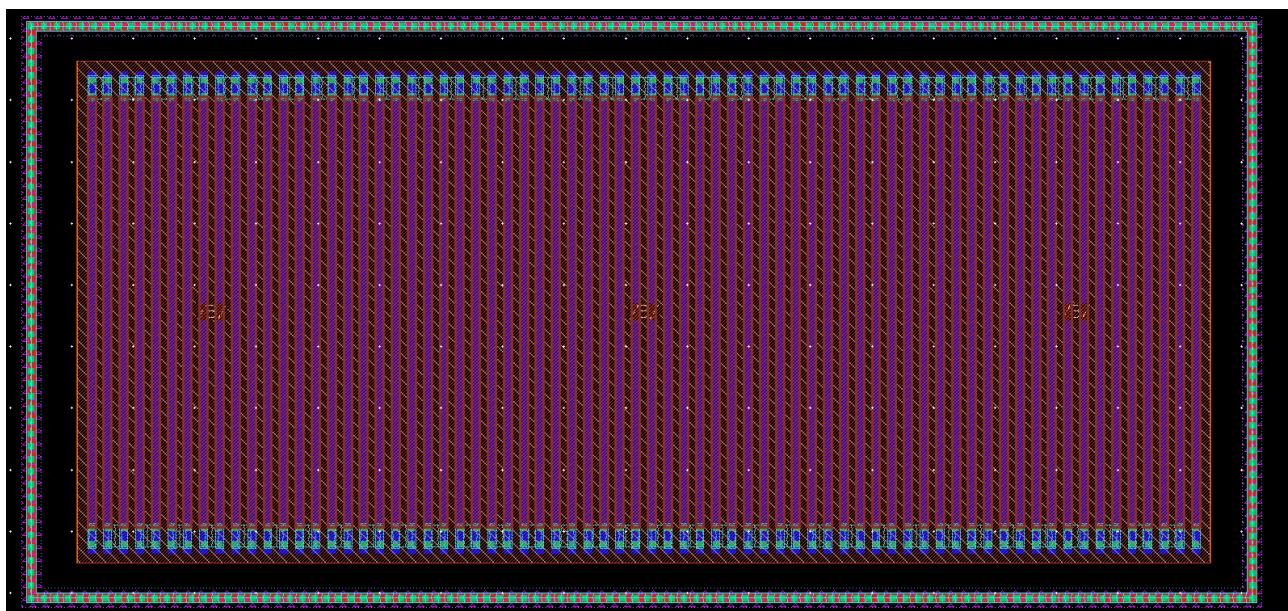
5.2.2.9. Resistors

- We saw that 150k ohm is too large in layout, so we decreased it to 50k and validated the simulation results.
- We chose a poly type resistor through the cell: RSNPO_SP in the umc65 pdk.
- The body terminal of the resistor is connected to the substrate, since its purpose is for noise isolation and not biasing, as we need to maintain the resistance value as stable as possible.
- The body connection is made by guard ringing the resistor by ptap connected to ground.

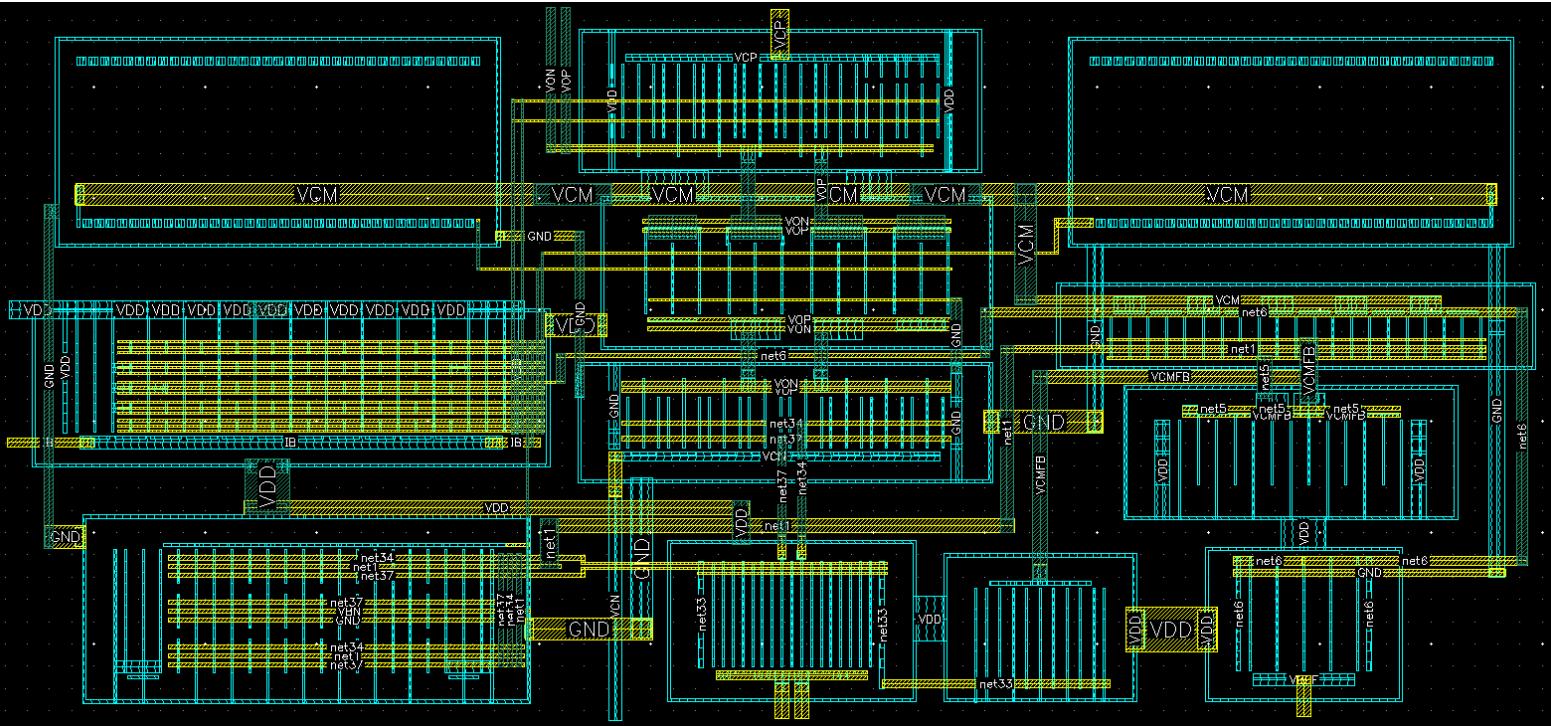
Resistor Parameters:

Segments	70
Segment Connection	Series
Calculated Parameter	Resistance
Resistance	50.6517K
Segment Width	130.0n
Segment Length	7u

Resistor Final Layout:



5.2.3. Global Routing

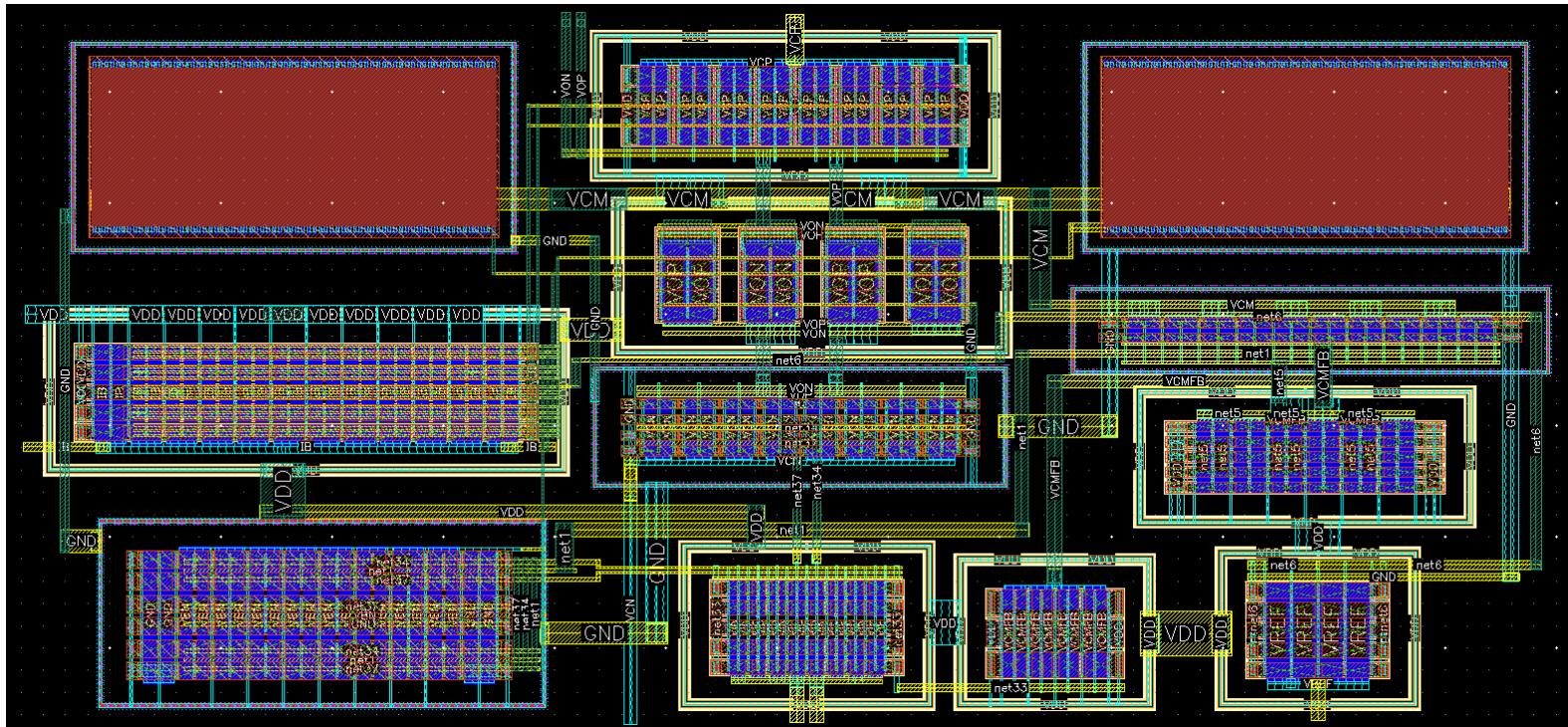


- We routed the nets following manhattan rule, except for short paths.
- Metal stack used: Metals 1,3 (vertically) and Metal 2 (horizontally).
- Pins were created on pin layers for each meal, and assigned labels on layer M_CAD of purpose text for each metal.

We tried to:

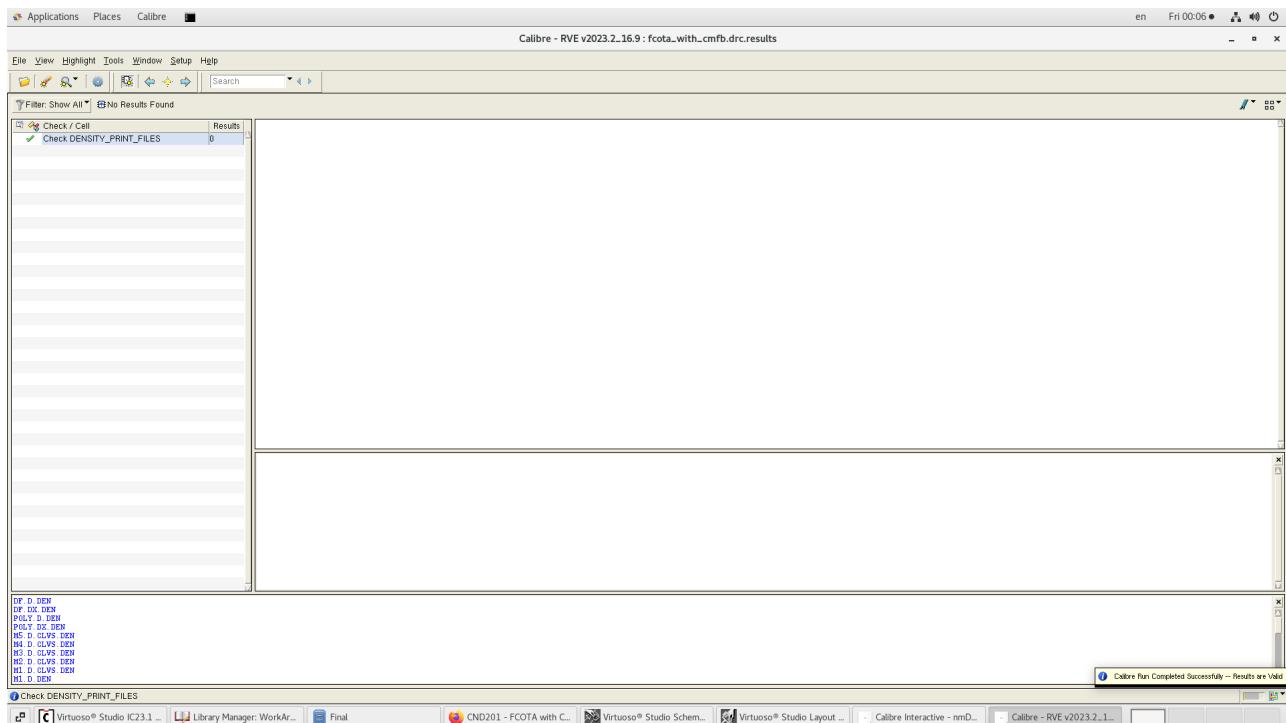
- route the nets as short as possible.
- route the differential nets close to each other with symmetry.
- use dummy nets when necessary to maintain symmetry.
- use large widths for power nets.
- not pass a net above a foreign block but route between the blocks.
- use as many vias as possible to decrease their resistance, hence lower the IR drop.
- for long routes (as VCM) we bridged the metal to avoid antenna effect.

5.2.4. Final Layout

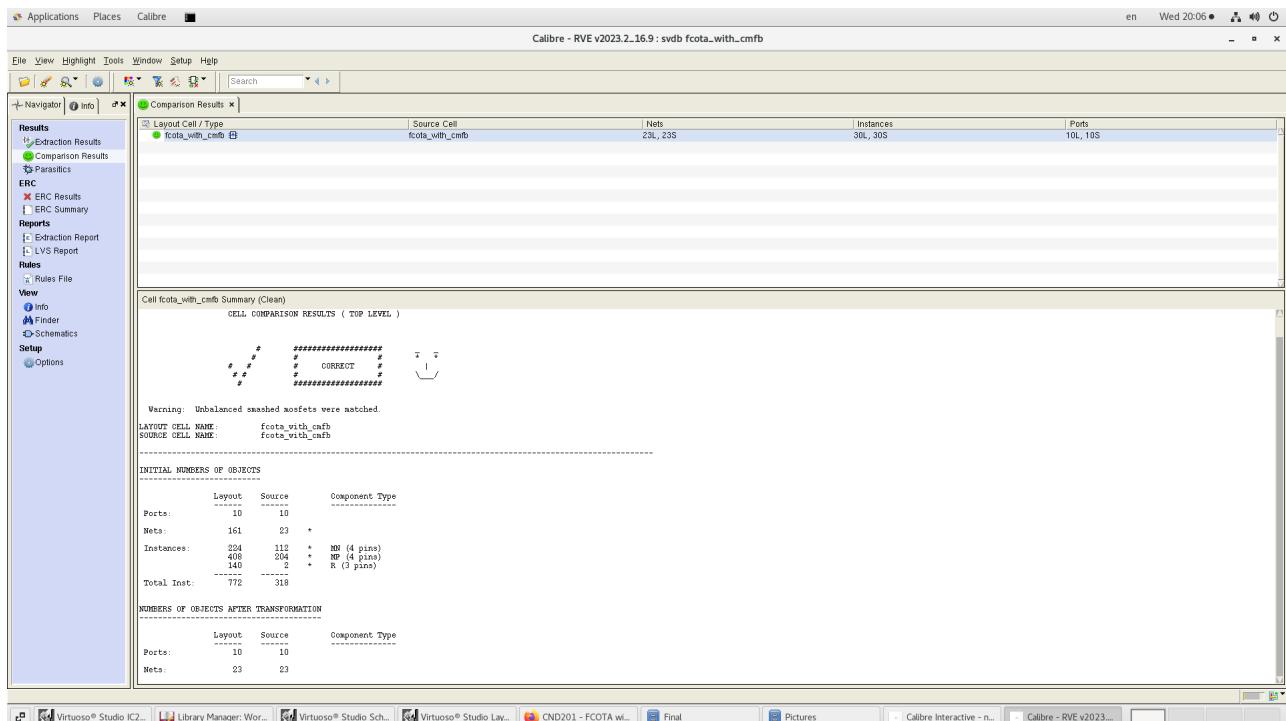


5.3. Physical Verification

5.3.1. DRC: clean



5.3.2. LVS: clean



5.4. PEX

PEX output (through calibre): 161 nets

Applications Places Calibre Interactive - PEX v2023.2_16.9 * en Sat 19:58

Calibre Interactive - PEX v2023.2_16.9 *

File Settings Configurations Help Search

Rules
Inputs
Outputs
LVS
Run Control
Search
Transcript

```
2031 // HIERARCHICAL SEPARATOR /*/
2032
2033 --- OUTPUT NETLIST FILE NAME foota_with_cmfb.pex.netlist
2034
2035 --- PROCESSING PARASITIC MODELS
2036
2037 --- NETWORK REDUCTION BEGIN:
2038 --- READING FROM PDB...
2039 --- BEGIN REDUCING NETS...
2040 --- DONE REDUCING NETS...
2041 --- WRITING TO PDB...
2042 --- NETWORK REDUCTION COMPLETE: CPU TIME = 0 REAL TIME = 0 LVHEAP = 315/318/318 MALLOC = 272/272/281

2043 ===== PDB NET SUMMARY =====
2044
2045 pdb file name = svdb/FOOTA_WITH_CMFB.pdb
2046 root cell name = FOOTA_WITH_CMFB
2047 total nets = 161
2048 top-level nets = 161
2049 non-top-level nets = 0
2050 degenerate nets = 0
2051 merged nets = 0
2052 error nets = 0

2053 ===== CALIBRE XRC WARNING / ERROR SUMMARY =====
2054
2055 ----- XRC Warnings = 6
2056 ----- XRC Errors = 0
2057
2058 ----- CALIBRE XRC:FORMATTER COMPLETED - Sat Oct 5 19:56:11 2024
2059 ----- TOTAL CPU TIME = 1 REAL TIME = 1 LVHEAP = 32/63/318 MALLOC = 275/275/281 ELAPSED TIME = 6
2060
2061 *** xRC run finished with exit code 0 ***
2062
2063
```

Run PEX Start RVE

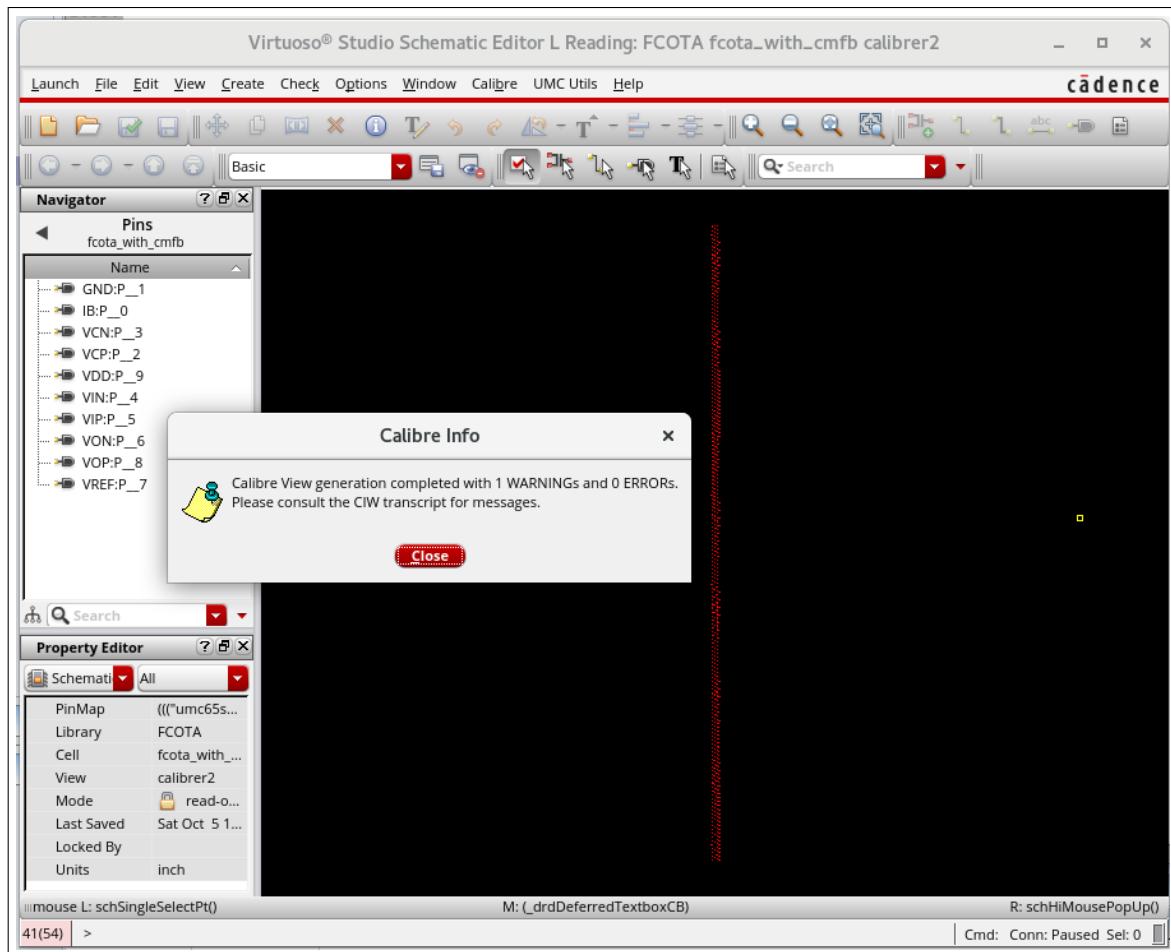
0 Errors, 20 Warnings, 3 Infos

Line	Type	Description
10	Info	Verifying the source netlist is complete before starting the run
91	Warning	Please increase max user process limit (4096) to system limit (15594)
92	Warning	Please increase descriptors limit for best performance (1024)
126	Warning	As of version 2010.3, the following optional keyword to SVRF command 'PEX EXTRACT TEMPERATURE ...' is deprecated: NOMINAL
198	Warning	As of version 2010.3, the following optional keyword to SVRF command 'PEX EXTRACT TEMPERATURE ...' is deprecated: NOMINAL
1000	Warning	Verifying the source netlist is complete before starting the run

Virtuoso® Studio IC23.1 - Lo... Library Manager: WorkArea: ... PEX_demo - Google Drive: ... layout Virtuoso® Studio Schematic E... Virtuoso® Studio Layout Suit... Calibre Interactive - PEX v202...

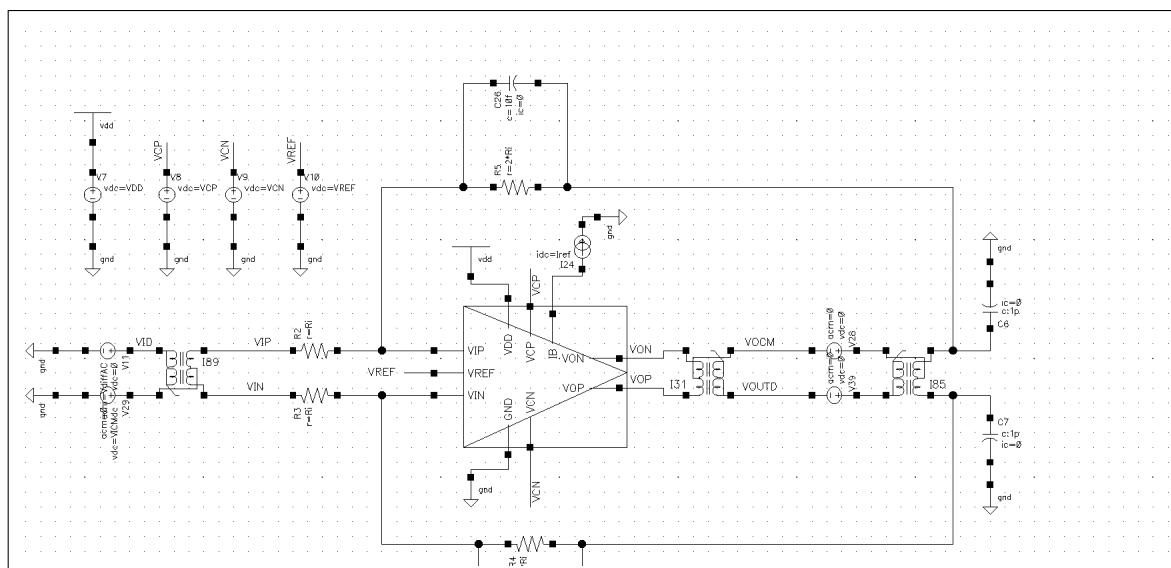
Parasitics listed (R-C-CC):

Calibre view:



5.5. Post layout simulation (closed loop)

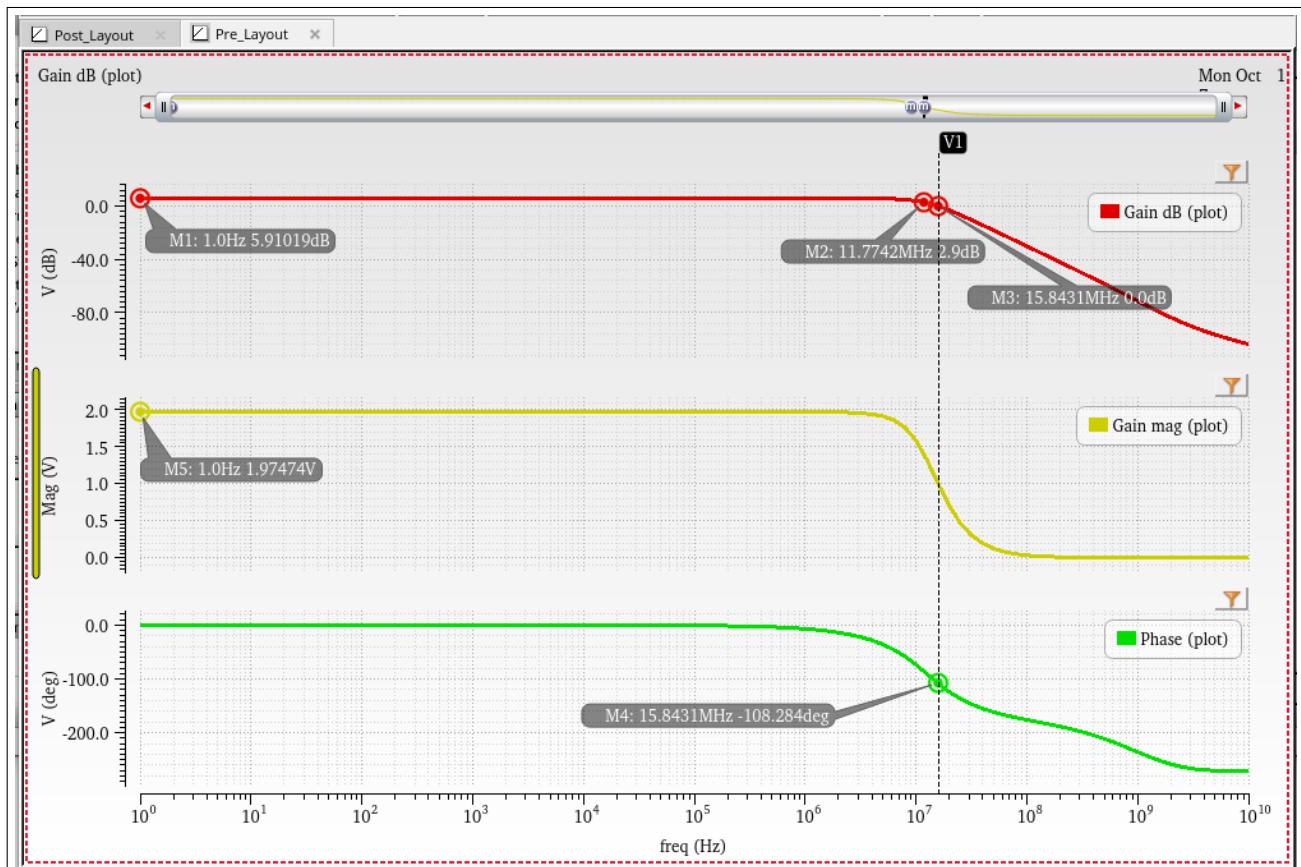
Test Bench:



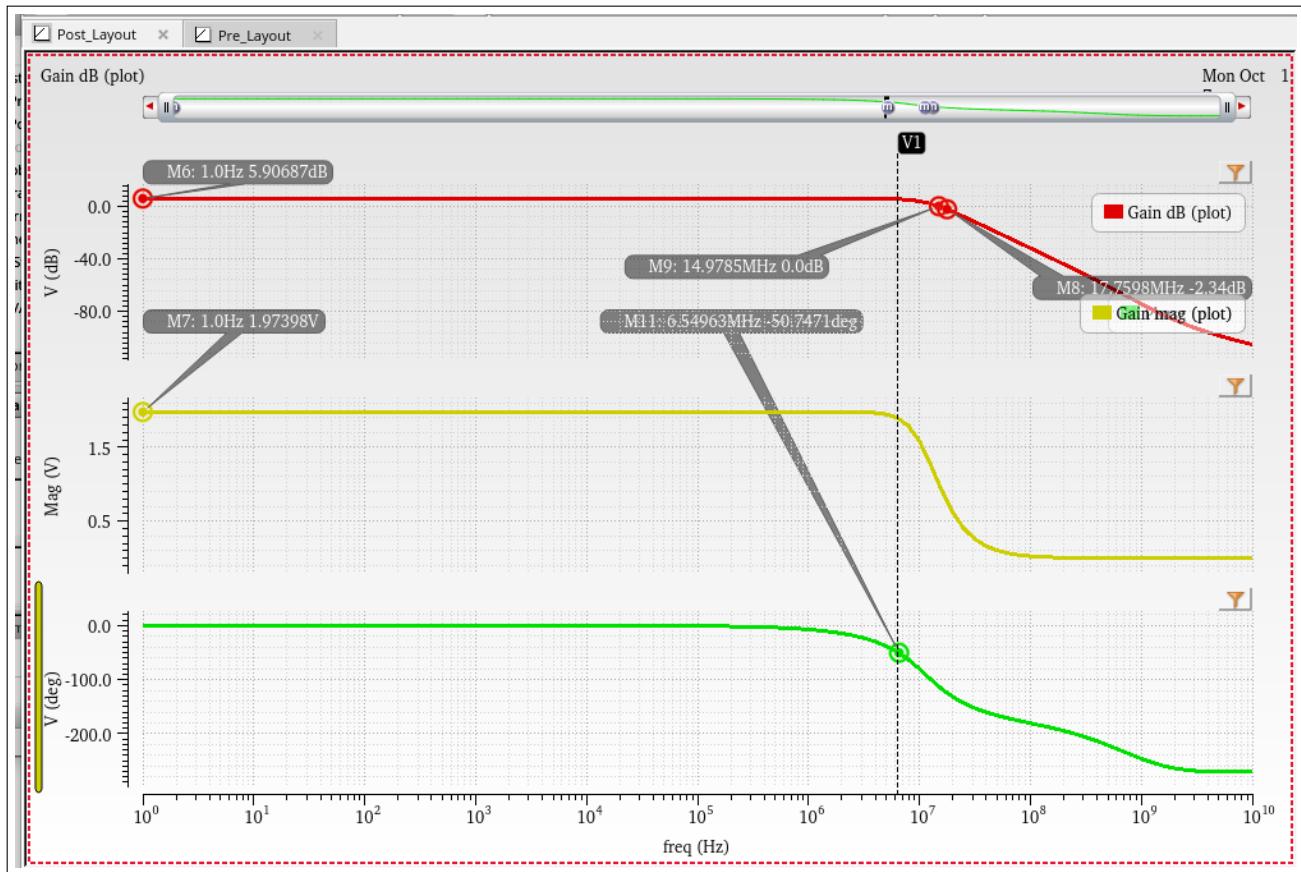
Results Compared to pre-layout:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
Pre_Layout	A_cl	1.975	> 2		near
Pre_Layout	A_cl_dB	5.91	> 6		near
Pre_Layout	BW	11.81M	> 10M		pass
Pre_Layout	GBW	23.32M	> 20M		pass
Pre_Layout	fu	15.84M			
Pre_Layout	Gain dB (plot)				
Pre_Layout	Gain mag (plot)				
Pre_Layout	Phase (plot)				
Post_Layout	A_cl	1.974	> 2		near
Post_Layout	A_cl_dB	5.907	> 6		near
Post_Layout	BW	11.51M	> 10M		pass
Post_Layout	GBW	22.72M	> 20M		pass
Post_Layout	fu	15.08M			
Post_Layout	Gain dB (plot)				
Post_Layout	Gain mag (plot)				
Post_Layout	Phase (plot)				

Plot pre-layout:



Plot post-layout:



Comment: We see no major degradation in the performance. Post layout simulation results are accepted.

End of Submission

Thank You

References

- [1] B. Razavi, “Chapters 3 and 9,” in *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, 2017.
- [2] H. Omran, “Lab 11 (mini project 02) fully-differential folded cascode ota,” in *Analog IC Design Course*, 2021.
- [3] M. Masoud, “Fully differential folded cascode amplifier,” in *Analog Integrated Circuits Designs Course at CND,AUC*, 2024.
- [4] J. S. Jens Lienig, “chapter 6,” in *Fundamentals of Layout design for Electronic Circuits*. Springer, 2021.
- [5] H. Omran, “Optimum split ratio for folded cascode ota bias current: A qualitative and quantitative study,” in *2019 31st International Conference on Microelectronics (ICM)*, 2019.