MIPI Interface Matching Solutions Based on GOWINSEMI FPGA

MIPI is the general standard for communication interconnection between components inside a mobile deceive. The physical layer of MIPI defines the MIPI D-PHY specification, including a camera serial interface (CSI) and display serial interface (DSI).

Figure 1 presents an overview of the electrical features of MIPI DPHY. The MIPI standard mainly has two types of working mode: high-speed (HS) mode and low-power (LP) mode.

- HS mode: Small voltage swing, about 200 mV, used for high-speed data transmission.
- LP mode: Large voltage swing, reach 1.2 V, used for control signal transmission.

Figure 1: MIPI DPHY Electrical Features

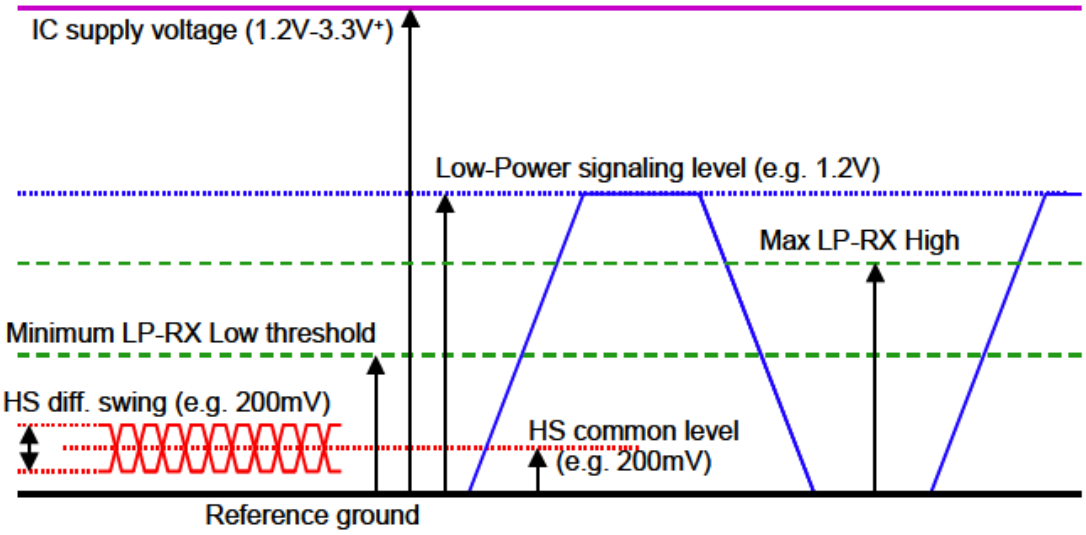


Table 1-Table 4 describe the DC parameters of the sending side and receiving side in the MIPI HS mode and LP mode. Table 5 and Table 6 describe the LVCMOS12 and LVDS25 DC parameters of GOWINSEMI devices. GOWINSEMI LVCMOS12 can meet LP mode electrical features, and LVDS25 can be compatible with HS mode electrical features by adding an appropriate external matching network.

Table 1: MIPI LP Mode DC Parameters - Sending Side

Parameter	Description	Min	Nom	Max	Units	Notes
Voh	Thevenin output high level	1.1	1.2	1.3	V	
Vol	Thevenin output low level	-50		50	mV	
Zolp	Output impedance of LP transmitter	110			Ω	

Table 2: MIPI HS Mode DC Parameters - Sending Side

Parameter	Description	Min	Nom	Max	Units	Notes
Vcmtx	HS transmit static common mode voltage	150	200	250	mV	
ΔVcmtx	Vcmtx mismatch when output is Diff-1 or Diff-0			5	mV	
Vod	HS transmit differential voltage	140	200	270	mV	
ΔVod	Vod mismatch when output is Diff-1 or Diff-0			10	mV	
Vohhs	HS output high voltage			360	mV	
Zos	Single-ended output impedance	40	50	62.5	Ω	
ΔZos	Single-ended output impedance mismatch			10	%	

Table 3: MIPI LP Mode DC Parameters - Receiving Side

Parameter	Description	Min	Nom	Max	Units	Notes
Vih	Logic 1 input voltage	880			mV	
Vil	Logic 0 input voltage, not in ULP state			550	mV	
Vil-ulps	Logic 0 input voltage, ULP state			300	mV	
Vhyst	Input hysteresis	25				

Table 4: MIPI HS Mode DC Parameters - Receiving Side

Parameter	Description	Min	Nom	Max	Units	Notes
Vcmrx	Common mode voltage HS receive mode	70		330	mV	
Vidth	Differential input high threshold			70	mV	
Vidtl	Differential input low threshold	-70			mV	
Vihhs	Single-ended input high voltage			460	mV	
Vilhs	Single-ended input low voltage	-40			mV	
Vterm-en	Single-ended threshold for HS termination enable			450	mV	
Zid	Differential input impedance	80	100	125	Ω	

Table 5: LVCMOS DC Parameters

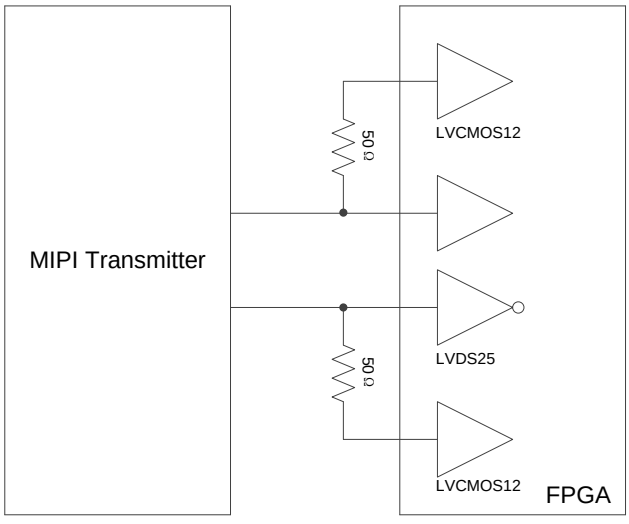
Parameter	Vil Max	Vil Min	Vih Max	Vih Min	Vol Max	Voh Min
LVCMOS12	0.42 V	-0.3 V	3.6 V	0.78 V	0.8 V	0.4 V

Table 6: LVDS25 DC Parameters

Parameter	Description	Min	Nom	Max	Units	Notes
Vthd	Differential input threshold	+/-100			mV	
Vcm	Input common mode voltage	0.05		2	V	
Voh	Output high voltage		1.375		V	
Vol	Output low voltage		1.025		V	
Vod	Output voltage differential	250	350	450	mV	

When FPGA is employed as a MIPI receiving device, the positive terminal and negative terminal of LVDS25 differential pairs are in series with 50 Ω and LVCMOS12. LVCMOS12 outputs 0 in HS mode, which is equivalent to the positive terminal and negative terminal of LVDS25 differential pairs connecting to one 100 Ω resistance, as shown in Figure 2.

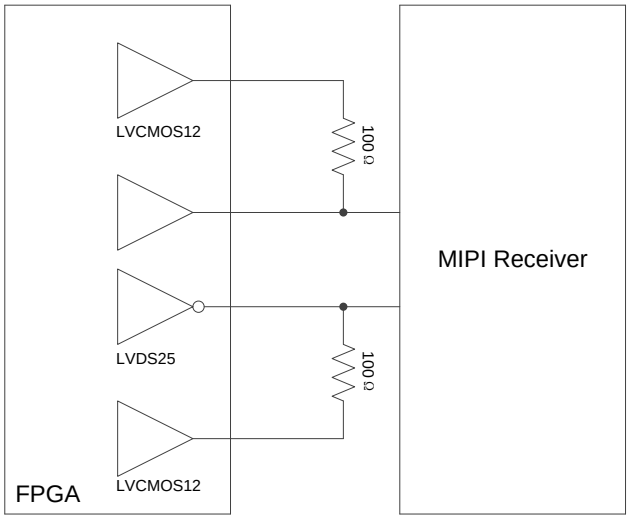
Figure 2: Matching Network - FPGA as a Receiving Device



When FPGA is employed as a MIPI sending device, the matching network is as shown in Figure 3. A 100 Ω resistance and 3.5 mA differential current output by LVDS25 generates bias voltage and results in 0 mV ~ 400 mV differential output.

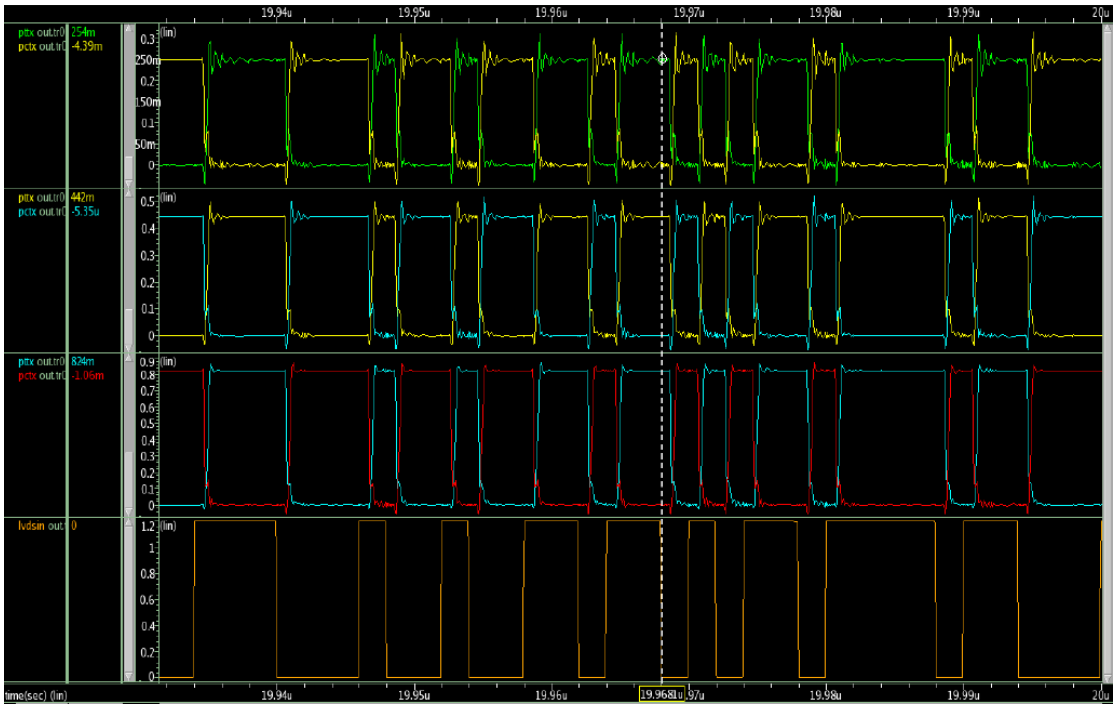
In HS mode, LVDS25 drives output, and the constant output of LVCMOS12 is 0; in LP mode, LVDS25 is in high impedance state and LVCMOS12 drives output. The benefit of this approach is that the 100 Ω resistance can also be terminal resistance, which is advantageous because it ensures the integrality of the high-speed signal. As such, the resistance location needs to be as close as possible to the terminals.

Figure 3: Matching Network - FPGA as a Sending Device



In practical applications, signal attenuation is closely related to PCB. Users can change the resistance value based on actual impedance. Figure 4 shows the simulation diagram of a high-speed signal swing that changes with resistance value.

Figure 4: Simulation Diagram of High-speed Signal Swing Changing with Resistance Value



Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

+Tel: 00 86 0755 82620391

Revision History

Date	Version	Description
03/21/2018	1.0E	Initial version published.

Disclaimer