Gowin FPGA-based DDR2&DDR3

Hardware Design Reference Manual

TN662-1.1E, 01/29/2021

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Revision History

Date	Version	Description
02/11/2019	1.0E	Initial version published.
01/29/2021	1.1E	DDR3 related contents added.

Contents

List of Figures

List of Tables

1 About This Guide

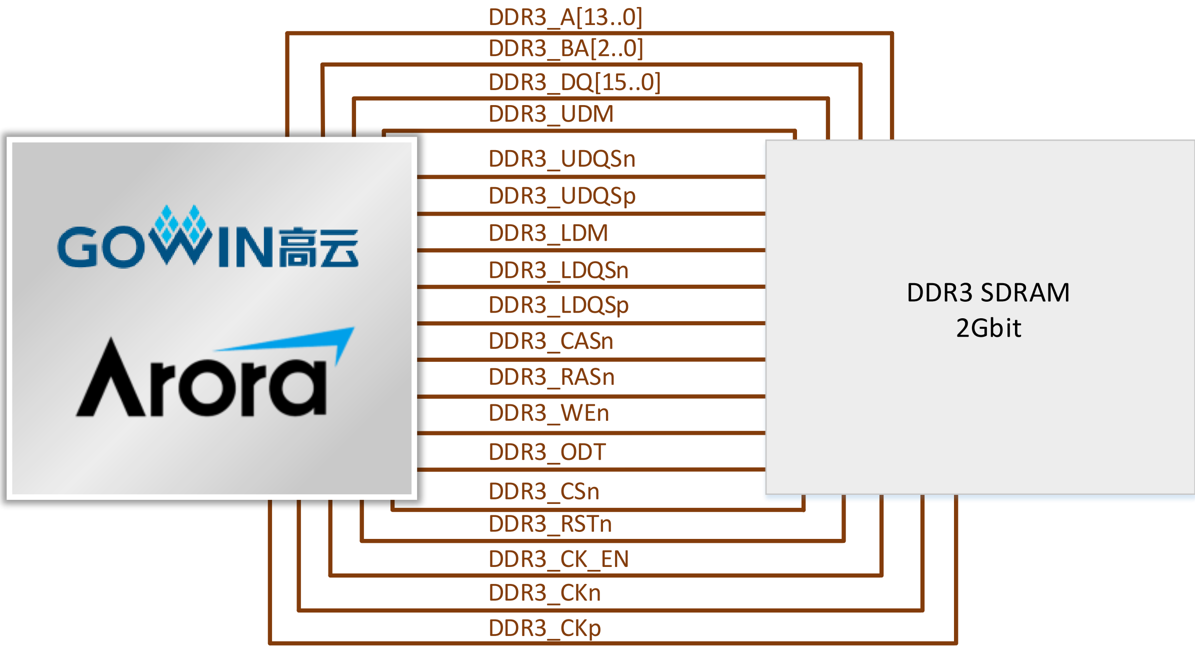
1.1 Purpose

Based on DDR3 devices, this manual mainly introduces hardware design method of high-speed storage circuit, including the I/O distribution, the schematic design, power network design, PCB routing, reference graphic design, and simulation, etc. It aims to help you quickly finish high-speed storage scheme of hardware design with the features of good signal integrity, low power consumption, and low noise.

For the device design method of DDR2, you may refer to that of DDR3. The difference between the two in architecture is very little. The main difference is that DDR3 device bus speed is faster. And DDR3 device power supply voltage is 1.5V, while DDR2 device power supply voltage is 1.8V.

Taking an example of a proven and stable design, this manual systematically introduces the connection between Gowin FPGA and DDR3. The FPGA chip is GW2A-LV18PG256, and the memory chip is a single die package DDR3 SDRAM device of MT41J128M16JT-125:K model manufactured by Micron. The two are point-to-point connection. The connection diagram is as follows.

Figure 1-1 Connection Diagram of Gowin FPGA and DDR3



1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS102, GW2A series of FPGA Products Data Sheet
- UG111, GW2A series of FPGA Products Package and Pinout Manual

1.3 Terminology and Abbreviations

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
PG256	PBGA256 package
OSE8	A serializer of 8 bits parallel input and 1 bit serial output.
OSE8_MEM	8 to 1 serializer with memory
DDR	Double-Data-Rate Synchronous Dynamic Random Access Memory
SSO	Simultaneous switching outputs
SDP	Single die package
ODT	On-Die Termination
PDN	Power Delivery Network
SI	Signal Integrity

1.4 Support and Feedback

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Website: www.gowinsemi.com/en

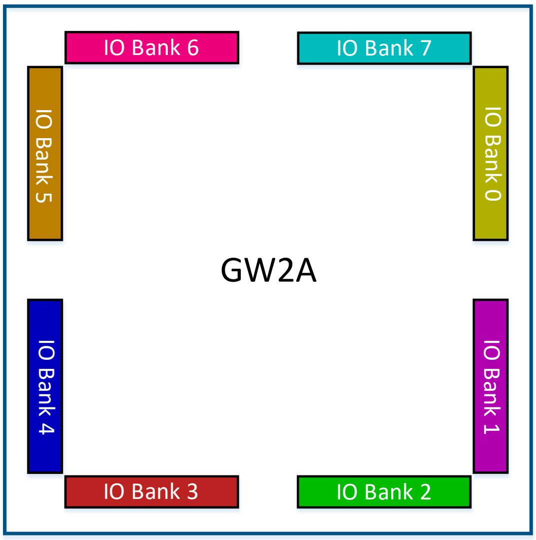
E-mail: support@gowinsemi.com

2 FPGA I/O Distribution

2.1 FPGA I/O Distribution

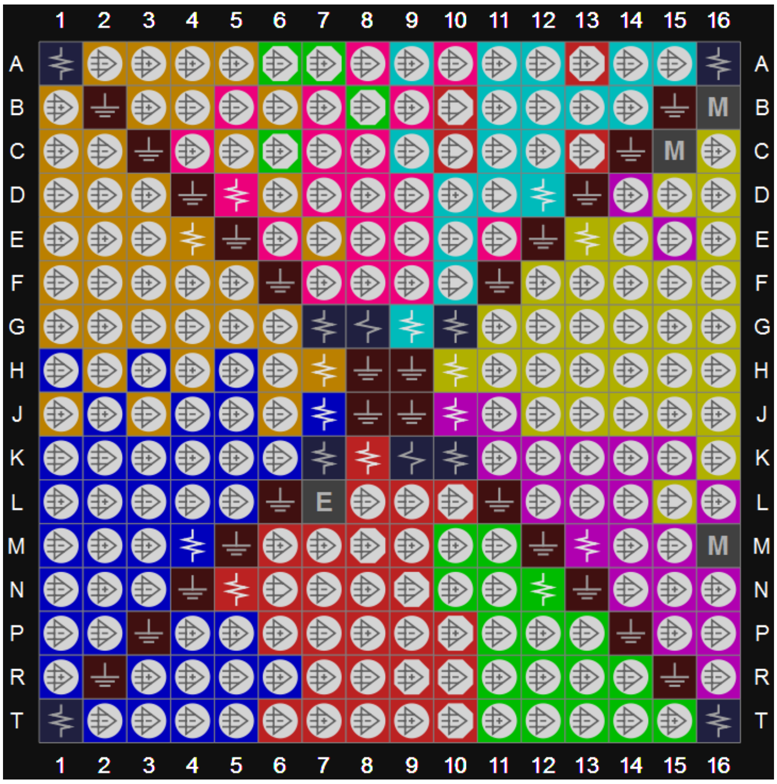
Before DDR3 I/O distribution, the Bank distribution of FPGA devices and the I/O resources of each Bank should be clearly understood. As shown in Figure 2-1, GW2A series FPGA consists of 8 I/O Banks.

Figure 2-1 FPGA Bank Distribution



GW2A-18 PG256 pins distribution is as shown in Figure 2-2.

Figure 2-2 GW2A-18 PG256 Pins Distribution



The number of GW2A-18 PG256 pins are listed in the following table.

Table 2-1 The Number of GW2A-18 PG256 Pin

Pin Type		GW2A-18
		PG256
I/O Single end/Differential pair/LVDS1	BANK0	29/14/10
	BANK1	20/10/10
	BANK2	20/10/7
	BANK3	29/13/10
	BANK4	36/18/12
	BANK5	36/18/11
	BANK6	18/9/8
	BANK7	16/7/5
Max. User I/O		207

2.2 DDR3 I/O Requirement

For MT41J128M16 device and 96pin FBGA package, a total of 47 I/O are required. If CS pin is fixed and lowered, at least 46 I/O are required.

The I/O signals required to connect are as follows.

Table 2-2 DDR3 Signal

Name	I/O Required
DQ[7:0]	8
LDQS,LDQS#	2
LDM	1
DQ[15:8]	8
UDQS,UDQS#	2
UDM	1
CK, CK#	2
CKE	1
A[13:0]	14
BA[2:0]	3
CS#	1
RAS#	1
CAS#	1
WE#	1
ODT	1
Total	47

2.3 I/O Distribution Rule

To ensure the signals of DQ[7:0], LDQSn, LDQSp and LDM data group of DDR3 are distributed in the same DQ cluster of FPGA, DQ5 is allocated in this design.

To ensure the signals of DQ[15:8], UDQSn, UDQSp and UDM data group of DDR3 are distributed in the same DQ cluster of FPGA, DQ6 is allocated in this design.

Clock group, command group and control group signals are not required to be in the same DQ cluster.

The differential clock CK and CK# signals need to be allocated to the global differential clock of FPGA.

2.4 FPGA I/O Mode

According to the I/O circuit design of Gowin FPGA, the data clock frequency of the I/O port can be twice or four times of the main frequency of the internal program, namely supporting 1:2 mode and 1:4 mode.

In the mode of 1:2, if the internal main frequency of FPGA is 100MHz and the data frequency of I/O port is 200MHz, after up and down sampling, the data rate of a single data line is 400Mbps. Common GPIO of FPGA also supports this mode, which can effectively utilize GPIO resources of FPGA.

In the mode of 1:4, if the internal main frequency of FPGA is 100MHz and the data frequency of I/O port is 400MHz, after up and down sampling, the data rate of a single data line is 800Mbps. All single-ended signals and differential signals connected to DDR3 occupy a pair of differential signals on the FPGA. If one differential pair only packages one pin, the pin can be used as a 1:4 mode. Differential pairs are not required to be true LVDS. For example, if DQ13 signal line is connected to IOB32A pin, then IOB32B pin can no longer be connected to other signals of DDR3. Higher data rate can be achieved with this mode.

In order to support high-speed transmission, this design needs FPGA to work in 1:4 mode.

2.5 I/O Distribution

According to the above analysis, FPGA works in the mode of 1:4 and needs 44 pairs of differential signals of FPGA. Bank4, Bank5 and Bank6 are selected in this design to connect DDR3 devices.

Detailed distribution information is shown in the following table.

Table 2-3 Resources Required for DDR3

Name	The Number of Differential Pair	DQ Cluster	The Number of OSE8 and OSE8_MEM
DQ[7:0]	8	DQ5	8 OSE8_MEM
LDQS,LDQS#	1		1 OSE8_MEM
LDM	1		1 OSE8_MEM
DQ[15:8]	8	DQ6	8 OSE8_MEM
UDQS,UDQS#	1		1 OSE8_MEM
UDM	1		1 OSE8_MEM
CK, CK#	1	Not required to be in the same DQ cluster	1 OSE8
CKE	1		1 OSE8
A[13:0]	16		16 OSE8
BA[2:0]	3		3 OSE8
CS#	1		1 OSE8 (can be lowered through resistance)
RAS#	1		1 OSE8
CAS#	1		1 OSE8
WE#	1		1 OSE8
ODT	1		1 OSE8

3 Schematic Design

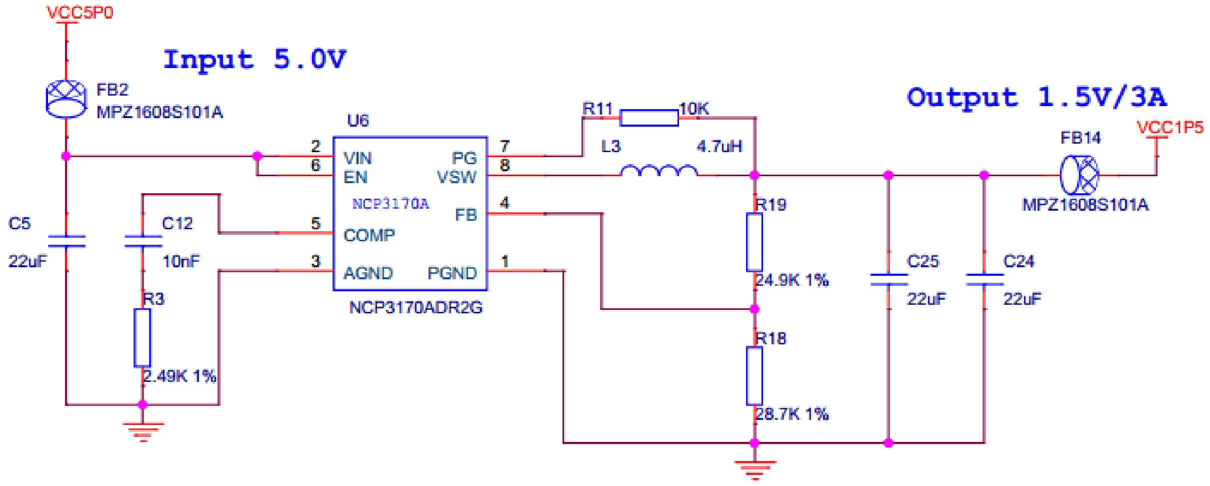
3.1 Power Module

This section only introduces the power supply required by DDR3 devices. For the power module of FPGA, please refer to the schematic document of the corresponding development board.

3.1.1 VDD and VDDQ Power Module

NCP3170ADR2G switching power chip is adopted, and its maximum current is 3A.

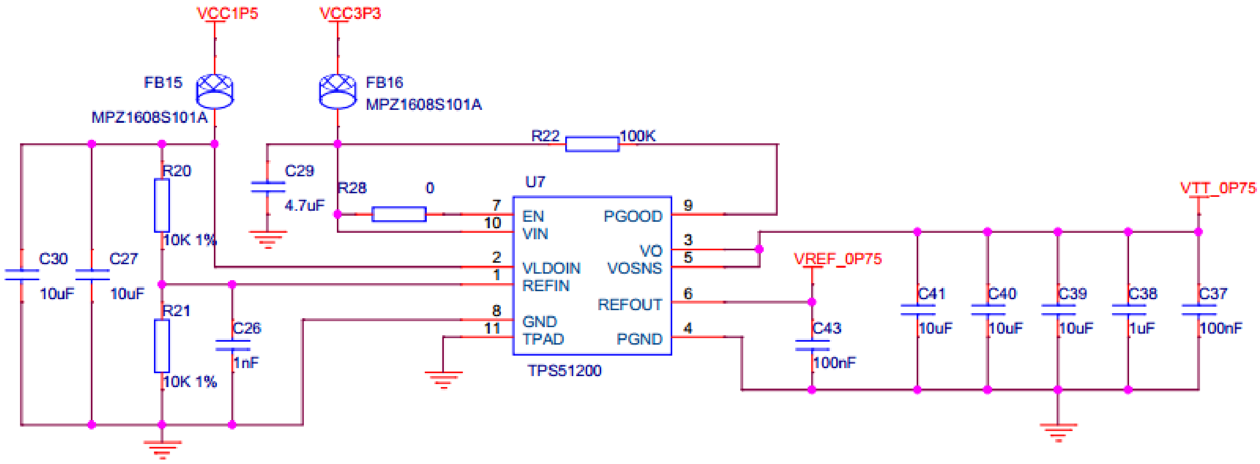
Figure 3-1 VDD/VDDQ Power Module Schematic



3.1.2 VREFCA, VREFDQ and 0.75V Pull-up Power Module

DDR device dedicated power chip is adopted, with push-pull function of the terminal regulator, source current 4A, sink current 5A.

Figure 3-2 VREFCA/VREFDQ Power Module Schematic



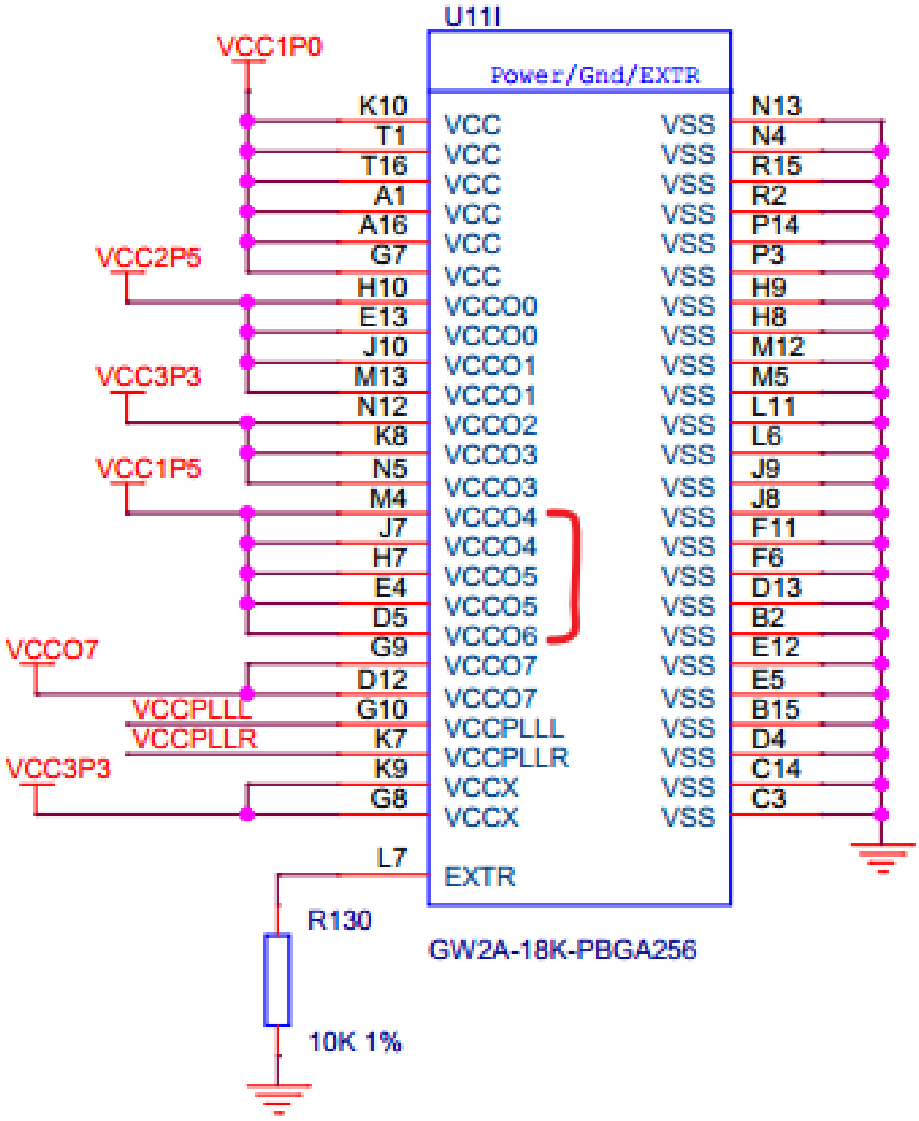
3.2 FPGA Module

The FPGA module design in this section only includes the voltage distribution of FPGA Bank and the distribution of I/O connected with DDR3.

3.2.1 Bank Voltage Distribution

The core voltage of Gowin FPGA is 1.0v, and the voltage of Bank4, Bank5 and Bank6 connected to DDR3 chip is 1.5v, and the voltage of other Banks is distributed as required.

Figure 3-3 GW2A18 FPGA Bank Voltage Distribution Schematic



3.2.2 Bank I/O Distribution

In 1:4 mode, all single-ended signals and differential signals connected to DDR3 both occupy a pair of differential signals on the FPGA. The differential clock of DDR3 is allocated to the global clock of FPGA. Unused differential signals can only be used as simple input ports, such as keys, switches, etc.

Figure 3-4 Bank4 I/O Distribution Schematic

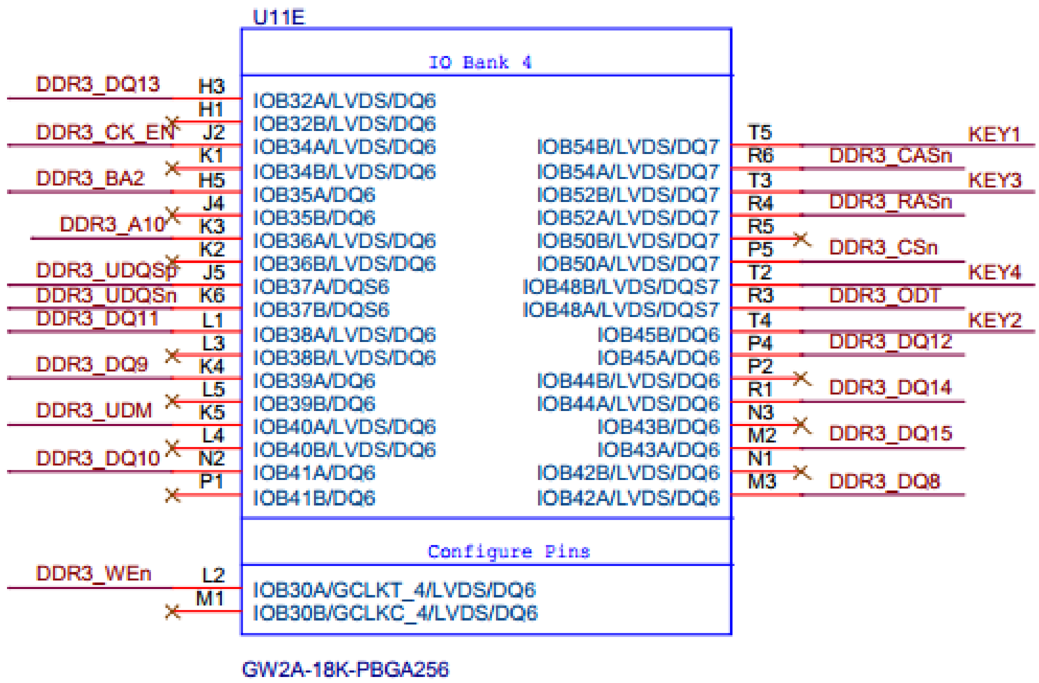


Figure 3-5 Bank5 I/O Distribution Schematic

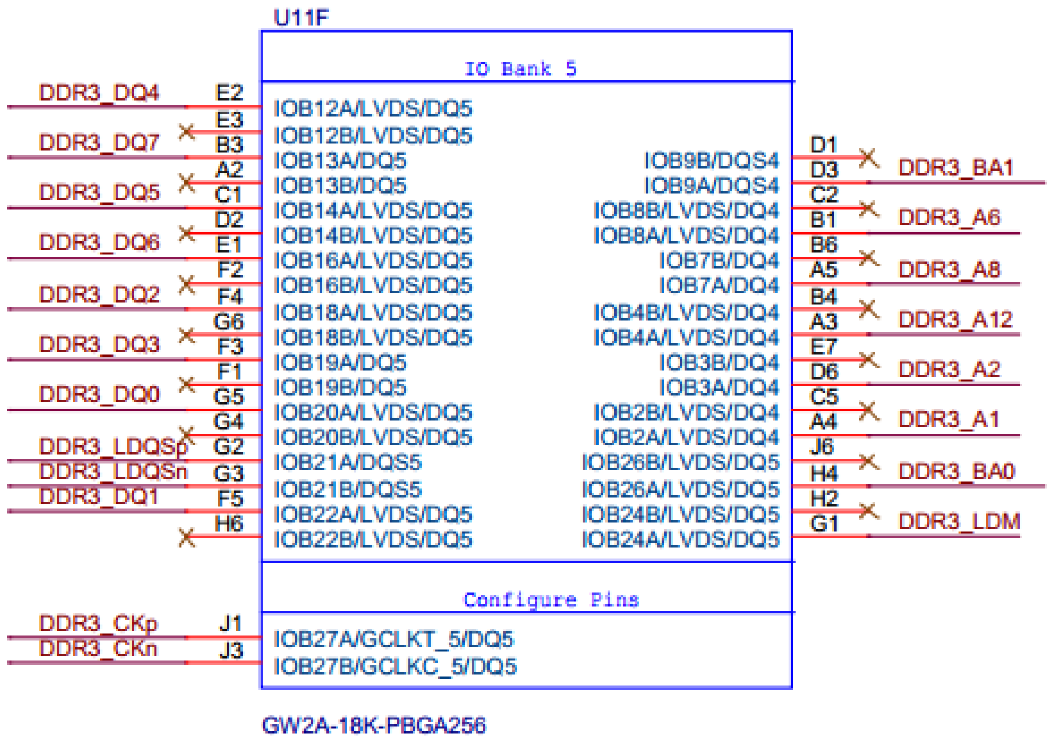
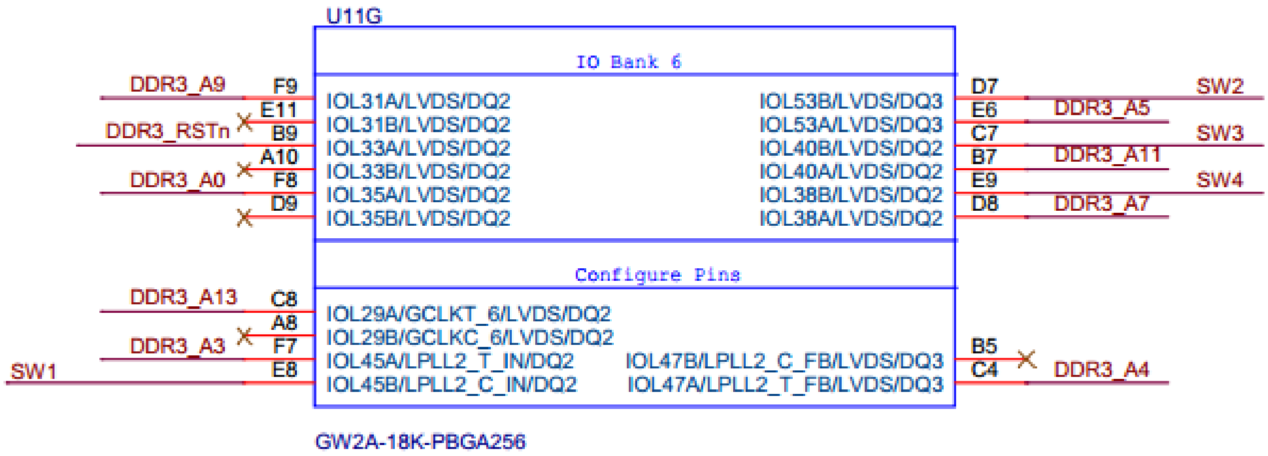


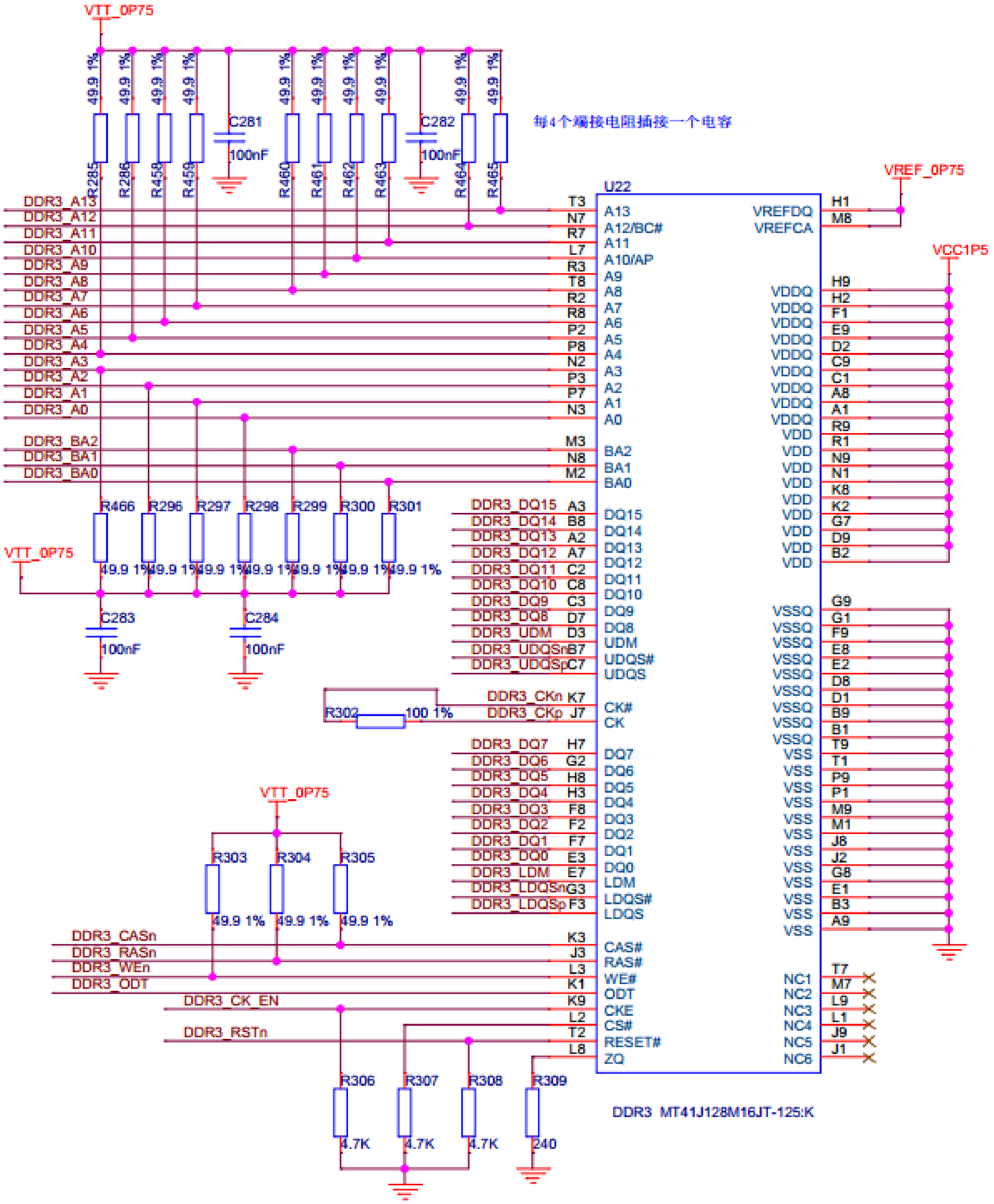
Figure 3-6 Bank6 I/O Distribution Schematic



3.3 DDR3 Design

DQ/DQS signals of DDR3 devices support ODT, and no external terminal resistance is required for the design of DDR3. There is no requirement in this official manual to design 49.9 Ω termination resistance for ADDR/CMD/CNTRL signal lines, but it has been shown to have many advantages. The impedance matching resistance of differential clock is 100 Ω.

Figure 3-7 DDR3 Schematic



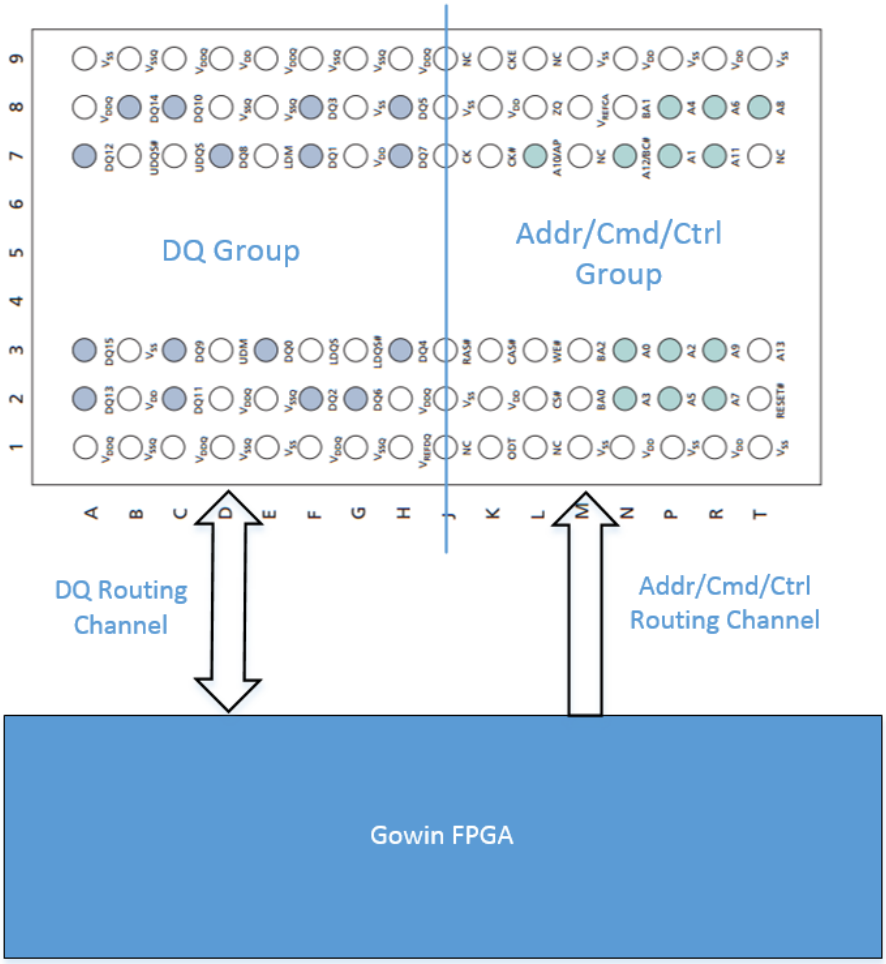
4 PCB Design

4.1 Point-to-Point Topological Structure

4.1.1 Devices Placement

The placement of devices directly affects the difficulty of routing. Reasonable placement not only makes routing easier, but also makes routing shorter and less via, ultimately improving the communication quality of signals The optimal placement and routing of a single device is shown in Figure 4-1.

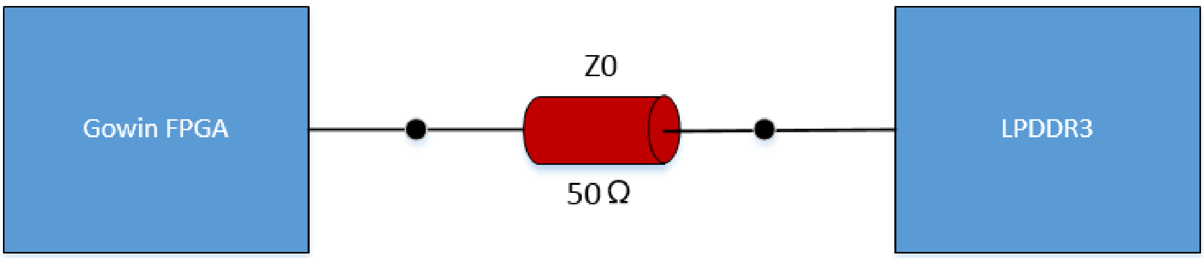
Figure 4-1 Schematic Diagram of Gowin FPGA and DDR3 Placement



4.1.2 Point-to-Point Topology

The topological structure of Gowin FPGA connected to a single DDR3 chip is shown in Figure 4-2.

Figure 4-2 Point-to-Point Connection Topology of Gowin FPGA and DDR3



4.2 PCB Structure

4.2.1 8-Layer Stackup Structure

Well-designed PCB structure is the key to eliminate switching noise.

The ground layer must provide a low impedance return path for the digital circuit Please take account of the ground layer for the routing of all signals as far as possible. The design adopts the 8-layer stackup structure, as shown in the Figure 4-3. The 1st, 3rd, 6th and 8th layers are for signal, the 2nd and 7th are for ground, the 5th is the power layer, and the 4th is the sharing layer for the power and the ground.

The high-speed data line connected with DDR3 is in the third layer, and the ground plane of the second layer is selected as the reference plane, so that the depth of the via is shallower and crosstalk can be reduced. The address line and control line are on 6th and 8th layers. If the high-speed signal is on a lower layer, it will go through deeper via to lead to more coupling jitter.

Figure 4-3 8-Layer Stackup Structure

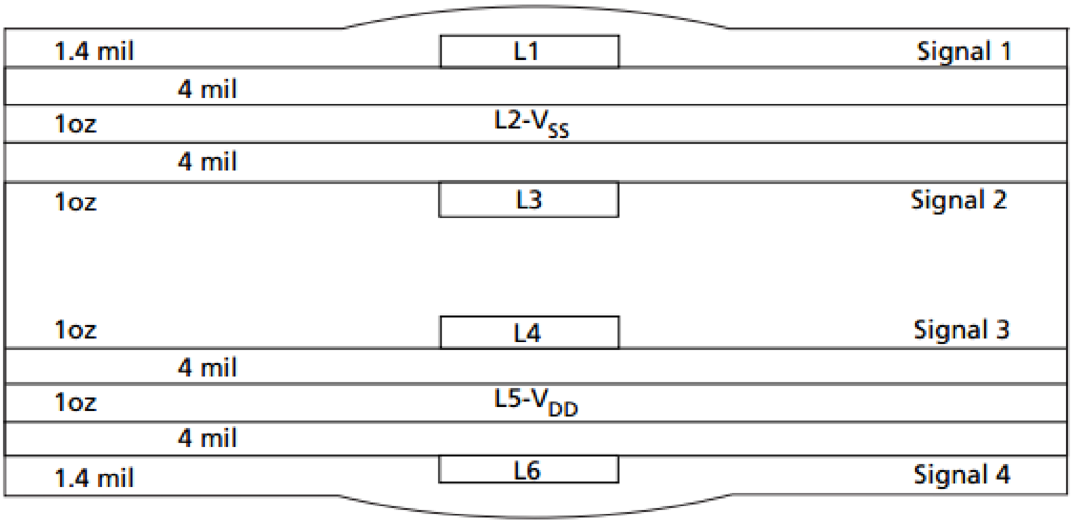
Objects		Types >>		Thickness >>	Physical >>	
		Layer	Layer Function	Value	Layer ID	Material
#	Name			mil		
*	*	*	*	*	*	*
		Surface				
1	TOP	Conductor	Conductor	1.2	1	Copper
		Dielectric	Dielectric	8		Fr-4
2	G2	Plane	Plane	1.2	2	Copper
		Dielectric	Dielectric	8		Fr-4
3	S3	Conductor	Conductor	1.2	3	Copper
		Dielectric	Dielectric	8		Fr-4
4	PG4	Plane	Plane	1.2	4	Copper
		Dielectric	Dielectric	8		Fr-4
5	P5	Plane	Plane	1.2	5	Copper
		Dielectric	Dielectric	8		Fr-4
6	S6	Conductor	Conductor	1.2	6	Copper
		Dielectric	Dielectric	8		Fr-4
7	G7	Plane	Plane	1.2	7	Copper
		Dielectric	Dielectric	8		Fr-4
8	BOTTOM	Conductor	Conductor	1.2	8	Copper
		Surface				

4.2.2 6-Layer Stackup Structure

It is recommended that a minimum of six layers of PCB stack design. The number of signal layers required is determined by the number of storage chips, the number of signals, and the signals space. It is recommended to obtain feedback on signal integrity through simulation. Below is a 6-layer PCB diagram with four inner layers Among them:

- The 1st, 3rd and 4th are for the signal
- The 6th is for signal and power (VDD1)
- The 2nd is for the ground
- The 5th is for power (VDD1)

Figure 4-4 6-Layer Stackup Structure



4.3 Power Delivery Network

4.3.1 PDN

With the increase of data transmission frequency, the timing and noise margin will decrease. The data bus width of DDR3 is 16 bits. In actual running, there are multiple I/O simultaneous switching outputs (SSO). When SSO occurs, a large amount of current is to source or sink into the power delivery network, especially on VDDQ and VSSQ lines. If the PDN is poorly designed, SSO will generate large noise on the power supply, resulting in a series of timing problems.

Hardware design engineers should design a strong PDN for the system board so that all components on the board have a stable power supply. A good and reliable PDN design method is as follows:

1. Make sure the path impedance from the power module to the FPGA and memory devices is as low as possible. The lower the path impedance, the smaller the ripple.
2. Use regional copper if space permits. If space is limited, make sure VDD/VSS and VDDQ/VSSQ are routed as wide as possible.
3. In order to improve the anti-noise ability, VDD/VSS and VDDQ/VSSQ are isolated from each other inside the chip, so the via sharing of VDD and VDDQ, VSS and VSSQ should be avoided as far as possible.
4. Sufficient decoupling capacitors are placed around the FPGA and memory devices to absorb high frequency current burrs.
5. Run complete system simulation to ensure that the PDN is enough strong to maintain a loose margin for peak current requirements.

4.3.2 Decoupling Capacitor

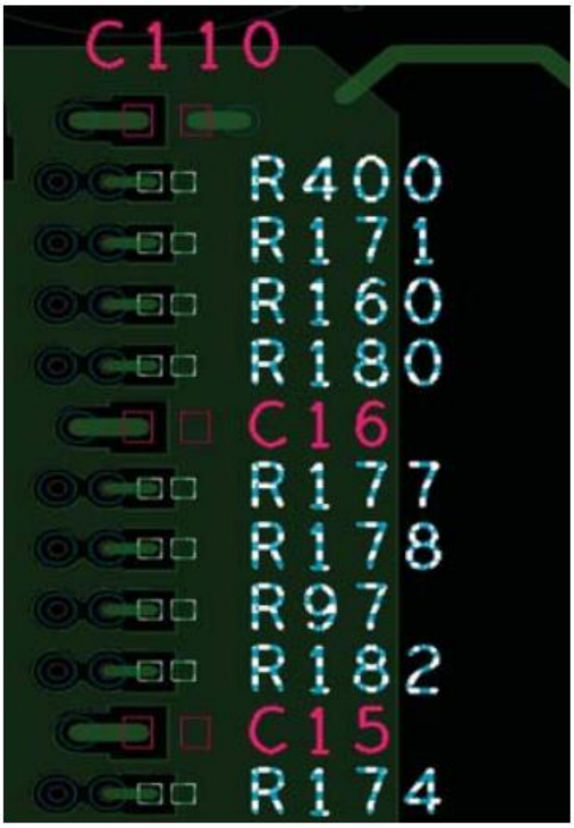
Sufficient decoupling capacitors are placed at appropriate locations on the PCB to prevent transmission errors caused by excessive power supply noise. When the circuit is in operation, the power supply will generate a lot of noise due to high-frequency data transmission. The capacitor placed to restrain power supply fluctuation and provide a current return path for the signal.

The power supply of DDR3 is divided into core power supply (VDD/VSS) and DQ data supply (VDDQ/VSSQ). Since the frequency of core is often lower than that of DQ data bus, the capacitance of core decoupling is larger. It is recommended to select capacitance between 100nF and 1uF. The DDR3 usually has an on-chip integrated capacitor and is not completely dependent on external decoupling, so it is not necessary to assign a capacitor to each power pin.

Usually DDR3 chip and power chip are on the same PCB board, and there are a lot of capacitors with different capacitance values around the power chip, so 100nF decoupling capacitors for VDD/VSS and VDDQ/VSSQ can be considered. Place one at the four corners of the chip, as close as possible to the chip. The connection via is between the capacitor and the chip, and the line width is matched with the via parameters.

For VTT terminal resistance of address, command and control signals, it is recommended that every four terminal resistances are accompanied by a 100nF capacitor whose position is aligned with the resistance, as shown in Figure 4-5.

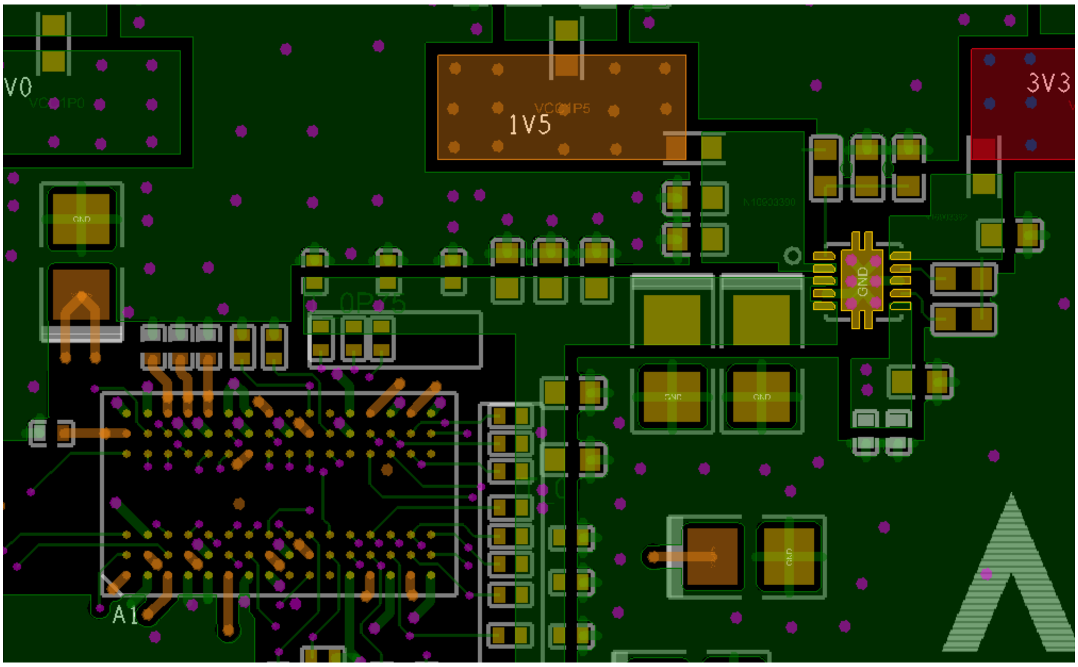
Figure 4-5 VTT Terminal Resistance Interval Decoupling Capacitor Placement Reference Diagram



4.3.3 Power Routing

Power supply voltage VDD, VDDQ, VSS and VSSQ are coppered as much as possible. Connection via routing is as short as possible, less than 8mil is recommended. Any connection from the supply voltage to the via should be as wide as possible, with a recommended line width of 20mil to reduce line impedance. The copper design of the power and the ground is shown in Figure 4-6.

Figure 4-6 Copper Design of the Power and Ground



4.4 Signals Routing

4.4.1 Signal Grouping

In order to facilitate the routing design, it is necessary to define the signal grouping of DDR3 devices, so as to divide the intra-group signal and inter-group signal. DDR3 is divided into five groups: low byte data group, high byte data group, differential clock group, address group and control group. The signals of each group are shown in the table below.

Table 4-1 DDR3 Signal Grouping

Name	Signal Group
DQ[7:0]	Low byte data group
LDQS,LDQS#	
LDM	
DQ[15:8]	High byte data group
UDQS,UDQS#	
UDM	
CK, CK#	Differential clock
A[13:0]	Address group
BA[2:0]	
CKE	Control group
CS#	
RAS#	
CAS#	
WE#	
ODT	

4.4.2 The Same Layer Routing

According to the signal grouping in the above section, the signals in the same group should be routed in the same layer, so as to keep the impedance of the intra-group signals continuous and consistent. Especially for data group signals, the requirement for the continuity of impedance is higher. The data group signals must be changed through the same via and the same layers, and the number of via cannot exceed two. Hierarchical routing of data groups, addresses, controls, and clocks are needed where possible.

On the other hand, the propagation delay is different because of the dielectric constant of inner and outer layer. The dielectric constant of the inner layer is determined by the glass and resin of the PCB. The outer layer is composed of PCB material, surface soldering layer, air and other materials of different properties. Generally, external routing reduces propagation delay by 10% compared with internal routing, and external routing signal transmission is faster. This difference can be ignored if all the routing that need to be matched have the same percentage of outer and inner routing. Otherwise, this difference should be taken into account when calculating any latencies or matches.

4.4.3 Trace width

Considering the space condition and impedance requirement of the whole PCB board, it needs to select the suitable trace width and trace spacing. The single-ended signal in this design chooses trace width of 6 mil, target impedance values of 50 Ω; Differential signal trace width is 4.5 mil, spacing of 9 mil, target impedance value of 100 Ω.

The recommended trace width is shown below.

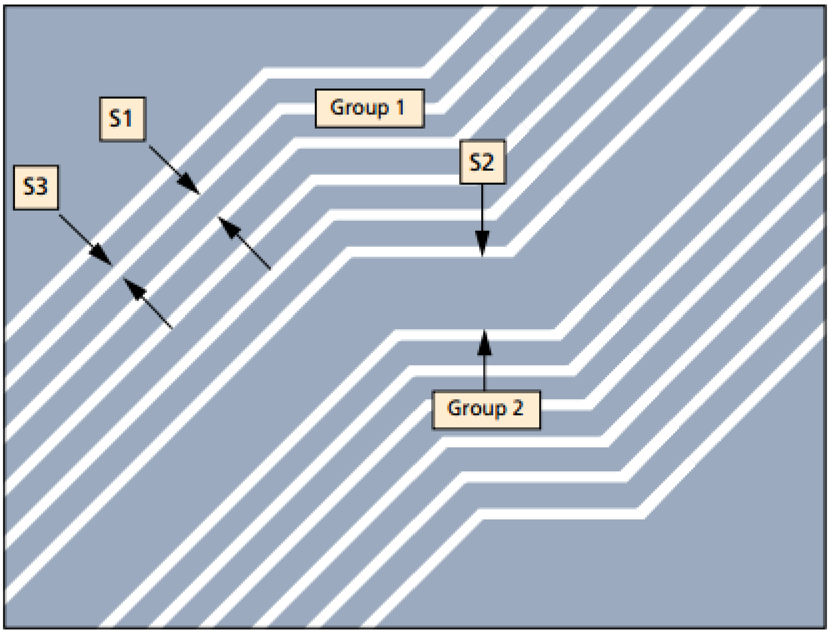
Figure 4-7 Recommended Trace Width

- DQ lines = 4 mil minimum, 6 mil nominal
- DQS lines = 4 mil minimum, 6 mil nominal
- Address lines = 4 mil minimum, 6 mil nominal
- Command/control lines = 4 mil minimum, 6 mil nominal
- Clock lines = 4 mil minimum, 6-10 mil nominal

4.4.4 Spacing

Inter-group spacing and inter-group spacing both have effects on signal integrity. As shown in Figure 4-8, Group1 and Group2 are signals of different groups, S1 is intra-group spacing, S3 is trace width, and S2 is inter-group spacing.

Figure 4-8 Intra-group and Inter-group Spacing Siganl



The recommended spacing depends on the thickness of the medium between the routing layer and the reference layer. Generally, it is recommended that the spacing is 3 times the thickness of the medium. The recommended intra-group spacing (S1) is 12mil on average and 8mil minimum. The recommended inter-group spacing (S2) is 20mil and 8mil minimum. Crosstalk can affect signal integrity (SI) if all signals are routed at 8mil throughout the whole course. If the short spacing exceeds the limit, there are little effect on the signal integrity.

Crosstalk is a function of spacing, dielectric thickness and signals transition frequency. For the signals transition frequency less than 1v/ns, the spacing can be closer. A low-speed system usually has more timing margin and can accommodate more crosstalk without affecting SI.

4.4.5 Length

When other conditions are met, the shorter the routing between the FPGA and the DDR3, the better. If the length is less than 1000mil (2.5cm), the routing is simpler and the signal quality is usually increased proportionally.

For single chip design, it is easy to meet the length of about 1000mil. The length of this design is about 1200mil. However, in most cases, especially in multi chips design, the length will be greater than 2000mil (5cm), which will lead to more undershoot, overshoot, ringing and other phenomena affecting the signal integrity, which needs to refer to the mature design provided by the official.

4.4.6 Equal Length

DDR3 devices have strict requirements on the signal length. In fact, the equal length is to keep the signal delay consistent. The transmission delay of 1000mil (1inch) routing is about 165ps. For an 800 MHz clock frequency, the clock cycle is 625ps. It makes more meaningful to consider the signal offset as a percentage of the period: 625ps * 1% = 6.25ps; 6.25 ps is about 40 mil. To match the length to within 1% of the clock cycle, it is required to match the routing to within 40mil, that is, the error is controlled within ±20mil.

The vias should be the same for equal length matching routing. The vias represents the additional length in the z-axis direction. The actual length of the vias depends on the starting and ending layers of the signal. Since all vias are different, it is not possible to specify the same delay value for all vias. The vias delay caused by stray inductance and capacitance exceeds the delay caused by the vias channel length. The maximum vias latency is 20ps. This number includes the delay based on z-axis and the delay caused by LC. Due to the complexity， it is recommended to use the same number of vias with the same parameters for matching routing.

Requirements of DDR3 devices for equal length signal are summarized as follows:

1. Data intra-group signal: The error is controlled at ±20mil, and DQS difference pair is set as the maximum in the group.
2. Address/control intra-group signal: The error is controlled within ±20mil.
3. Inter-group signals: The error is controlled within ±50mil.
4. The recommended routing length of the clock line is 250mil (42ps) longer than the average value of other bus lengths. This is because the differential signal has stronger anti-noise ability and better signal integrity than the single-ended signal, so the differential clock is faster than the single-ended signal transmission.
5. Differential intra-pair signal: The error is recommended to be controlled at 10mil.

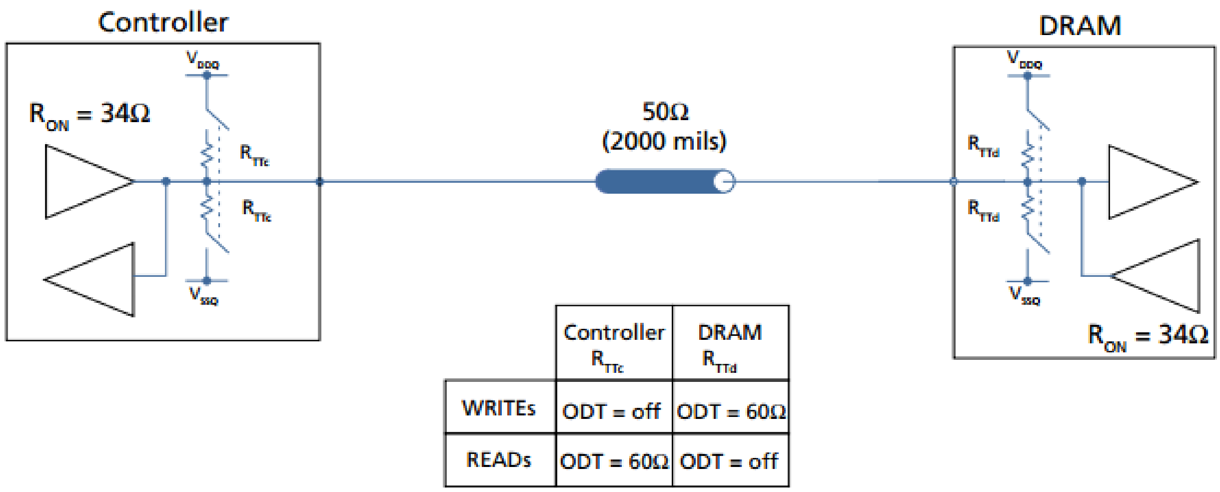
4.4.7 Impedance Matching

It is recommended the impedance (Z0) 50 Ω for all single-ended routing. The error is ±10%. The differential signal impedance is 100 Ω, and the error is ±10%. Impedance values in this range are well matched with those of DDR3 devices and FPGA devices. The Z0 is usually specified by the designer, and eventually the PCB manufacturer adjusts the thickness and trace width of the medium to meet the impedance requirements.

When the drive impedance matches the routing impedance, the best signal quality can be obtained. The DQ bus of the DDR3 device supports On-Die Termination (ODT), which enables the device to dynamically control whether the DQ bus connects to the termination resistance. Combined with the programmable drive of the DDR3 device, this increases the system flexibility and provides more accurate impedance matching in point-to-point system.

For the DQ bus termination resistance, this design uses DDR3 ODT function. When in write operation, DDR3 internal ODT is set to 60 Ω; In reading, the internal ODT is closed, 34 Ω or 40 Ω drive strength can be chosen, as shown in Figure 4-9.

Figure 4-9 Data Bus Termination Scheme



Based on the simulation, ADDR/CMD/CNTRL signal lines are suggested to be connected to Ω 40-60 Ω VTT termination resistance in order to enhance signal driving ability. The ADDR/CMD/CNTRL signal line in this design is connected to 49.9 Ω termination resistance, which has been shown to have many advantages.

4.5 The Reference Plane

4.5.1 Continuous Reference Plane

Signal line routing must have a continuous reference plane to avoid hollowing out area across the reference plane, as shown in Figure 4-10. The routing with reference plane and vias edge should be maintained at least 30mil, as shown in Figure 4-11, except for signal fan-out area. All signal groups must have a complete VSSQ or VDDQ reference plane.

For read-write operations, the key signals are CK/ CK#, DQ, DM and

DQS, which run twice as fast as other signal groups and require higher signal integrity. DQ, DQS and clock line are preferably to choose VSSQ as the reference plane to reduce the noise to the minimum. If the VSSQ plane is not easy to reference, address and command signals can refer to the VDDQ plane.

Figure 4-10 Trace Spanning Split

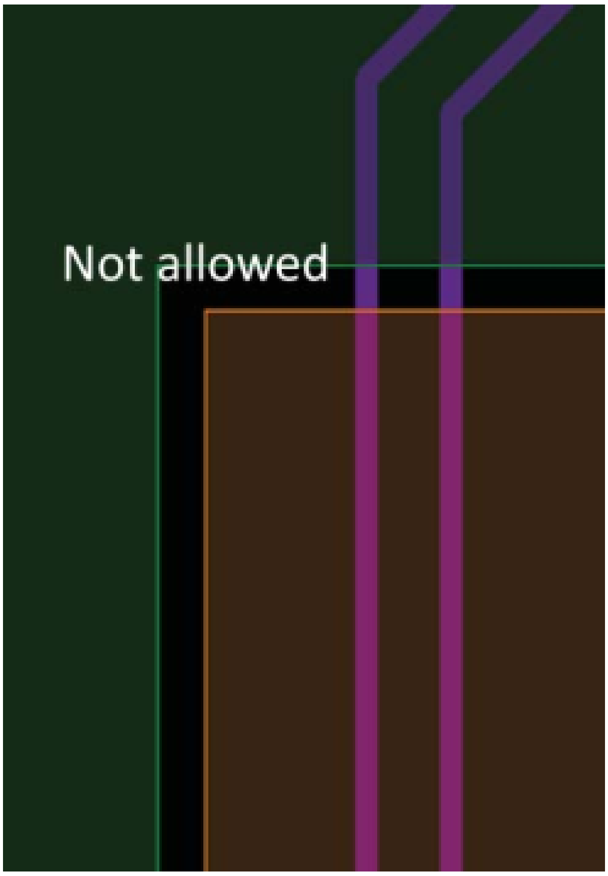
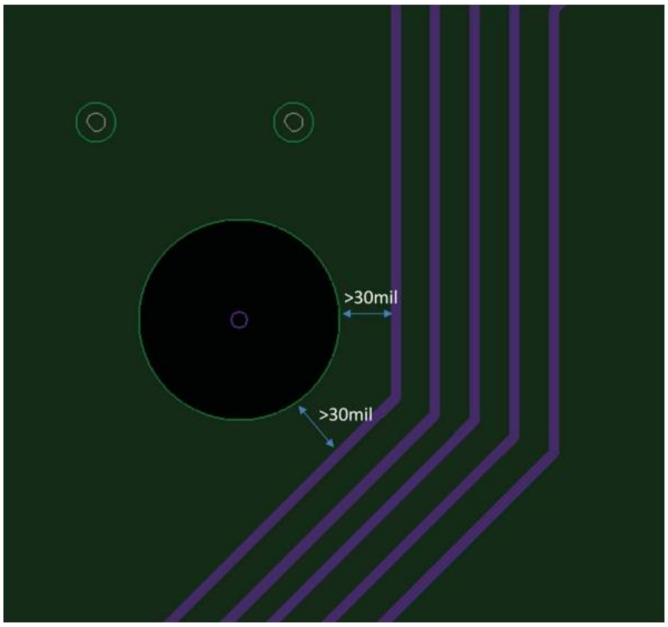
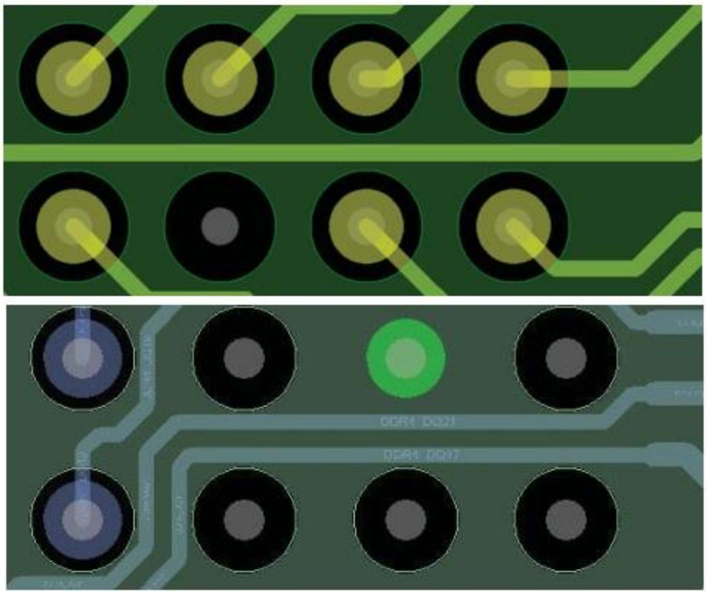


Figure 4-11 Margin between Trace and Hollowing out Area



In the fan-out area, the signal line should be in the middle of the two vias, and try to avoid the edge of the vias avoidance area of the reference layer, as shown in Figure 4-12.

Figure 4-12 Routing in the Pin Area



4.5.2 Reference Plane Suture

In some areas of the device, ground pins are rare, which can result in discontinuities in the reference plane. Coupled with the dense signals and small spacing, this can increase crosstalk and cause data errors.

As shown in Figure 4-13, the signal can be fanned out on both sides to leave a non-vias area in the middle, so that a ground plane suture can be made. As shown in Figure 4-14, in the crowded area, the ground vias should be appropriately added, and the vias should be placed as far as possible in the semi-arc area formed by the routing.

Figure 4-13 Ground Plane Suture

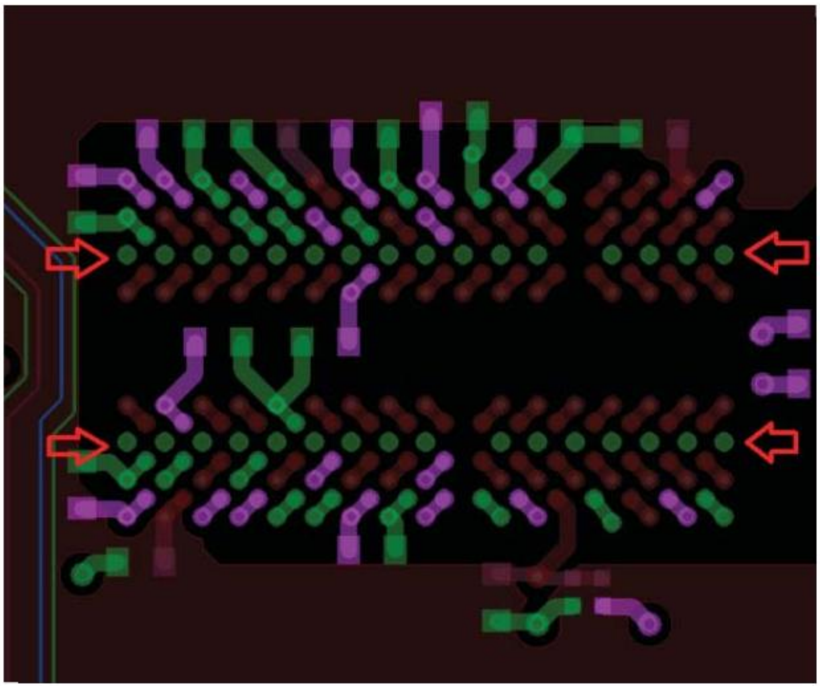
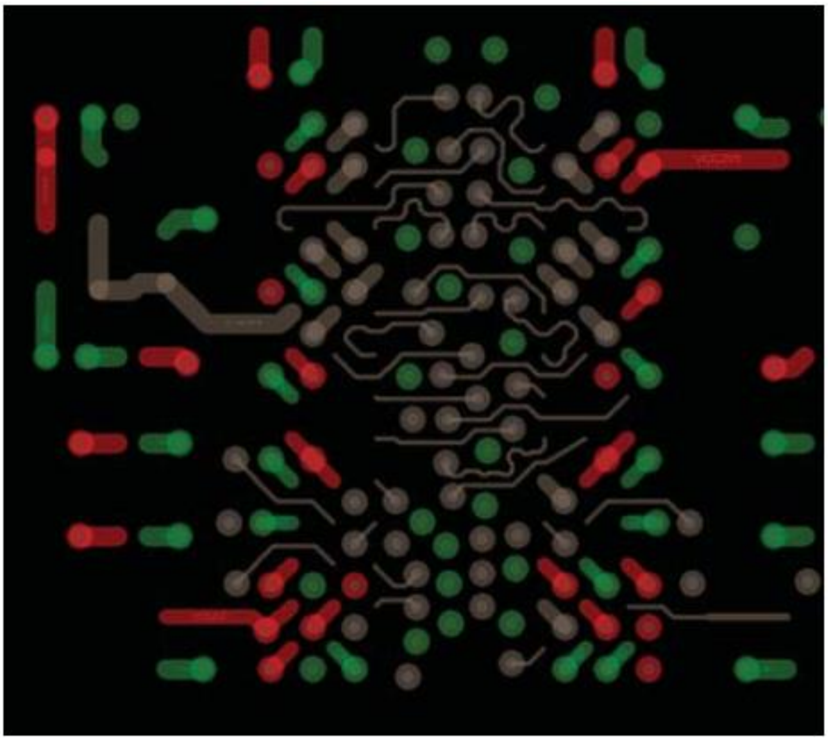


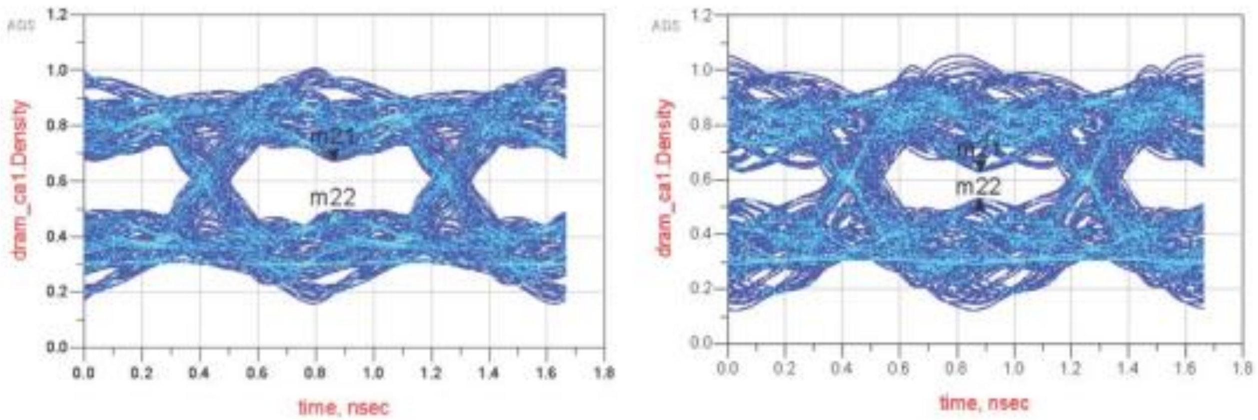
Figure 4-14 Add Ground Via to Crowded Area (Green for Ground, Red for Power Supply)



A simulated eye view of the command/address/control line is shown in

Figure 4-15, which makes a contrast between the two situations: with or without a suture vias in the ground plane. The left figure simulates the use of ground suture vias, and the eye diagram height is180 mV. While the right figure simulates the non-use of ground suture vias, and the eye diagram height is 99 mV.

Figure 4-15 Command, Address, Control Line Simulation and Contrast



4.5.3 Signal Return Path

The easiest thing to overlook in PCB design is the current return path. It is important for termination resistance signals (parallel termination resistance) because the current through the termination resistance is very large. Most board-level emulators only consider the reference plane boundary and gap, but not consider the effect of the return path. Being aware of this problem, visual measurement can achieve good results.

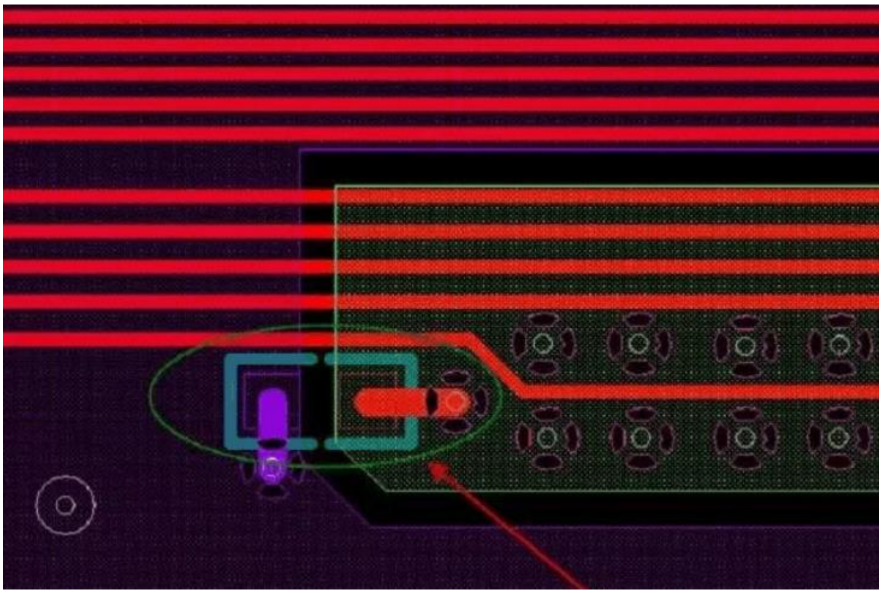
The shorter the signal return path, the smaller the current noise and the stronger the anti-interference ability. The optimal signal return path should be located directly in the adjacent layer of the signal routing, and the layer spacing should not be greater than 5mil. Otherwise the area of the signal loop will increase. For the 8-layer stackup structure in this design (section 4.1.1), the 2nd and 7th are the complete ground plane, and it is a good choice to put the signal at the 3rd and 6th layers.

The signal changes between layer 1 and layer 3, causing minimal interference to the return path. The signal changes between layer 1 and layer 6, causing great interference to the return path. Even though in both cases the reference plane is the ground plane, the return path is different. When the signal is changed between the 1st and 6th layers, the return current needs to find a path between the different reference planes This will increase the area of the loop. If this is required, a ground vias can be placed near the changed layer to minimize the loop area.

Add as many ground vias as possible to the inside and edges of the device to provide a good return path for signals and power, especially at the corners of the device, where the number of griund pins is usually small.

If there is a reference plane changing from the ground plane to the power plane, the return path needs to be connected with a capacitance for plane-to-plane change, i.e., the jumper capacitance, as shown in Figure 4-16. This usually results in larger increase of loop area, so try to avoid it.

Figure 4-16 Jumper Capacitance



4.6 Simulation

4.6.1 Simulation

Periodic simulation of I/O performance is recommended during the layout of a new design or modified design. The interface can be optimized by simulation to reduce noise and increase timing margin before prototype construction. When the problem is found in the simulation, the problem is often easier to solve. When the problem is found after PCB, it will face expensive and time-consuming circuit board redesign.

Manufacturers of memory devices have created many types of simulation models to match different tools. For Micron, the current component simulation models on the official website include IBIS, Verilog, VHDL, Hspice, Denali and Synopsys.

It is impractical to verify all possible conditions, but it needs to focus on some key points: the DC level, the signal transmission rate, undershoot, overshoot, ringing, and the waveform. In addition, it is important to verify whether the design has sufficient signal eye diagram openings to satisfy timing and resist power supply interference.

Snaking provides the required delay, but note that there is some kind of self-coupling that can alter the propagation delay of the signal. It is recommended to use simulation with coupling to verify timing.

Vias may cause timing errors. If every signal in the bus change layer through the same vias on the same layer, the influence of the vias can be ignored. If a mismatch occurs, the extra delay may bring the timing margin into negative. Vias should be considered in simulation, and if the entire bus is simulated, all vias should be considered. If the simulation does not include the entire bus, consideration should be given to compensating for additional vias delays. One formula for the extra delay is that the path length of the signal vias is twice the actual length of the vias.

4.6.2 Timing Budget Design

If there is an appropriate timing margin, it is recommended to design the hardware from the perspective of timing budget, so as to increase the flexibility of placement and routing. Starting from the simulation, the setup and hold time of the signal can be obtained by referring to the eye diagram of the memory device under ideal conditions. Then the parameters not included in the simulation are added to make the simulation result closer to the actual running environment.

The timing budget requires the system to work normally with all parameters considered. The higher the speed or the more complex the system, the more difficult to meet the timing budget. In some designs allowing deviations, it should first consider whether there is enough margin in the timing budget. The following table shows the parameters commonly included in the address bus timing budget.

Table 4-2 Address Timing Budget Example

Parameter	Setup	Hold
The value obtained from the ideal simulation	476	651
Setup and Hold requirements provided by DDR3 manual	45	120
The reduction calculated from the signal conversion rate	2.3	2.8
Offsets related to the VREFCA	13	11
DDR3 Derating	88	50
Crosstalk	47	42
Controller error	200	200
Clock error	30	30
Routing error	10	10
Margin	41	185

The margin is the ideal value minus all the other parameters. If it's a positive number, there's a margin. If there is a big difference between setup and hold margins, you need to offset the clock to get a more even result. The margin result in the above figure is acceptable.

4.7 Conclusion

Signal integrity, power supply, routing, and decoupling are major concerns when you are designing.

For different applications, before layout, the design analysis and simulation verification should be made to achieve better function and stability.

5 Notes

1. For using other manufacturers or other types of memory devices, first read the official design guide carefully.
2. Please refer to the official documentation for multiple memory devices design.

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