BK7231U Chip Datasheet

802.11n + BLE 4.2

For more technical information and development tools, please contact Mr. Zhong: 15361810961 QQ/VX: 371230015

Broadcom Integrated Circuits (Shanghai) Co., Ltd.
Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai,
China
Building 41, Science and Technology Leadership Capital, No. 1387 East Zhang Rd.
Tel: 86-21-51086811
www.bekencorp.com

catalogs

Revision history

releases	descriptive	dates	author
0.6	Official Chinese Version	October 29, 2018	WF
0.7	Add BLE RF features	December 13, 2018	QXU
0.71	Add QFN40	December 20, 2018	WF

1. summary

The BK7231U is an integrated Bluetooth low power BLE 4.2, Wi-Fi 802.11n, audio capture, image capture and hardware compression chip. The chip integrates the hardware and software resources needed for complete 802.11n and BLE applications, and can support dual role AP and STA connectivity, as well as BLE connectivity. The extremely fast 32-bit MCU and the built-in high-capacity
RAM enables the chip to support multi-cloud connectivity, and the MCU's extended instructions specifically for signal processing allow it to efficiently encode and decode audio.

Code.

The BK7231U has a rich set of peripherals such as PWM, I2S, I2C, UART, SPI,
SDIO, USB, and IrDA. up to six 32-bit PWM outputs make the chip ideal for high-quality LED control.

The BK7231U has a built-in microphone signal amplifier and a high-performance ADC to capture 16-bit voice signals at a 16 kHz sampling rate.

The BK7231U's I2S interface supports both master and slave modes, adopts rates from 8 kHz to 48 kHz typically, and can provide a master clock for an external CODEC.

The BK7231U has an 8-bit digital video interface that takes the raw signal directly from the CMOS image sensor and transmits the image compressed by the BK7231U's internal MJPEG encoder. The integrated QSPI interface allows simultaneous operation of external FLASH and RAM.

The BK7231U can be used with a standalone Bluetooth chip. The BK7231U provides a low-power clock and a main runtime clock for the Bluetooth chip, as well as a coexistence interface. The BK7231U can support external PA and LNA extensions by providing an indication of the current transceiver's transceiver status.

The BK7231U has a 32-byte eFUSE to provide a unique serial number, code encryption and to secure the debug interface. An internal true random number generator is integrated to ensure secure communication.

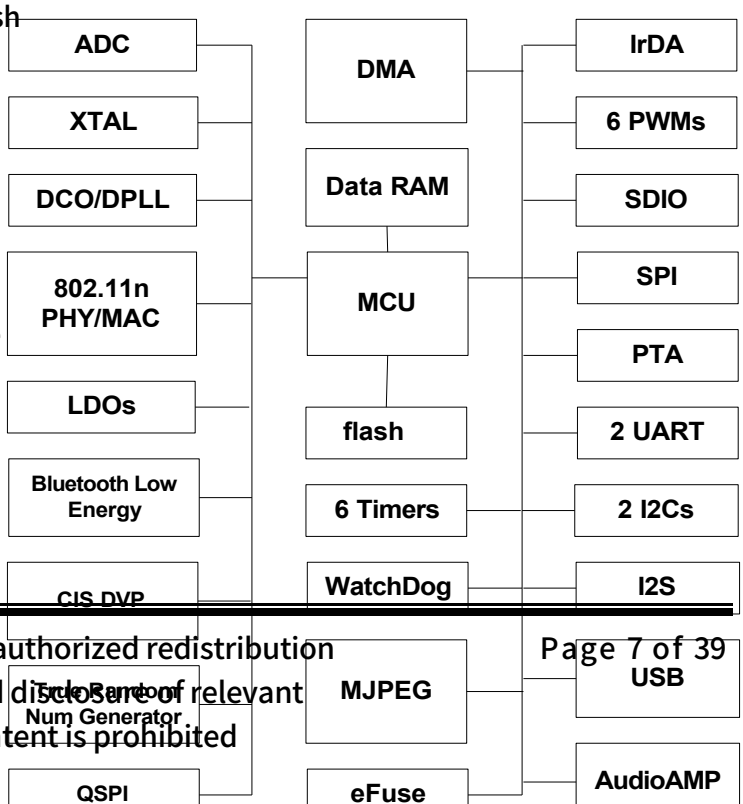
The BK7231U supports a low-power sleep mode, where the MCU can enter a sleep state and reach a sleep current of a few tens of microamps.

The deep sleep mode supported by the Bk7231U can run a 32-bit clock at a few milliamps of current and can be woken up by this clock or by any GPIO.

2. Technical characteristics

- 802.11 b/g/n 1x1 compliant
- 54 Mbps Output power 15 dBm
- 54 Mbps Sensitivity -74 dBm
- Wideband and narrowband interference detection and suppression
- 20/40 MHz bandwidth and STBC
- Supports STA, AP, and Direct modes
- Supports AP and STA dual role parallelism
- Bluetooth mode supports up to 20 dBm transmit power
- Complete Bluetooth coexistence interface

- High-speed 32-bit MCU
- Large internal RAM
- 2MB or 4MB internal Flash
- QSPI support for PSRAM and FLASH expansion
- PSRAM directly mapped to data memory space
- Download and debug in one interface
- Full-speed USB with support for master and device modes
- SDIO and SPI interfaces with at least 50 MHz clock frequency
- Dual I2C Interface
- UART interface with flow control
- Six 32-bit counters and one low-power counter
- Six-way support for high-speed clock or low-power



Time-consuming clock PWM output

- Microphone Signal Amplifier
- High-speed 10-bit multi-channel ADC with internal filtering to 16 bits
- 8-bit CMOS Image Sensor Interface
- MJPEG hardware encoding at VGA level
- 32-Byte eFUSE and True Random Number Generator
- 26 MHz and 32 KHz clock signal outputs

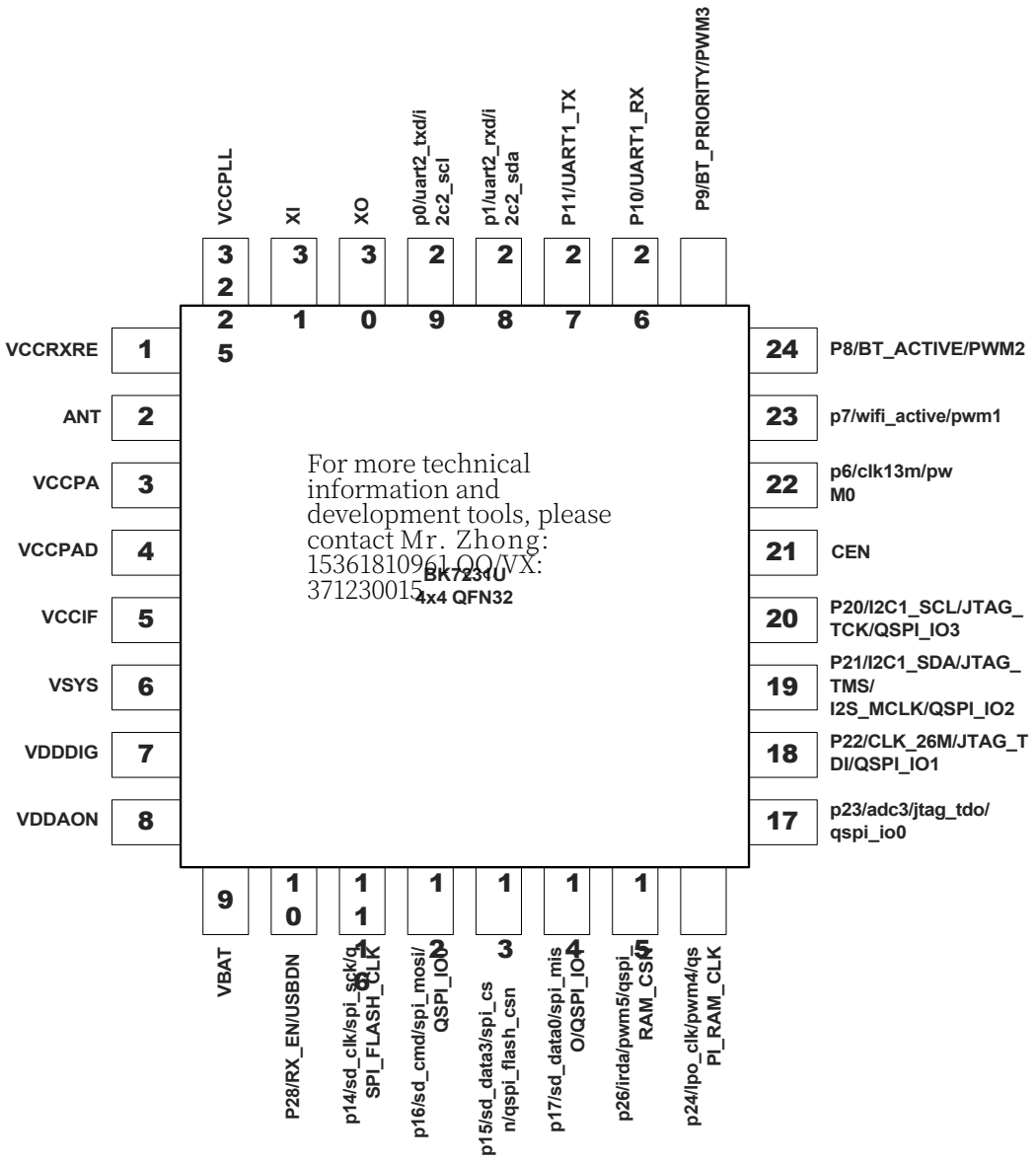
For more technical information and development tools, please contact Mr. Zhong: 15361810961 QQ/VX: 371230015

3. appliance

- Smart Home and Smart Family
- wireless stereo
- Wireless Image Transmission

4. pin

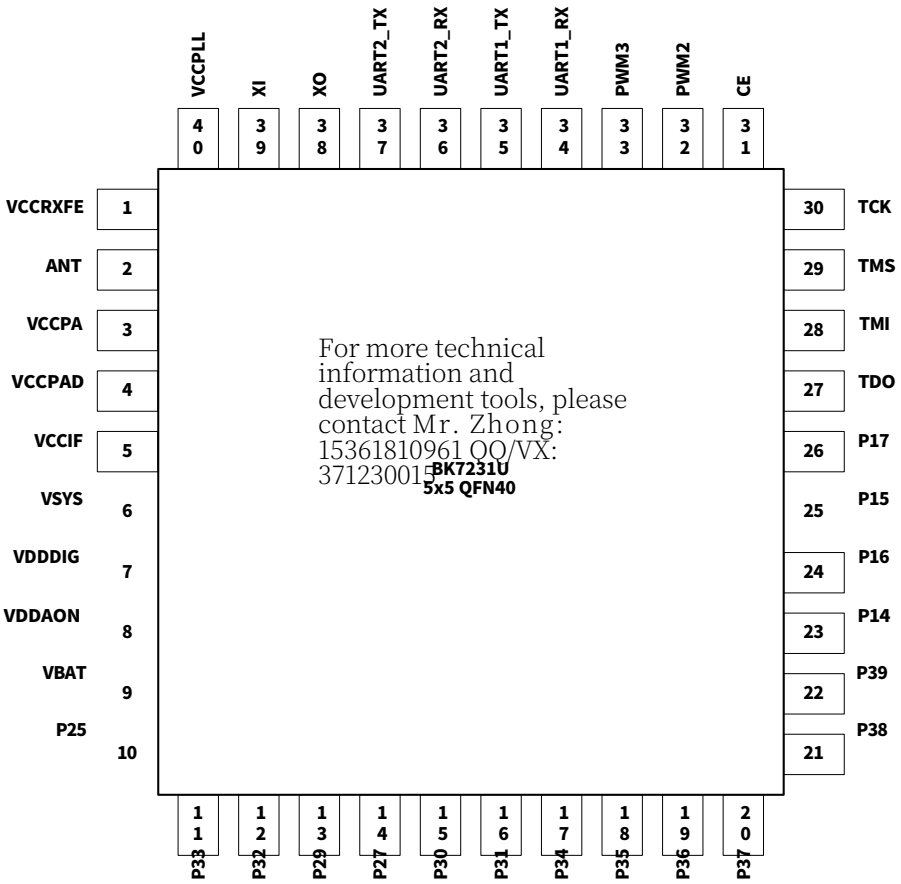
The BK7231U is available here in the QFN5x5 32-pin and QFN5x5 40Pin package formats designed for IoT data applications. Larger packages are required for audio and graphics applications.



32PIN	name (of a thing)	Pin Type	descriptive
1	VCCRXFE	I	RF Front End Power Supplies
2	ANT	IO	2.4 GHz signal antenna port
3	VCCPA	I	RF PA Power Supplies
4	VCCTX	I	RF Transmitter Power Supplies
5	VCCIF	I	Medium Frequency Power Supply
6	VSYS	o	System power supply
7	VDDDIG	O	digital power
8	VDDAON	O	Low Power Supply
9	VBAT	I	Chip Mains
10	P28/RX_EN/USBDN	IO	GPIO, Receive Status Indication, USB DN
11	p14/sd_clk/spi_sck/qspi_flASH_CLK	IO	GPIO, SD Card clock, SPI clock, QSPI FLASH Clock
12	p16/sd_d0/spi_mosi/qspi_iO0	IO	GPIO, SD Card DATA0, SPI MOSI, QSPI IO0
13	p15/sd_cmd/spi_csn/qspi_FLASH_CSN	IO	GPIO, SD_CMD, SPI CSN, QSPI FLASH CSN
14	p17/sd_d1/spi_miso/qspi_iO1	IO	GPIO, SD Card DATA1, SPI MISO, QSPI IO1
15	p26/irda/pwm5/qspi_ram_CSN	IO	GPIO, IrDA input, PWM 5, QSPI RAM CSN
16	p24/ lpo_clk/pwm4/qspi_ram_CLK	IO	GPIO, Low Power Clock Out, PWM 4, QSPI RAM Clock
17	p23/adc3/tdo/qpio_io0	IO	GPIO, ADC, JTAG TDO, QSPI IO0 In download mode it is FLASH download data transmission. exportation
18	p22/xhout/tdi/qspi_io1	IO	GPIO, Crystal Clock Out, JTAG TDI, QSPI IO1 In download mode it is FLASH download data transmission. entrances

19	p21/i2c1_sda/tms/qspi_io2	IO	GPIO, I2C1 SDA, JTAG TMS, QSPI IO2 In download mode it is the FLASH download command that makes the

			suitably qualified candidate (old)
20	P20/I2C1_SCL/TCK/QSPI_IO3	IO	GPIO, I2C1 SCL, JTAG TCK or QSPI IO3 In download mode is the FLASH download clock port
21	CEN	I	Chip Enable, High Active
22	P6/CLK13M/PWM0	IO	GPIO, 13 MHz clock output, PWM 0
23	P7/WIFI_ACTIVE/PWM1	IO	GPIO, Wi-Fi activity indication output, PWM 1
24	P8/BT_ACTIVE/PWM2	IO	GPIO, Bluetooth activity indication input, PWM 2
25	P9/BT_PRIORITY/PWM3	IO	GPIO, Bluetooth priority indication inputs, PWM 3
26	P10/UART1_RXD	IO	GPIO, UART1 RXD
27	P11/UART1_TXD	IO	GPIO, UART1 TXD
28	P1/UART2_RXD/I2C2_SDA	IO	GPIO, UART2 RXD, I2C2 SDA
29	P0/UART2_TXD/I2C2_SCL	IO	GPIO, UART2 TXD, I2C2 SCL
30	XO	o	26/40 MHz crystal outputs
31	XI	I	26/40 MHz crystal inputs
32	VCCPLL	I	PLL Power Supplies



40PIN	name (of a thing)	Pin Type	descriptive
1	VCCRXFE	I	RF Front End Power Supplies
2	ANT	IO	2.4 GHz signal antenna port
3	VCCPA	I	RF PA Power Supplies
4	VCCTX	I	RF Transmitter Power Supplies
5	VCCIF	I	Medium Frequency Power Supply
6	VSYS	O	System power supply
7	VDDDIG	O	digital power
8	VDDAON	O	Low Power Supply
9	VBAT	I	Chip Mains
10	P25	IO	GPIO, TX Indication, USB DP
11	P33	IO	GPIO, PXD1, SPI_MISO
12	P32	IO	GPIO, PXD0, SPI_MOSI
13	P29	IO	GPIO, PCLK
14	P27	IO	GPIO, CIS_MCLK
15	P30	IO	GPIO, HSYNC, SPI_SCK

16	P31	IO	GPIO, VSYNC, SPI_CSN
17	P34	IO	GPIO, PXD2, SD_CLK
18	P35	IO	GPIO, PXD3, SD_CMD
19	P36	IO	GPIO, PXD4, SD_DATA0
20	P37	IO	GPIO, PXD5, SD_DATA1
21	P38	IO	GPIO, PXD6, SD_DATA2
22	P39	IO	GPIO, PXD7, SD_DATA3
23	p14/sd_clk/spi_sck/qspi_flASH_CLK	IO	GPIO, SD Card clock, SPI clock, QSPI FLASH Clock
24	p16/sd_d0/spi_mosi/qspi_iO0	IO	GPIO, SD Card DATA0, SPI MOSI, QSPI IO0
25	p15/sd_cmd/spi_csn/qspi_FLASH_CSN	IO	GPIO, SD_CMD, SPI CSN, QSPI FLASH CSN
26	p17/sd_d1/spi_miso/qspi_iO1	IO	GPIO, SD Card DATA1, SPI MISO, QSPI IO1
27	p23/adc3/tdo/qpio_io0	IO	GPIO, ADC, JTAG TDO, QSPI IO0 In download mode it is FLASH download data transmission. exportation
28	p22/xhout/tdi/qspi_io1	IO	GPIO, Crystal Clock Out, JTAG TDI, QSPI IO1 In download mode it is FLASH download data transmission. entrances
29	p21/i2c1_sda/tms/qspi_io2	IO	GPIO, I2C1 SDA, JTAG TMS, QSPI IO2 In download mode it is the FLASH download command that makes the suitably qualified candidate (old)
30	P20/I2C1_SCL/TCK/QSPI_IO3	IO	GPIO, I2C1 SCL, JTAG TCK or QSPI IO3 In download mode is the FLASH download clock port
31	CEN	I	Chip Enable, High Active
32	P8/BT_ACTIVE/PWM2	IO	GPIO, Bluetooth activity indication input, PWM

			2
33	P9/BT_PRIORITY/PWM3	IO	GPIO, Bluetooth priority indication inputs, PWM 3
34	P10/UART1_RXD	IO	GPIO, UART1 RXD
35	P11/UART1_TXD	IO	GPIO, UART1 TXD
36	P1/UART2_RXD/I2C2_SDA	IO	GPIO, UART2 RXD, I2C2 SDA
37	P0/UART2_TXD/I2C2_SCL	IO	GPIO, UART2 TXD, I2C2 SCL
38	XO	O	26/40 MHz crystal outputs
39	XI	I	26/40 MHz crystal inputs
40	VCCPLL	I	PLL Power Supplies

5. Wi-Fi and Bluetooth

The BK7231U supports the full range of 802.11b/g/n features, including HT20 and HT40, and the system can be connected to external LNAs and PAs for longer ranges through the transmit-activated indication of GPIO25 and receive-activated indication of GPIO28.

The BK7231U integrates a Bluetooth low-power BLE 4.2 system with shared antenna and transceiver circuits for Bluetooth and Wi-Fi. Precise internal time division multiplexing logic ensures the stability of dual Bluetooth and Wi-Fi connections and efficient sharing of air resources.

6. clocks

The system contains seven primary clock sources as follows.

- X26M: High-frequency crystal oscillator, typically 26 MHz. also serves as a reference clock for DPLL and I2S PLLs. the X26M contains adjustable 6~18 pF capacitors (6~18 pF each for the input and output ports), with a total of 64 steps of adjustment. the X26M is a high-frequency crystal oscillator, typically 26 MHz. The oscillator startup time is about a few milliseconds.
- DCO: Internal high-frequency digitally controlled oscillator, frequency 26 to 120 MHz. calibrated to a frequency error of about +/-2%. The start-up time of the DCO is about a few microseconds

- X32K: Low frequency crystal oscillator with external 32.768 kHz crystal
- D32K: 32 kHz clock divided from 26 MHz
- ROSC: internal low-frequency oscillator with a frequency error of around +/-2%
- DPLL: High-speed 480 MHz PLL
- I2SPLL: PLL designed for audio applications, e.g. I2SPLL can generate 1024*FS clocks for audio signals with sample rate FS of 44.1 kHz or 48 kHz.

The low power clock (LPO_CLK) comes from the X32K, D32K or ROSC.

The clock source for the MCU and other peripherals can be selected as follows.

	X26M	DCO	DPLL	LPO_CLK	I2SPLL
MCU	√	√	√	√	
ADC	√	√			√
SDIO	√	√			
PWM	√	√		√	
SPI	√	√			
I2C2	√	√			
IrDA	√	√			
I2C1	√	√			
UART2	√	√			
UART1	√	√			
QSPI	√	√	√		
Timer 1	√				
Timer 2				√	
I2S					√
CIS/MJPEG			√		
Watch Dog				√	
Always on timer				√	

The chip can also output clocks for other external devices as follows.

- LPO_CLK and X26M clocks can be output to GPIOs.
- The 13 MHz clock from the X26M frequency divider can be output and is typically used to provide a master clock to an external FM receiver.
- I2S MCLK: Divide the I2SDPLL output by 1, 2, 4, or 8, and use the output as the MCLK of the external CODEC.
- PCLK: typically 24, 48, or 96 MHz, used to provide the master clock for external CMOS image sensors

7. reset (a dislocated joint, an electronic device etc)

Circuits other than the low-power normally open AON logic, system power-up, digital

power-on, and watchdog reset have the same reset effect, resetting the entire chip to its initial state. the AON logic has 32-bit counters and 16-bit holding registers, which are only reset to their initial state by a system power-up, and the effects of the other reset signals do not change their content.

The entire system reboot process is triggered when the system wakes up from Shut down mode or Deep sleep mode.

8. Low Power Management

To minimize power consumption, the BK7231U can enter the following low-power modes.

Shutdown - When CEN=0 the system enters shutdown mode. When CEN=1 for a few milliseconds, the system powers up and enters operating mode.

Deep sleep mode - In this mode, the main MCU system is powered down, only the GPIO status is maintained and the AON section remains active. a GPIO edge change or an AON counter interrupt can wake up the system to an active state. the AON's Holding Register maintains its contents.

Normal Standby - In this mode, the MCU stops running and the peripherals can continue to work and generate interrupts to wake up the MCU to continue running.

Low Voltage Standby - To further minimize leakage, the system can enter a low voltage standby mode. Throughout this mode, the MCU and all digital peripheral clocks are stopped, and only GPIO interrupts and AON counter interrupts are available to wake up the system to normal voltage and continue operation.

9. peripherals

9.1. UART

The BK7231U has two sets of UARTs with a maximum baud rate of 6 Mbps.The UARTs support 5, 6, 7 and 8 bit data widths. The UART supports 5, 6, 7, and 8 bits data width. It supports even, odd, or 0 checksum. The stop bit can be 1 or 2 bits.

UART1 contains RTS and CTS signals that support flow control.

In the low voltage standby state, continuously applying a low level to the TXD or RXD data line can wake up the MCU and UART to return to normal voltage and operation.

9.2. SPI

The BK7231U's SPI supports both master and slave modes. In slave mode, the rate can generally go up to at least 50 MHz, at which time there is a dedicated DMA channel to process data from the SPI interface.

The BK7231U's SPI can support 8 MHz in either master or slave mode, and the clock edge used for receiving data can be any edge of the clock. The transmit data start bit can be MSB or LSB.

9.3. SDIO

The BK7231U SDIO can be used as master and slave, with a bit width of 1 to 4 bits and a maximum clock frequency of 50 MHz.The SDIO is generally used as a master for reading SD card or as a slave for external host control chip.

SDIO has a dedicated DMA channel for high-speed data exchange.

9.4. I2C

The BK7231U supports two sets of I2Cs, with general speed support up to 400 kHz and 7-bit addressing. The I2C will generate an interrupt to inform the MCU when a low level on SCL or bus idle time exceeds the set threshold.

9.5. USB

The BK7231U supports full-speed USB 2.0 in both master and

device modes, with modes configured by software. USB has a

dedicated DMA channel for carrying data.

9.6. ADC

The BK7231U has multiple ADC channels, with internal averaging and downsampling filters, the ADC supports 10~16 bit outputs. The outputs can be single, continuous or software read update mode.

The ADC's signal source, in addition to the GPIO, can also directly measure the voltages

of the VSYS pin, the internal temperature sensor, and the internal calibration circuitry.

9.7. PWM

The BK7231U has six 32-bit PWM outputs, and the PWM operation clock can be either a high-speed clock or a low-power clock. Each PWM can have its own independent duty cycle and frequency.

The PWM supports capture mode, which uses the internal high-frequency clock to calculate the signal pulse width, i.e., the number of high-frequency clock cycles between signal edges.

9.8. Timer Counter

The BK7231U has two groups of counters, each with three 32-bit counters. The first group runs on X26M and has a 4-bit prescaler. The second group runs on a low-power clock and has a separate 4-bit prescaler.

The watchdog clock is used to reset the system to avoid the system running in disorder. When the MCU stops running or power is lost, the watchdog will also stop running.

Counter in the AON power domain for low-power timing that continues to run even if the MCU loses power.

9.9. GPIO

The BK7231U has a total of 40 GPIOs, any of which can be configured as an interrupt source to wake up the system from low-power mode.

GPIOs are generally mapped for other functions, as shown in the table below.

GPIO	function mapping
GPIO0	UART2_TXD/I2C2_SCL
GPIO1	UART2_RXD/I2C2_SDA
GPIO2	I2S_CLK/ADC5
GPIO3	I2S_SYNC/ADC4
GPIO4	I2S_DIN/ADC1

GPIO5	I2S_DOUT/ADC2
GPIO6	CLK13M/PWM0
GPIO7	WIFI_ACTIVE/PWM1
GPIO8	BT_ACTIVE/PWM2
GPIO9	BT_PRIORITY/PWM3
GPIO10	UART1_RX
GPIO11	UART1_TX
GPIO12	UART1_CTS/ADC6/PGA_INP
GPIO13	UART1_RTS/ADC7/PGA_INN
GPIO14	sd_clk/spi_sck/qspi_flash_clk
GPIO15	sd_cmd/spi_csn/qspi_flash_csn
GPIO16	SD_DATA0/SPI_MOSI/QSPI_IO0
GPIO17	SD_DATA1/SPI_MISO/QSPI_IO1
GPIO18	SD_DATA2/QSPI_IO2
GPIO19	SD_DATA3/QSPI_IO3
GPIO20	I2C1_SCL/JTAG_TCK/QSPI_IO3
GPIO21	I2C1_SDAJTAG_TMS/ I2S_MCLK/QSPIO_IO2
GPIO22	CLK_26M/JTAG_TDI/QSPI_IO1
GPIO23	ADC3/JTAG_TDO/ QSPI_IO0
GPIO24	lpo_clk/pwm4/qspi_ram_clk
GPIO25	TXEN/USBDP/
GPIO26	IRDA/PWM5/QSPI_RAM_CSN
GPIO27	CIS_MCLK
GPIO28	RX_EN/USBDN/
GPIO29	PCLK
GPIO30	HSYNC/SPI_SCK
GPIO31	VSYNC/SPI_CSN
GPIO32	PXD0/SPI_MOSI
GPIO33	PXD1/SPI_MISO
GPIO34	PXD2/SD_CLK
GPIO35	PXD3/SD_CMD
GPIO36	PXD4/SD_DATA0
GPIO37	PXD5/SD_DATA1
GPIO38	PXD6/SD_DATA2
GPIO39	PXD7/SD_DATA3

Figure 1 GPIO Function Mapping

9.10. FLASH Download

Within a few hundred milliseconds after the digital logic is reset to the working state, GPIO20~GPIO23 will be used as mode selection pins, at this time, if the instruction is received to enter the FLASH download mode, the chip and these four pins will enter the FLASH download mode, and the external download device can download the program into the FLASH through these four pins.

9.11. CMOS image sensor interface and MJPEG encoding

The CMOS image sensor interface provides an 8-bit parallel data interface (GPIO32~GPIO39) to the VGA sensor. Also provided to the sensor are the master clock (GPIO27), pixel clock (GPIO29), HSYNC (GPIO30), and VSYNC.
(GPIO31) signals. Supported sensors include, but are not limited to: OV7676, OV7670, GC0308, GC0309, GC0329, and PAS6329.

The interface and MJPEG operate on a 96 MHz clock divided by a DPLL, and the main clock to the sensor is also an integer division of the 96 MHz main clock. The YUV output from the sensor is sent directly to MJPEG for encoding, and the result is written to internal memory using a dedicated DMA.

The YUV signal format can be: YUYV, UYVY, YYUV and UVYY. the clock edges of HSYNC and VSYNC can be configured independently.

9.12. IrDA Infrared

The chip supports hardware IR decoding in NEC format. The interface also supports capture mode, which is suitable for software decoding of IR signals in any format.

9.13. I2S

The I2S interface supports master-slave mode, and the sample rate can be configured from 7.35 kHz to 96 kHz. together with an external CODEC, the I2S can output the master clock MCLK from GPIO21.

9.14. microphone amplifier

GPIO12 and GPIO13 can be used as differential microphone signal inputs, which are

amplified by the internal audio amplifier and can then be converted by the ADC to a 16-bit PCM signal with a 16 kHz sampling rate.

9.15. QSPI

QSPI is used to extend the FLASH and data RAM. the data port is shared by FLASH and RAM, but FLASH and RAM can have their own independent clock and chip select signals. qspi can operate up to 120 MHz, and the FLASH clock and RAM clock can be set to different values.

9.16. surety

The true random number generator and eFUSE are responsible for the security of the system.

A total of 32 bytes of eFUSE can be burned by the download ports GPIO20~GPIO23 or written by the internal MCU in download mode.

Bytes 31	Bytes 30:16	Bytes 15:0
containment	user-defined	code encryption

The byte (byte)31 is defined as follows:

bit 7: 1: disable JTAG; 0: use JTAG

bit 6: 1: disable FLASH download; 0: enable FLASH download

bit 5: 1: byte15:0 do code encryption; 0: no code encryption function,

byte15:0 to user bit 4: read disable for byte15:0 (1)

bit 3: write disable for byte15:0

(1) bit 2: write disable for

byte16:23 (1) bit 1: write disable

for byte24:29 (1)

bit 0: eFUSE Write disable for all 32 bytes (1)

The above read disable operation is only valid when byte15:0 is used for code encryption; otherwise byte15:0 is always readable. The above write disable operation is suitable for burner port and MCU.

9.17. temperature sensor

The on-chip temperature sensor can measure internal temperatures from -40 to 125 degrees with an accuracy of +/-3 degrees. The measurement results can be read by the

ADC sampling software.

Often the software will initiate calibration of specific modules based on the temperature value, narrowing down the difference in performance of the chip at different temperatures. The host can also read the on-chip temperature and decide whether to reduce the transmit power or suspend operation at high temperatures.

10. Electrical Characteristics

10.1. Limit parameters

sports event	Pin Name	minimal	greatest	unit (of measure)
Battery and mains powered IO	vccrxfe, vccpa, vcctx, vccif. VSYS, VBAT, CEN, VCCPLL	-0.3	3.9	V
Kernel Power Supply	VDDDIG, VDDAON			
Digital Input Pins		-0.3	3.9	V
analog pin	XI, XO	-0.3	1.5	
RF pins	ANT	-0.3	1.5	V
Storage temperature		-55	125	℃

10.2. ESD Indicator

sports event	descriptive	(be) worth	unit (of measure)
ESD_HBM	Electrostatic Discharge Tolerance - Human Body Models	+/-2000	V
ESD_MM	Electrostatic Discharge Tolerance - Machine Model	+/-200	V
ESD_CDM	Electrostatic Discharge Tolerance - CDM Modeling	+/-250	V

10.3. Recommended working conditions

parameters	prerequisite	minimal	typical case	greatest	unit (of measure)
operating voltage	VBAT-pin	3.0	3.3	3.6	V
Operating temperature (ambient)		-20		85	℃

10.4. power wastage

parameters	prerequisite	minimal	typical case	greatest	unit (of measure)
electric current (e.g. electrostatic)	17 dBm, 802.11b 11 Mbps		220		mA
electric current (e.g. electrostatic)	14 dBm, 802.11g 54 Mbps		200		mA
Receiving Current	-10 dBm input, 802.11g 54 Mbps		104		mA
Receiving Current	-10 dBm input, 802.11n HT40 MCS7		124		mA
Normal Standby Current	MCU stops running, Modem powers down		68		uA
Low Voltage Standby Current	MCU stops and goes low voltage		24		uA
Deep Sleep Current	All main logic is powered down, only the AON counter works		7		uA
Shutdown Current	CEN=0		1		uA
Note: All measurements were obtained at room temperature and 3.3V.					

10.5. Wi-Fi Receiving Characteristics

parameters	prerequisite	minimal	typical case	greatest	unit (of measure)
operating frequency		2412		2484	MHz
(level of) sensitivity	HT40 MCS7		-69		dBm
	HT20 MCS7		-71		dBm
	54 Mbps OFDM		-74		dBm
	6 Mbps OFDM		-92		dBm
	11 Mbps DSSS		-90		dBm
	2 Mbps DSSS		-92		dBm
Neighbor Channel Rejection Ratio	HT40 MCS7		20		dB
	HT20 MCS7		25		dB
	54 Mbps OFDM		26		dB

	11 Mbps DSSS		40		dB

10.6. Wi-Fi Launch Characteristics

parameters	prerequisite	minimal	typical case	greatest	unit (of measure)
operating frequency		2412		2484	MHz
Transmit power (EVM compliant) (quasi-requirements)	HT40 MCS7		13		dBm
	HT20 MCS7		14		dBm
	54 Mbps OFDM		15		dBm
	11 Mbps DSSS		17		dBm

10.7. BLE Receiving Characteristics

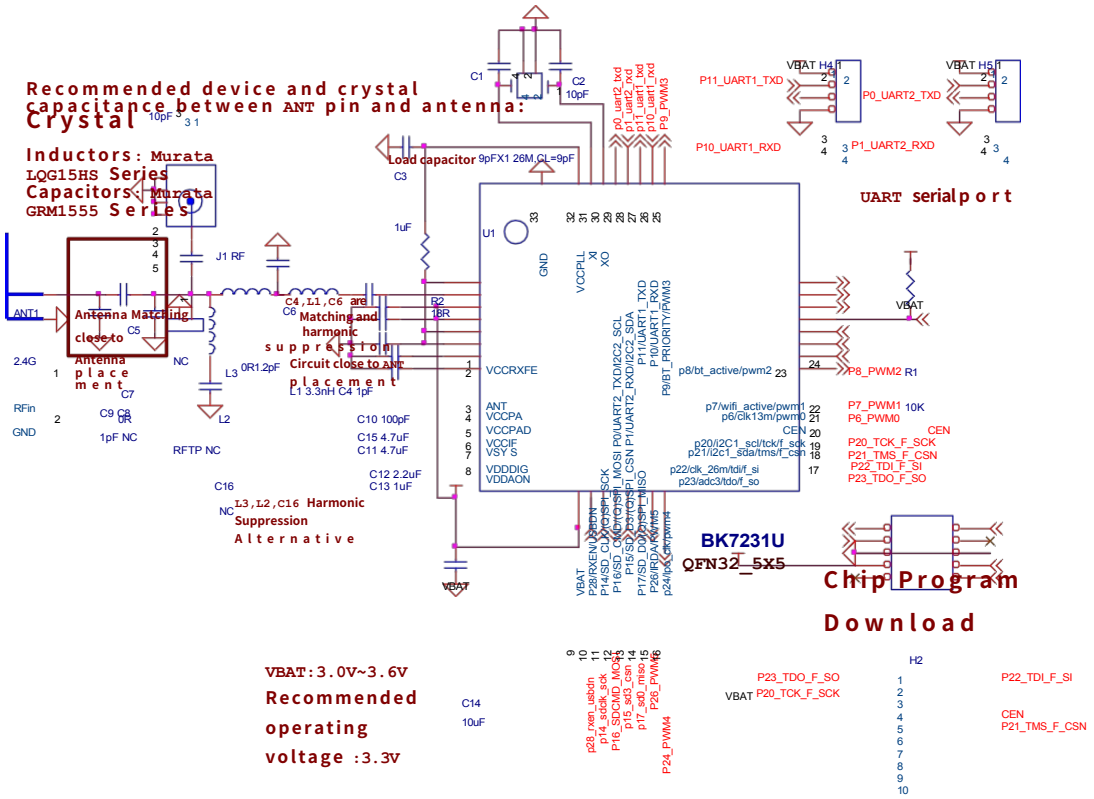
parameters	prerequisite	minimal	typical case	greatest	unit (of measure)
operating frequency		2402		2480	MHz
airspeed			1		Mbps
(level of) sensitivity			-85		dBm
Maximum RF signal input		-10			dBm
intermodulation				-23	dBm
Common channel rejection ratio C/I			10		dB
Neighbor channel rejection ratio C/I	+1MHz		0		dB
	-1MHz		0		dB
	+2MHz		-20		dB
	-2MHz		-27		dB
	+3MHz		-25		dB
	-3MHz		-36		dB
Out-of-band Blocking	30 MHz ~2000 MHz	-10			dB
	2000 MHz ~2400 MHz	-20			dB
	2500 MHz ~3000 MHz	-10			dB
	3000 MHz ~12.5 GHz	-10			dB

10.8. BLE Launch Characteristics

parameters	prerequisite	minimal	typical case	greatest	unit (of measure)
operating frequency		2402		2480	MHz
airspeed			1		Mbps
firing power		-20	5	20	dBm
20dB bandwidth BW			1		MHz
Freq Offset		-150		150	KHz
Max Drift		-50		50	KHz
Drift Rate			80	400	Hz/us
△f1avg		225	244	275	KHz
△f2max		185	195		KHz

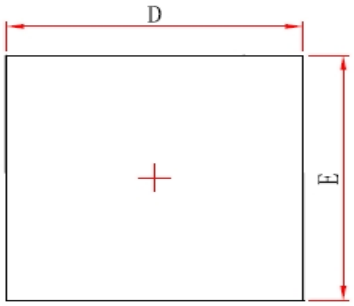
△f1avg/△f2avg		0.8	0.85		
Neighbor channel transmit power	2MHz Offset		-45	-20	dBm
	>=3MHz Offset		-47	-30	dBm

11. Application Schematic

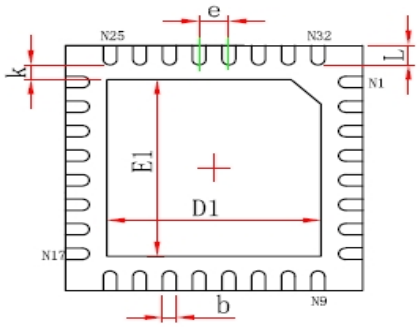


12. Package Size

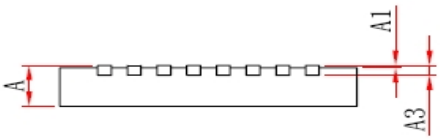
12.1. QFN32



Top View



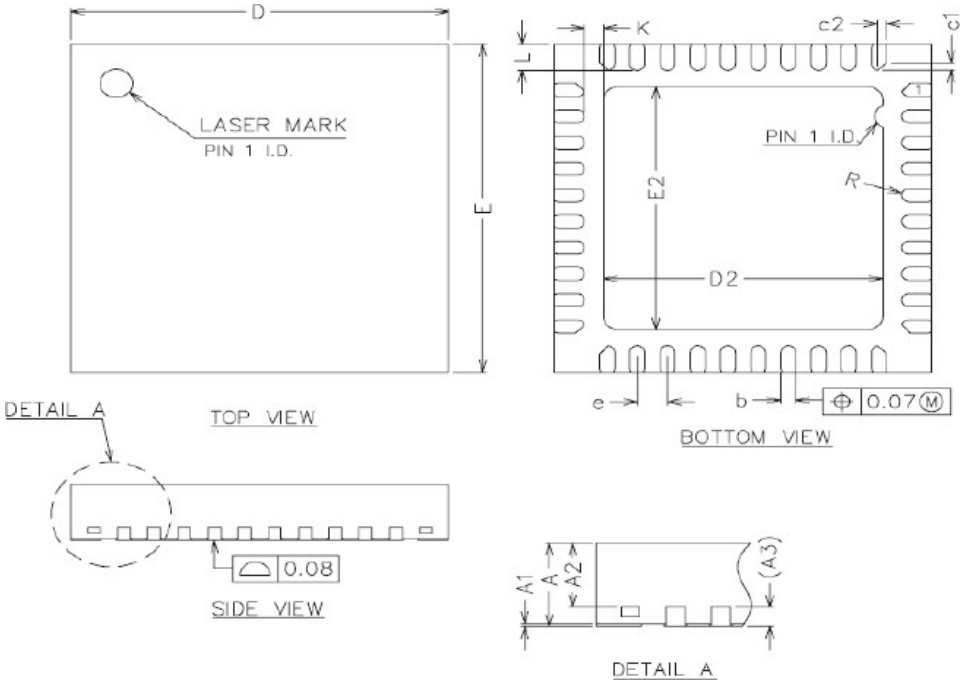
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

12.2. QFN40



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.50	0.65	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.075	–	–
C1	–	0.12	–
C2	–	0.12	–

13. Order Information

material number	seal inside	wrap	Minimum Order
BK7231UQN32	QFN32_5X5	Tape Reel	3K
BK7231UQN40	QFN40_5X5	Tape Reel	3K