Task 1 Synthesis and Implementation Run

Project Summary

Overview | Dashboard

Settings Edit

Project name:	xtea
Project location:	/home/homeunix/u138175/ece545/xtea/xilinx
Product family:	Artix-7
Project part:	xc7a12tcsg325-3
Top module name:	xtea
Target language:	VHDL
Simulator language:	Mixed

Synthesis

Status:	✓ Complete
Messages:	No errors or warnings
Part:	xc7a12tcsg325-3
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	None

Implementation **Summary** | Route Status

Status:	✓ Complete
Messages:	No errors or warnings
Part:	xc7a12tcsg325-3
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: 2 critical warnings
1 warning
Implemented DRC Report

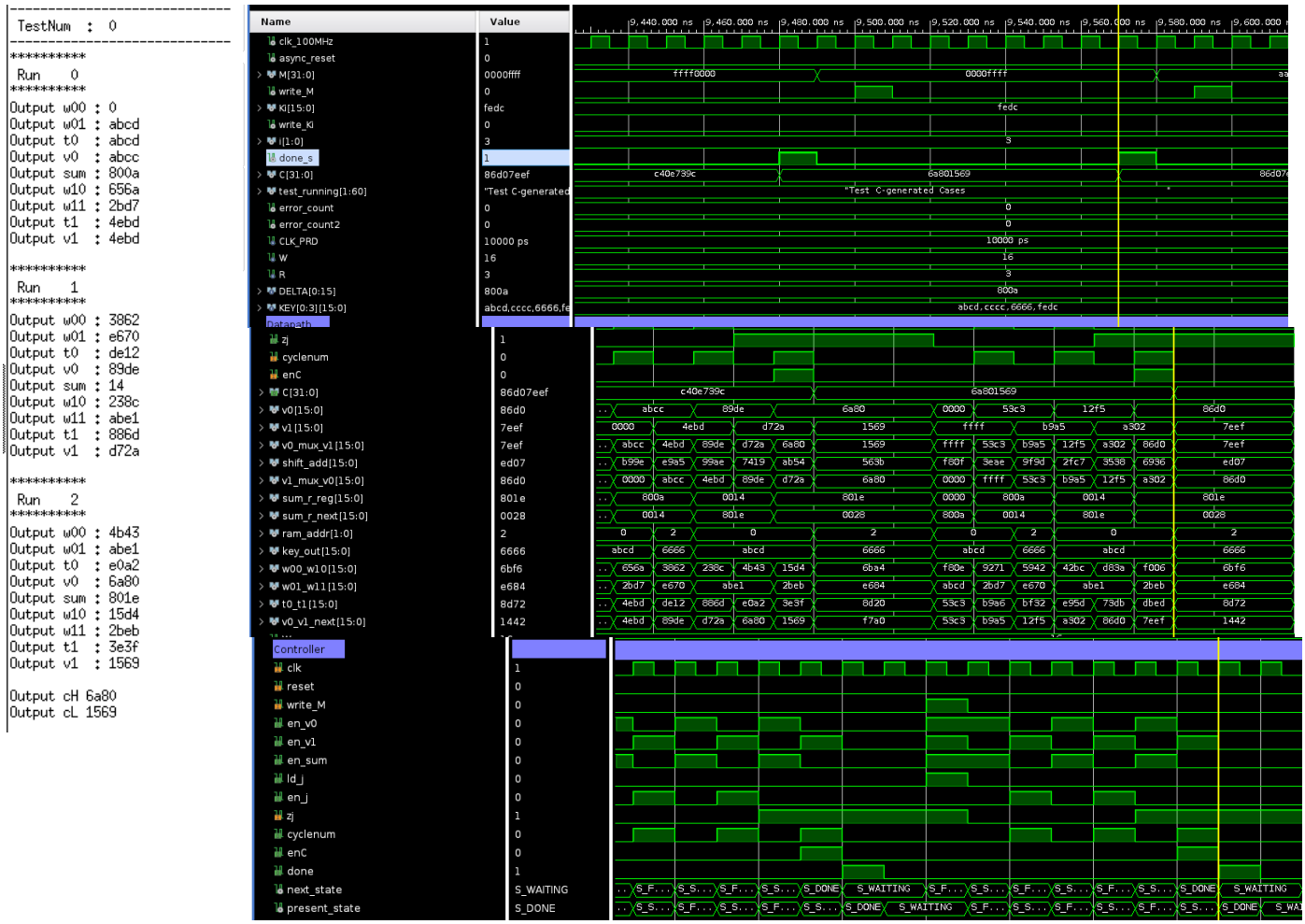
Timing **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	1.04 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	303

Implemented Timing Report

Name	Severity	Details
Pin Planning (3)		
NSTD-1 (1)		
NSTD #1	Critical Warning	87 out of 87 logical ports use I/O standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all I/O standards. This design will fail to generate a bitstream unless all logical ports have a user specified I/O standard value defined. To allow bitstream creation with unspecified I/O standard values (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks NSTD-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hc for write_bitstream step for the implementation run. Problem ports: CI[31:0], KI[15:0], MI[31:0], I[1:0], clk, done, reset, write_KI, write_M.
UCIO-1 (1)		
UCIO #1	Critical Warning	87 out of 87 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all pin locations. This design will fail to generate a bitstream unless all logical ports have a user specified site LOC constraint defined. To allow bitstream creation with unspecified pin locations (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks UCIO-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: CI[31:0], KI[15:0], MI[31:0], I[1:0], clk, done, reset, write_KI, write_M.

Task 2 Wave window



Task 3

3.

a. Synthesis Table

Run	LUTs	FFs	BRAMs	DSPs	Target Clock Period [ns]	Target Clock Frequency [MHz]	WNS (Worst Negative Slack [ns]	TNS (Total Negative Slack [ns]
1	144	86	0	0	10	100	4.703	0.000
2	144	86	0	0	5	200	-0.297	-10.220
3	144	86	0	0	6.667	150	1.370	0.000
4	144	86	0	0	8	125	2.703	0.000

b. Utilization Table

Run	LUTs	FFs	BRAMs	DSPs	Target Clock Period [ns]	Target Clock Frequency [MHz]	WNS (Worst Negative Slack [ns]	TNS (Total Negative Slack0 [ns]
1	135	86	0	0	10	100	1.040	0.000
2	135	86	0	0	5	200	-2.406	-159.181
3	135	86	0	0	6.667	150	-0.968	-36.476
4	135	85	0	0	8	125	-0.534	26

- Maximum clock frequency : 100MHz