CSCE-312 | Skill Assessment 1

Combinational Logic and Computer Arithmetic

Rules

You have **1 hour** to complete this assessment from your start time. Your final grade will be based on private test cases that are chosen to be like the ones provided to you. There may be additional discretionary credit awarded for partial solutions.

You may:

- work on the problems in any order you choose.
- consult your course books and notes (electronic or paper format).
- consult the course Canvas page and its resources, including your own prior submissions.

You may NOT:

- collaborate with anyone else.
- access the internet (other than the above-stated resources).

Logistics

To get started, please download the SA1Code.zip file from Canvas. Your job is to complete the necessary chips (HDL files) for each problem below.

Grading

The grade for this assignment is 100% based on the HDL of the chips you submit. The grader will use the Hardware Simulator tool, along with our own test scripts, to verify the correctness of your chips. Partial credit will be given for chips that are not fully functional.

Late submissions will lose 1 point (out of 10) per minute past the allotted time.

Deliverables

You must turn in the completed HDL files for all implemented chips.

- Put your full name and UIN in the header comment present in each HDL file.
- You do not need to submit any of the .tst or .cmp files.

Zip all the required HDL files into a compressed file called FirstName-LastName-UIN.zip and submit this zip file to SA1 on CANVAS. If you do not follow these steps properly, you may receive a 0.

Problems

This assessment consists of two problems, each of varying difficulty. There are 10 points total divided among the problems. Please read the instructions and the starter code thoroughly *before* attempting to solve a problem. Partial or complete test scripts are included with each problem.

Problem A **[4 points]**

Task

An Aggie is creating a security chip for his house. The specifications of the chip are given below:

- The chip accepts a 3-digit security code as input along with the identity (ID) code of the person who is trying to enter the house.
- Each family member receives their personalized, unique 3-digit security code:
    - Son: a=0, b=1, c=1
    - Mom: a=1, b=0, c=0
    - Dad: a=1, b=1, c=0
- Each family member also has their unique ID code (MSB i[1] is the first bit, LSB i[0] is the second bit):
    - Son = 00
    - Mom = 01
    - Dad = 10
    - 11 is an illegal state and will not be tested.
- When either an incorrect security code is entered **OR** the entered ID code does not match that of the selected person, the chip will not unlock the door.
- If the security code is correct **AND** the ID code of the selected person is correct, the chip will unlock the door.

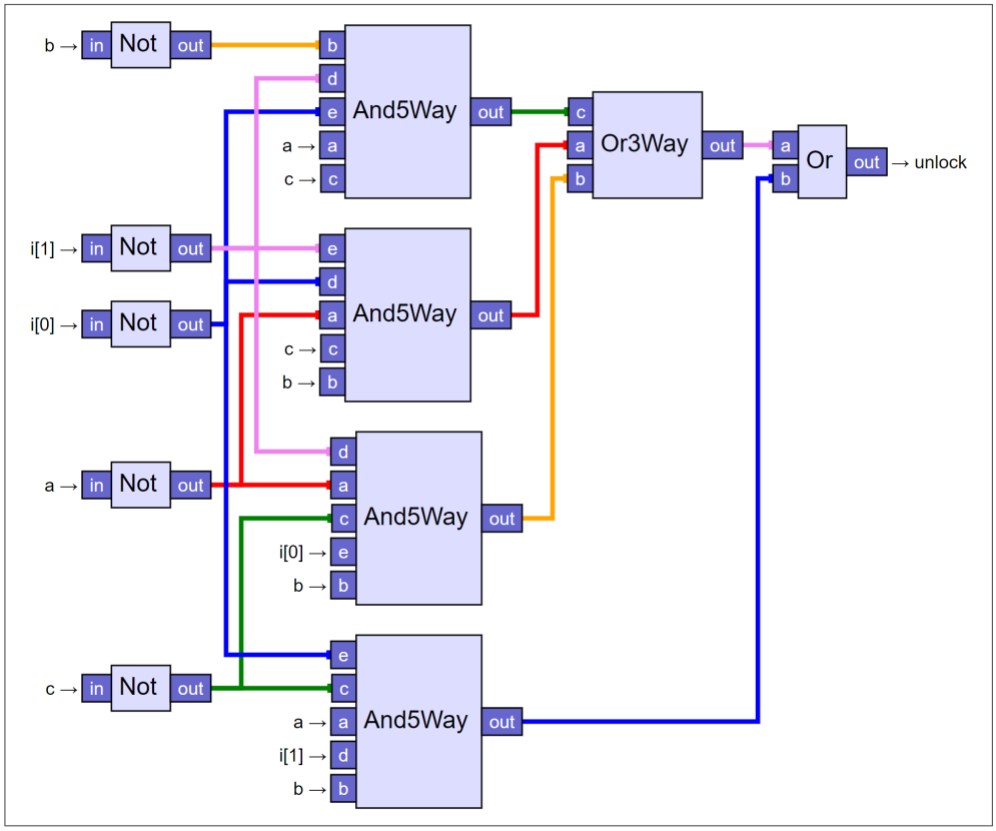
The dad tested the chip, but the results were not satisfactory (refer to the bottom table on Page 4). Specifically, the following issues were noted:

1. The chip unlocks in 4 cases instead of 3 cases.
2. Three cases are found to be implemented incorrectly.

Could you help this fellow Aggie fix his chip and secure the house? Your goal is to find and fix the two bugs that cause the faulty behaviors above. The order of the bugs discovered and fixed is not important. No need to worry about test cases beyond the provided ones.

Schematic

AggiePass.hdl



Note: The above schematic diagram details the ***faulty*** circuit

Rubric

Component	Points
Bug #1	2
Bug #2	2
Total	**4**

Example Test Cases

Expected outputs of the chip:

a	b	c	i[1]	i[0]	unlock
0	1	1	0	0	1
1	0	0	0	1	1
1	1	0	1	0	1
0	0	0	1	0	0
0	1	0	0	1	0
1	0	1	0	0	0
1	1	0	0	1	0
1	1	1	1	0	0

Actual outputs of the implemented chip:

a	b	c	i[1]	i[0]	unlock
0	1	1	0	0	1
1	0	0	0	1	0
1	1	0	1	0	1
0	0	0	1	0	0
0	1	0	0	1	1
1	0	1	0	0	1
1	1	0	0	1	0
1	1	1	1	0	0

Problem B **[6 points]**

Task

You talked to NVIDIA, a major graphics card company, during the SEC Career Fair and got an Online Assessment (OA) from their recruiter. The OA wants you to design a 3-input Majority Chip and verify that your design works as intended. The specifications of the chip are given below:

- **Name**: Majority
- **Description**: The 3-input chip outputs 1 if 1 is the majority bit in the input, and 0 otherwise.
- **Expected outputs**: Given in the Test Cases table shown below.
- **Limitations**: Implementation is limited to 7 or fewer total number of gates, using only the built-in gates from the following catalog: AND, OR, NOT, NAND, NOR.
- **Provided files**: Majority.hdl (incomplete), Majority.cmp (completed), Majority.tst (completed)

Your goal is to complete the Majority.hdl file and run the design through the given .cmp and .tst file to ensure its correctness. The successful completion of this OA will allow you to enter the in-person interview round at NVIDIA's headquarters in Santa Clara, CA along with a private meeting with the company's CEO, Jensen Huang.

Rubric

Component	**Points**
Design compiles without error (correct HDL syntax)	0.5
Only built-in gates	0.5
No more than 7 gates	1
Chip working as intended (passing all test cases)	4
Total	**6**

Test Cases

a	**b**	**c**	**out**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1