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1. V+(15V)

VR=1 KR

6V - WR

VE - WR

FE - WR

4=6V I = 6mA, T = 25.2 & IN O. 2mA

(a) No Load, Vo = ?

 $S_{0}|^{n}$: $V_{20} = 6 - 25 \times 6 \times 10^{-3}$ = $6 - 150 \times 10^{-3}$ = 6 - 0.15

= 5.85 V

I = 0= 15-5.85 = 8.926 mA

·· V. = 5.85 + 8.926×25 = 6.073 V

.. Vo = 6.073 V

(b) R= 4KR, DNO =?

Sol": ic = 6.073 = 0.001518 = 1.518 mA

: DV0 = - 25 x 1.518 =-0.03795 V

NOV = - 37.950 mV

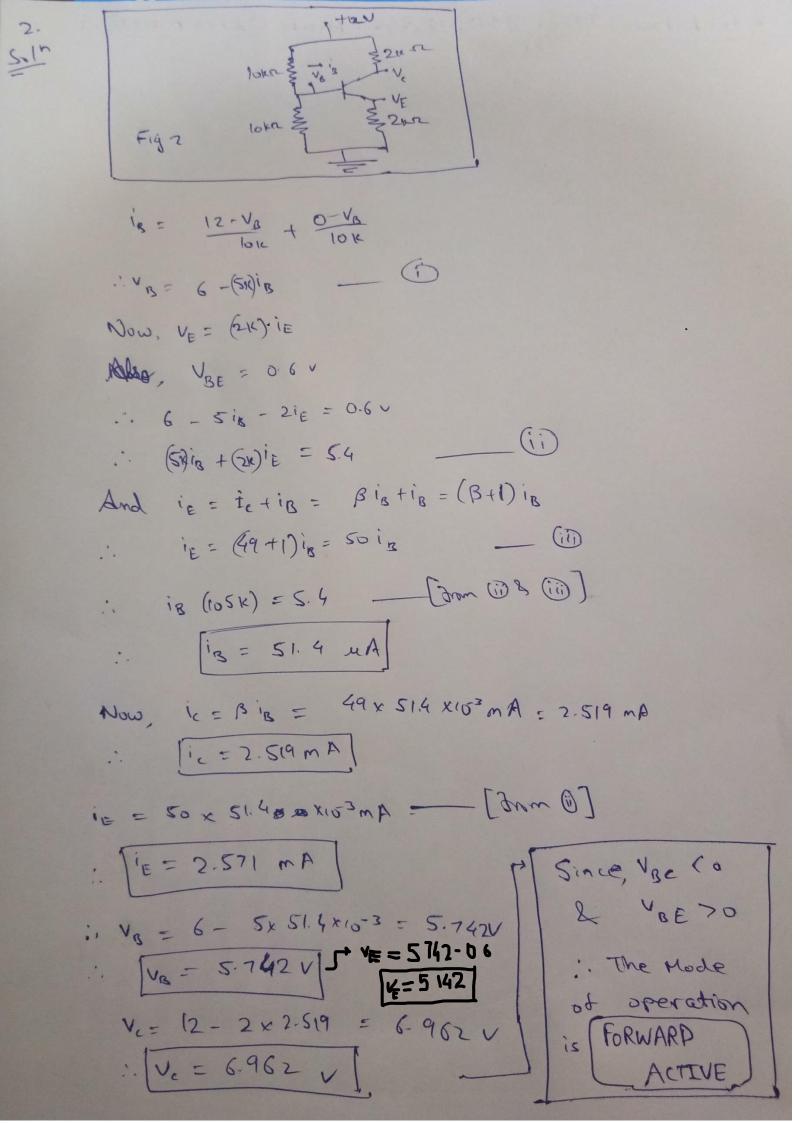
(c) Minimum value of RL for which zener diade will operate =?

Sol7: in = 15-5.85 = 9.15 mA

i = (9.15-02) mA = 8-95 mA

: R = 5.85 KR = 0-65363 X1000 A

: R = 65363 -2



Let's derive a general expression for Vo V. - V1 (-Re) (-Ru) + V- (-R2) - Ru) - Ry V4 = (V1 + V2) (R2 R4) - (R4) (V3 + V4) · Vo = (V, +V2) (R2 R4) - (V3+V4) (R4) (a) If all the Resistors are = R. [3nm 0] (b) R=R, R2 = 2R, R3 = 4R, R4 = 6R From O. :. V. = (V, +V2) (2R) (GR) - (BR) (V3+ V4)
(R) (4R) - (BR) (V3+ V4) =3(V1+V2) - 3 (V3+V4) = 3 V1+V2 - V3 - V4 $V_0 = 3 \left(V_1 + V_2 - V_3 - V_4 \right)$

Amplefication Active Filter (Non-inverting) de = 1500 Hz , fr = 3700 Hz , R = R2 = R3 = R4 = 23KR Band Pass gain (BP6)= (1+ Rg) = (+1) = 2 [:BPG=2] (i) Ce = 1 = 1 = 0.00461 x10= F · · · · (low Pass Capacitance) CL = 46.1 nf EN = 1 = 27 x 23 x 37 x 105 = 0.00 187 x 10-5 F CH = 18.7 MF (High Rass Capacitonice) (ii) Vous = 1 \\
\(\text{Vin} = \frac{1}{\sqrt{1+\left(\frac{4}{5700}\right)}} \times \frac{1}{\sqrt{1+\left(\frac{4}{1500}\right)}} 150 x (1+(±)2)(1+(±)2) 750 V (1+(1)) (4 (1))

4. (iii)
(a)
$$f = fL/4 = 1500/4 = 375 Hz$$
(b) $f = fL$

$$\frac{V_{out}}{V_{in}} = \frac{1}{2} \frac{1}{375} \times \frac{375}{\sqrt{1 + (\frac{375}{5700})}} \sqrt{1 + (\frac{1}{1})^2}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{295} \times \frac{1500}{\sqrt{1 + (\frac{1500}{3700})}} \sqrt{1 + (\frac{1}{1})^2}$$

$$= \frac{1}{2} \frac{4}{\sqrt{1.16435}} = 0.4824$$

$$= \frac{1}{2} \frac{2\sqrt{2}}{\sqrt{1.16435}} = 1.3106$$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{2} \frac{1}{375} \times \frac{375}{\sqrt{1 + (\frac{1}{4})^2}} \times \frac{1}{\sqrt{1 + (\frac{1}{4})^2}}$$

$$\frac{-1}{2} \frac{2\sqrt{2}}{\sqrt{1.16435}} = 1.3106$$

$$V_{out} = (1.3106) V_{in}$$

(c)
$$f = f_H$$

 $\frac{V_{out}}{V_{in}} = \frac{1}{1} \cdot \frac{1}{1} \times \frac{(3700)^2}{\sqrt{1+(1)^2} \sqrt{1+(\frac{3700}{1500})^2}} = \frac{1}{1} \cdot \frac{1}{1+(\frac{3700}{1500})^2} \times \frac{4 \times 3700}{\sqrt{1+(\frac{3700}{1500})^2}} = \frac{1}{1+(\frac{3700}{1500})^2} \times \frac{1}{1+(\frac{3700}{1500})^2} \times \frac{1}{1+(\frac{3700}{1500})^2} = \frac{1}{1+(\frac{3700}{1500})^2} \times \frac{1}{1+(\frac{3700}$

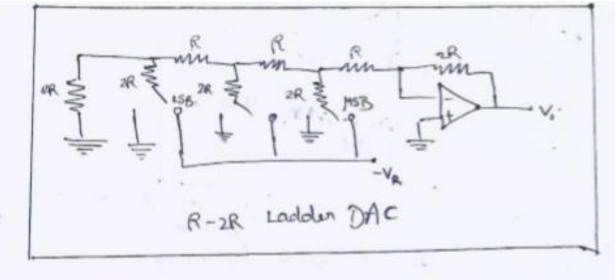
$$=\frac{1}{2}\frac{4.867}{\sqrt{2}\sqrt{7.0844}}=1.3106$$

= 39.468 1 = 0.4824

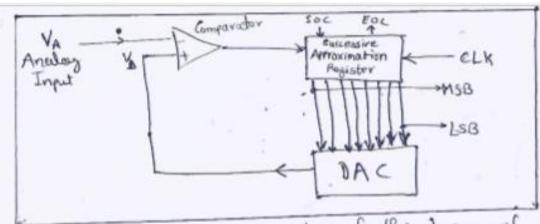
$$\sqrt{17}\sqrt{98351}$$
 2

5. 6 Rs = 5 KR, Rp = 12 KR, CB = 47mf, Cp = 35nf Here based on the terminologies, R=5KR, R=12KR, G=47nf & C2=354 Wien Bridge Oscillator (i) As we know, iw Raci 1- wir, R2 (1 (2 + 1 w (R, G + R2 G + R2 G) IN (54193) (47×169) 1-W (12 x 5x 108) (47x35 x 108) + iw (5x 47+35x 12+12x47) x 106 in (564) x10 6 1 - 102 (987 × 10-10) + 110 (1219) ×10-6 sw(564) 106 - W (987X10-4) +jw (1219) 1772.049-02 (1.75×10-4)+3W(2.161) = 177 3-049 -W- (1.75 x 107) + jw(2-161) 271 N 6 X10 7 X 47 X35 X 10 18 27 N 987 X 16 10 (ii) f = _1 21 187 = 506.595 Hz : f = 506. 595 Hz for W= 1 A B to the real

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6.



The basic type principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB.

This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps:

(1) The MSB is initially set to I with the remaining remaining 7 bits set as 0000000. The digital equivalent valtage is

compared with the unknown analog input voltage.

(2) If the analog input voltage is higher than the oligital equivalent voltage, the MSB is retained as I and the second MSB is set to 1. Otherwise, the MSB is set to a and the second MSB is set to I Comparison is made as given in step (1) to decide whether to retain as reset the second MB

An 8-bit ADC was used. In order to find the input voltage we know the output signal = 011 00101 Hence, the input voltage would have been = 26+25+22+1.

From here we have to reverse Engineer how the conversion

would have started. (i) MSB bit is set to 1 8= @[10000000]2= 128v > VA=101v

(ii) .. VD = [01000000] Z = 64 V (VA = 102V

(11) Than , rece the next bit as I, Vo=[01100000]2= 96V < VA=101V

step token	Status
(11)	Approved
	I.

Approved (2)

Approved (1)

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Status Step Not (iv) Again keep the next bit as I Approved (1) Vo= 01110000]2=112V 7 VA=101V Not Approved (2) (V): V= [01101000]z = 104V 7 1/= 101v Approved (2) (vi) : V = [01100100]2 = 100V < VA = 101V Not (1) Approve (vii) Now, y=[01100]10]2=102V > Y=101V Approved & (viii) Finally, VD=[01100101]2 = 101V = (VA=101V) (2) Auepted This is how we got the output digital 01100101. Page 9 as