Assignment No: 6

Title :- Parity Generator

Objective :- Learn Even / Odd parity Generator / Checker using logic gates

Problem statement :- Design & Implement Parity Generator using EX-OR

Hardware & software requirement :-

Digital Trainer kit, IC 7486 (Ex-OR), IC 7404 (NOT), IC 74180, Patch cord, +5V Power Supply

Theory :-

In digital communication, the digital data is sent over the telephone lines using different binary codes.

During the transmission, because of noise signal 0 may become 1 or vice versa and wrong information may be recieved at destinations.

That's why at the recieving end, Parity will be checked.

Parity :- A term used to specify the number of one's in digital world as odd or even.

Parity checker: At recieving end a logic circuit is used to check the parity of recieved information.

Even bit parity code :- The total number of ones in parity code word is even.

Odd bit parity code :- The total number of Ones in parity code word is odd.

Limitations :-

1) The one bit parity code word can detect one bit error.
2) It cannot detect the location of error & hence error cannot be corrected.

A] Even Parity Generator.

Truth Table :-

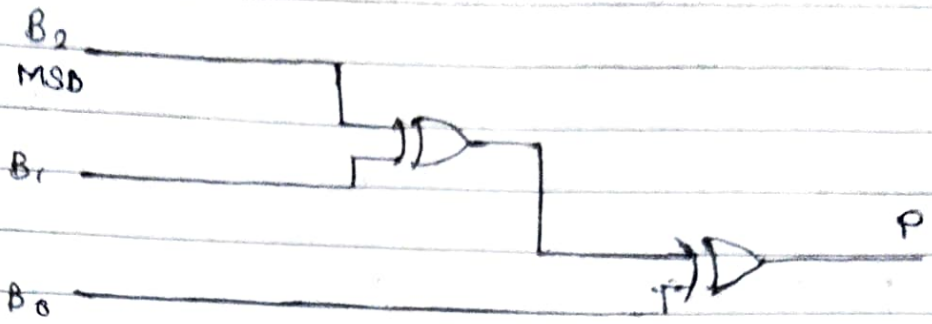
INPUT			OUTPUT
B_2	B_1	B_0	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

2) K-map for reduced Boolean Expression of output

B_2 \ B_0B_1	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$P = B_2 \oplus B_1 \oplus B_0$

3) Circuit Diagram :-
Even parity generator



B) Odd Parity Generator

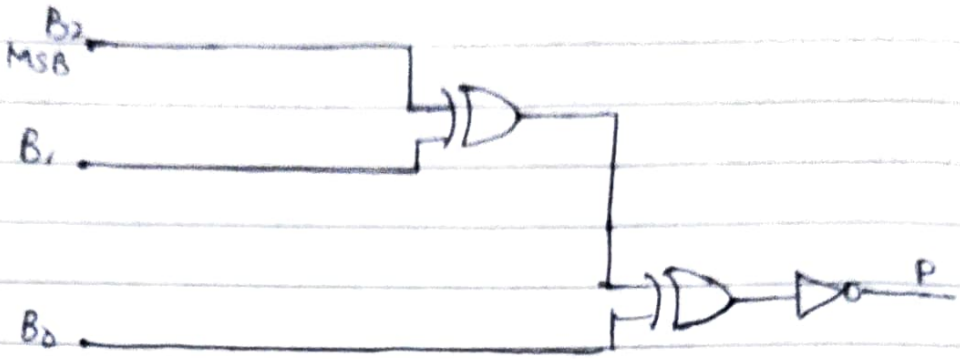
INPUT			OUTPUT
B_2	B_1	B_0	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

2) K map for reduction of boolean expression

B_2 \ B_1B_0	00	01	11	10
0	1	0	1	0
1	0	1	0	1

$P_1 = B_2 \oplus B_1 \odot B_0$

9) Circuit Diagram :-



Outcome :-

Thus, we studied Parity generator / checker and their working & limitations.