Assignment No. 5

- Title:- Multiplexer / Demultiplexer
- Objective:- To learn different techniques of designing multiplexer
- Problem Statement:-
  Design & Realization of Boolean Expression for suitable combinational logic using MUX 74151 / DMUX 74154
- Hard ware and Software requirements:-
  Digital trainer board, IC 74151, IC 7404, IC 7432, patch cords, +5V Power supply.

- Theory:
  1. What is multiplexer?
     - Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. Basic multiplexer has several data inputs and a single output line.
     - The selection of particular input line is controlled by a set of selection line.
     - Strobe:- It is used to enable/disable the logic circuit.
     - Mux is single pole multiple way switch.
  2. Necessity of multiplexer:-
     - In most of the electronic system, digital data is available on more than one lines. It is necessary to rotate this data over a single line.
     - It select one of the many I/P at a time.

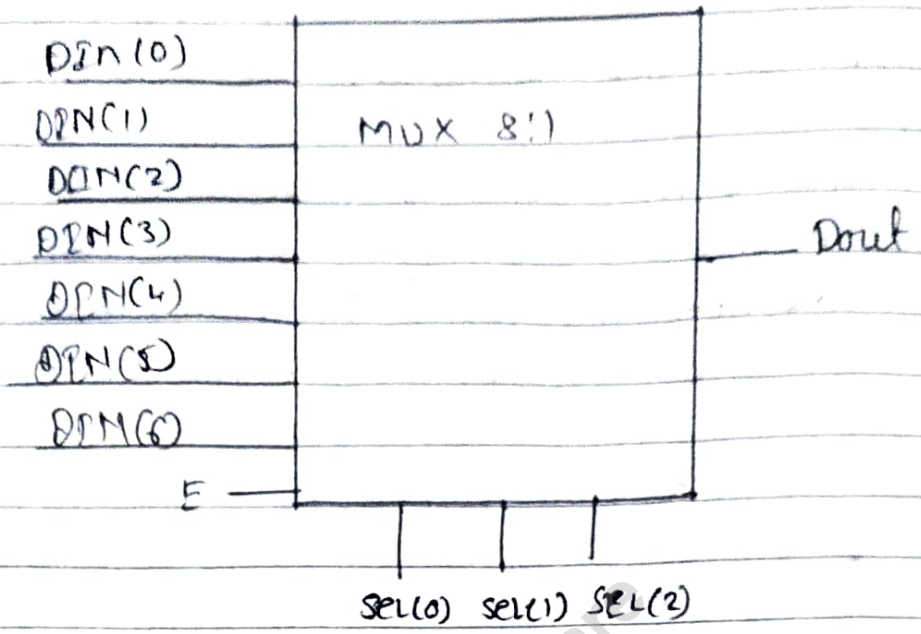
- Multiplexer improves the reliability of digital system because it reduces the number of external wire connection.

4. Application of MUX:-
   - Data Selector to select one out of many data I/P
   - In Data Aquisition system.
   - In the D/A converter.

8:1 MUX:
The block dig. of 8:1 MUX & its TT is shown. It has eight data I/P & one enable input.

Operating principle:-
When the Strobe or Enable input is active low, we can select any one of eight data I/P & connect to O/P.

Design:-



SELECTION LINES			STROBE	OUTPUTS	
C	B	A	E	Y	$\bar{Y}$
X	X	X	1	0	1
0	0	0	0	D_0	$\bar{D_0}$
0	0	1	0	D_1	$\bar{D_1}$
0	1	0	0	D_2	$\bar{D_2}$
0	1	1	0	D_3	$\bar{D_3}$
1	0	0	0	D_4	$\bar{D_4}$
1	0	1	0	D_5	$\bar{D_5}$
1	1	0	0	D_6	$\bar{D_6}$
1	1	1	0	D_7	$\bar{D_7}$

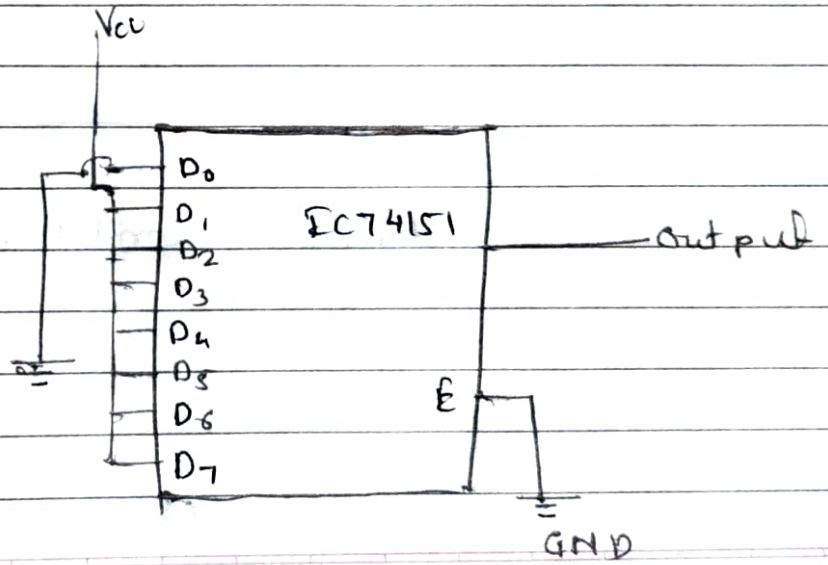
X = dont care condition.

Part 1 : MUX as a function generator

Convert the given Boolean expression into a standard SOP / POS format if required & complete the logic diagram design accordingly for realization of the same.

i] $Y = \Sigma m(0, 2, 3, 4, 5, 6, 7)$

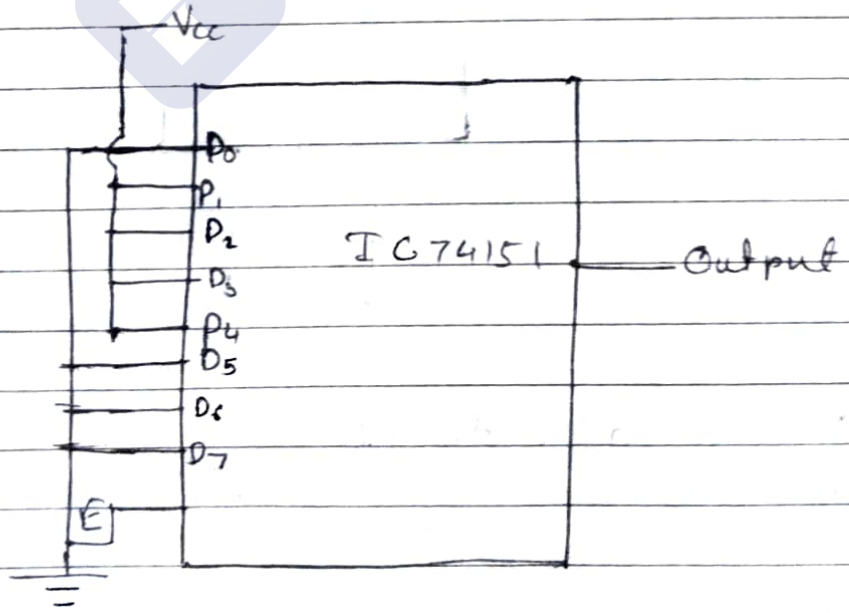
SELECTION LINES			STROBE	OUTPUTS	
C	B	A		Y	$\bar{Y}$
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	0



ii] $Y = \pi M(0, 5, 6, 7)$

SELECTION LINES			STROBE	OUTPUTS	
C	B	A		Y	$\bar{Y}$
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1

POS realization Diagram

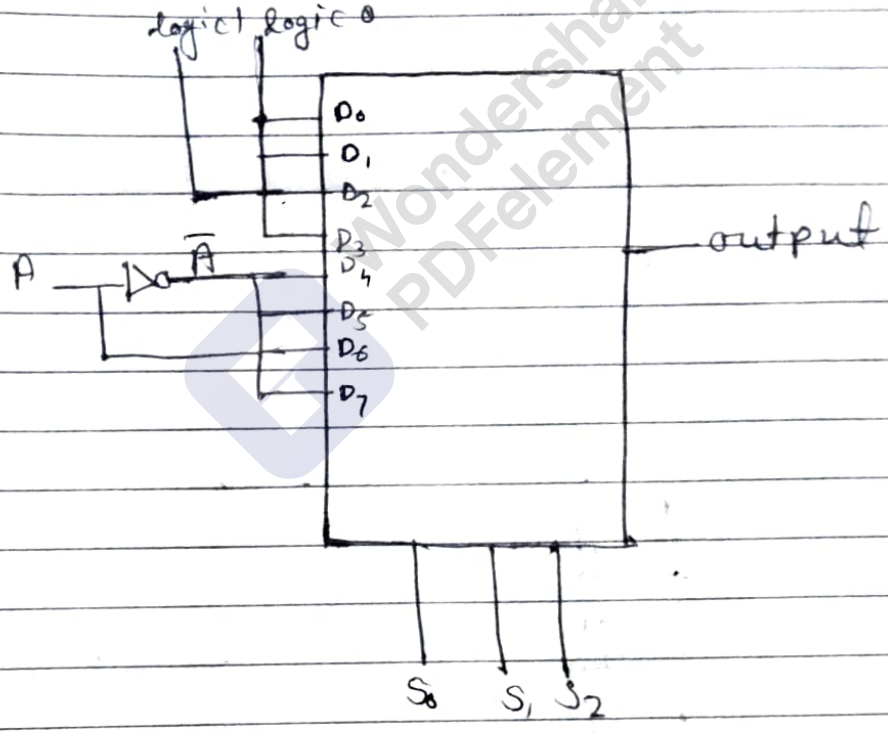


Part 2 : Implementation of 16:1 MUX using 8:1 MUX

Use hardware reduction method & implement the given Boolean expression with the help of neat logic diagram

$F(A,B,C,D) = \Sigma m(2,4,5,7,10,14)$

16:1 MUX using 8:1 MUX Diagram

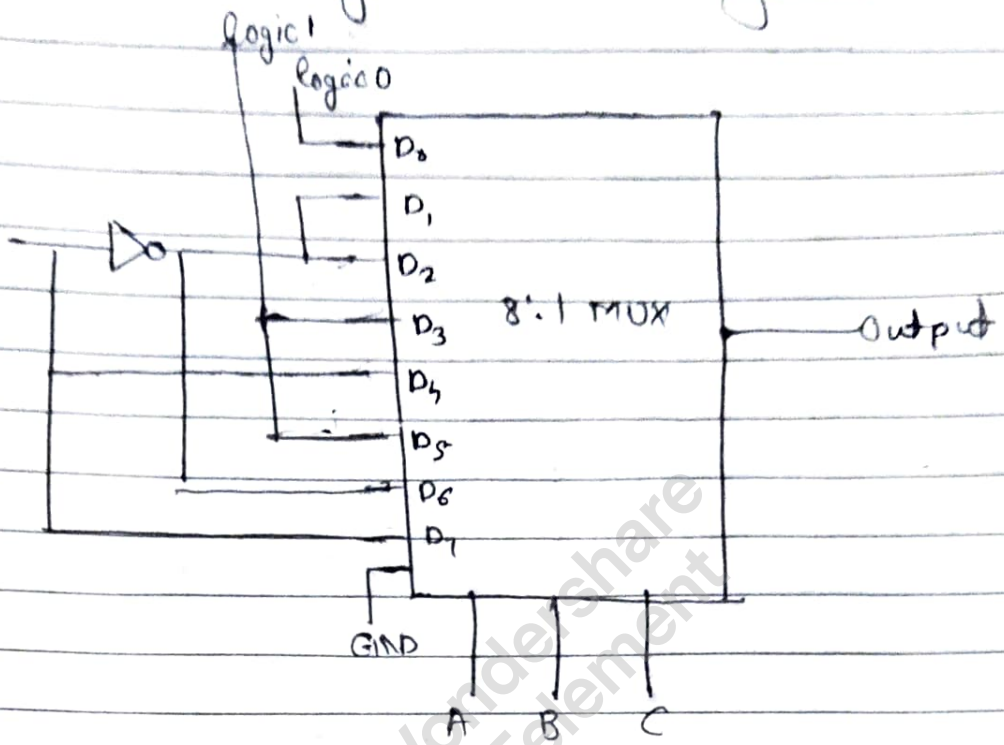


Reduction method :

1. Make a combination of pair according to same values of A, B, C,
2. Check output values with respect to value of D.

A	B	C	D	output	Output
0	0	0	0	0	0
0	0	0	1	0	
0	0	1	0	1	$\overline{D}$
0	0	1	1	0	
0	1	0	0	1	$\overline{D}$
0	1	0	1	0	
0	1	1	0	1	1
0	1	1	1	1	
1	0	0	0	0	D
1	0	0	1	1	
1	0	1	0	1	1
1	0	1	1	1	
1	1	0	0	1	$\overline{D}$
1	1	0	1	0	
1	1	1	0	0	D
1	1	1	1	1	

16:1 MUX using 8:1 MUX Diagram



Implementation of 16:1 MUX using two 8:1 MUX

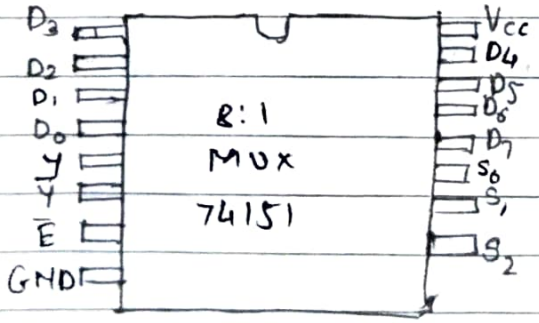
$F(A,B,C,D) = \sum m(2,4,5,7,10,14)$

→ STEP 1 : Connect S_1, S_2, S_0 select lines of two 8:1 MUX parallel whereas MSB select input is used for enabling MUX.

Step 2: S_3 is connected directly to the enable (E) to mux-2 where as $\overline{S_3}$ is connect to enable input of mux-1.

- Truth table :-

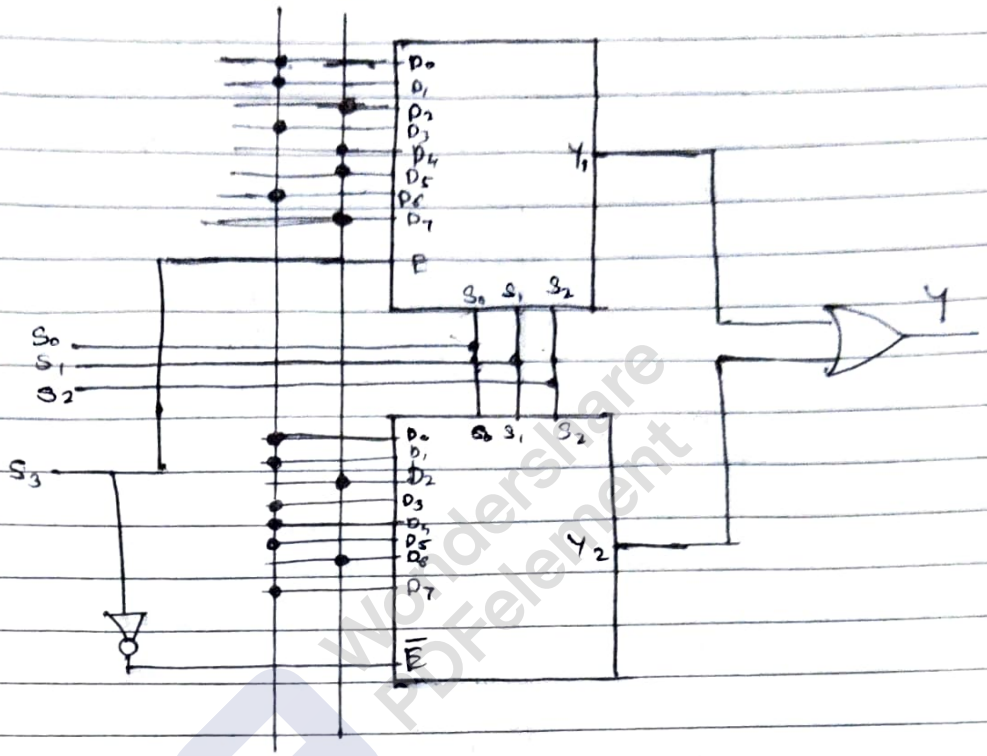
Select line				Output		Final Output
S_3	S_2	S_1	S_0	Y_1	Y_2	Y
0	0	0	0	D_0	-	D_0
0	0	0	1	D_1	-	D_1
0	0	1	0	D_2	-	D_2
0	0	1	1	D_3	-	D_3
0	1	0	0	D_4	-	D_4
0	1	0	1	D_5	-	D_5
0	1	1	0	D_6	-	D_6
0	1	1	1	D_7	-	D_7
1	0	0	0	-	D_8	D_8
1	0	0	1	-	D_9	D_9
1	0	1	0	-	D_{10}	D_{10}
1	0	1	1	-	D_{11}	D_{11}
1	1	0	0	-	D_{12}	D_{12}
1	1	0	1	-	D_{13}	D_{13}
1	1	1	0	-	D_{14}	D_{14}
1	1	1	1	-	D_{15}	D_{15}



Ē :- Active low enable

Ȳ = complement output

Multiplexer tree according to given equation :-



Outcome:

Multiplexer is used as a data selector to select one out of many data inputs.

It is used for simplification of logic design.

It is used to design combinational circuit.

Use of multiplexer minimizes no. of connections.

FAQ:

1. Enlist application of MUX.

1. MUX is used as data selector.
2. It is used to design combinational circu
3. Less number of wires required which reduces complexity
4. There is no need to design K-map.
5. We design equation using truth table.