ASSIGNMENT NO. 3

Design and Implement Code Converters Binar to Gray and BCD to Excess 3 code

Objectives: of To Understand concept of code converters.

Hardware requirements:

Digital - trainer hit, Ta404, EC7408, JC7432, Po cord, tov Power Supply

To design combinational arcuits wing K-map &

Boolean algebra.

1. Binary to Gray code Converter 1-

Gray rade system is a binary number system in which every succesive pair of number idiffers in only one bit. Hormal Binary may

graduce an error during transmission from one number to next

For Example, the states of system may change from 3 (011) to 4 (100) as D11 - 001 - 101 - 100

The Gray code eliminates this problem since only one bit changes its value during any translation detuperen tope numbers.

-	-	Bim	-	- 1	Gray					
	ba	b2	b,	b	3	9,	9,	9.	L	
	0	0	0	0	0	0	0	0	1	
	0	0	0	14	0	٥	0	1,0	L	
	0	٥	1	0	0	0	1	1	L	
	0	0	(1	0	0	1	0	_	
	10	1	6	0	0	1	1	0	L	
	0	1	0	4	0	1	1	1		
	0	1	1	0	٥	10	0	1	L	
	0	1	3	1	0	G	O	0	6	
	1	٥	. 0 .	0	138	1	0	0		
	1	ð	٥	1	1	9-	0	W		
	+	0	1	0	1	1)	1 6	1		
ŀ	(0	VI		21	1	1	6		
Ì	1	1.	0	0	1	0	1/2	0		
t	1	Vi	0	1	1	0	1	1		
١	.1	· 64 :	1.	0	1.	10	0	1		
١	1	1.	1	1	4	0	0	0		

To final the corresponding digital circuit, were

K-map - for go

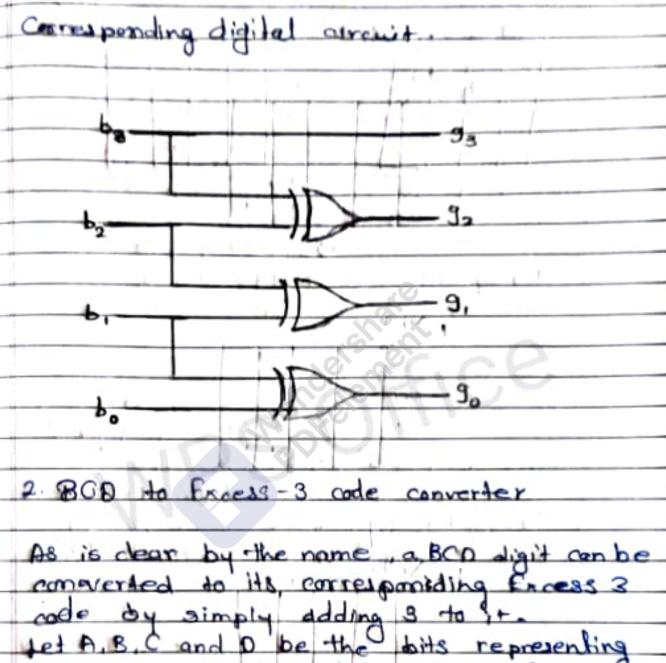
	_	The .				-
	302	00	01	11	61	
11 2 2	,00	0	1	0	_	
	1 01	٥	1	6	4	
	11	0	1	0	-1	
	10	0	.1	0	1	

K-map for g.
haba 00 01 11 10
00 0 0 1 7
01 1 1
11 1 1 0 0
10 0 0 1
K-map for g2
Ash 6, 60 01 11 10
01 1 1 0
11 0 0 0 0
10 10 10
Kmap for gr
The state of the s
baba 60 01 11 60
000000
01 0 0 0 0
10 1 1 1
Corresponding minimzed doolean expression
90 = bob, + b, bo = bo 10 b,
0 1 01

92 = b2 € b9 93 = b3

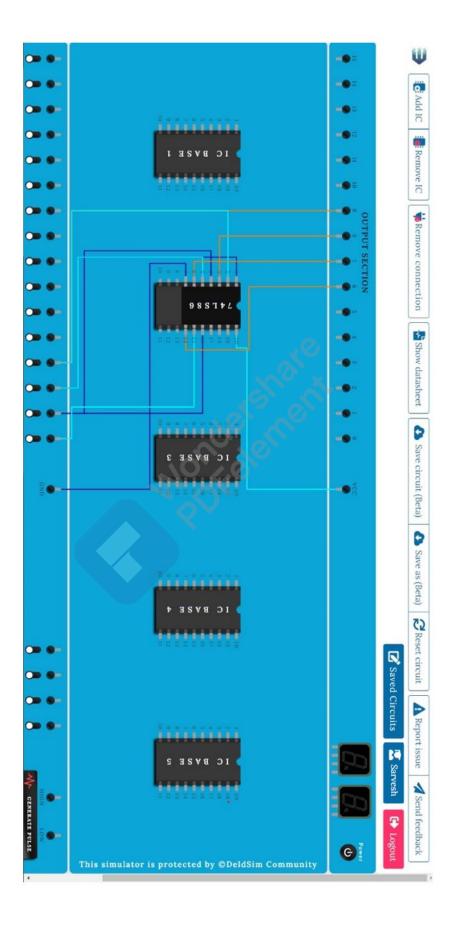
b, @ b2

91=



the binary numbers where D is the 1SD and A is the MSB.

Let w, x, y, x be bits representing ers-3



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The true	tha	del	€ -	For J	ha	Cany	ctai	nà is	aiven
enbed						•			0
	٠,				-		_	,	-
+	BCD (R4					Excess-2			
	/A'	В	C	O	W.	7	Y	Z	
4	٥	0	. 0	8	0	10	1	'	
	0	ø	0	1	0	1	٥	0	
	٥	0	1	0	0	14	0	1	
	0	0	ياني	1	0	. 6		٥	
	0	ı	0	0	0	1.	1	١	
	٥	1	٥	1	11	0	6	0	
	0	1		0		0	6	1	
	0	1	1	(C)		0	1	O.	
	1	D	٥	01	1	0	1.	3) .	
	1	٥	0	1	1		0	0	
A. A. A.	1	0	Ĭ	0	K	*	X	X	
	V	0	2.1	1	×	×.	×	×	
it		11.	0	9	A.	A	N	K	
	311	t'	6	1	*	×	K	×	
	1	1	-	0	~	^	×	×	
	1	'	l	U	*	*	5	×	
K-map -	100	ex	eas.	5 3	mele	211			- 22
	10	nhi			10		116 11	9.3	
AB CD		1		- 6	ABC	-	4.	-	
1		11			\rightarrow	1	1	\vdash	
		-11'	_		_	1	1		
×	*	×	1_		_	* 7	C K	×	
11		KK				1	7	ŽĮ.	
.7	= b'					. *	= CD	+00	

				Dute Page	
a cr					
40.6	7,1,1	11	7	111	
	1		-	1.1.1	
	× × × ×	× .	1/2	x x x	
1	1 1	X	TAT	1 × ×	
	x' = B'C + B'	h+BC'D'	1	A+BC+BD	
YI .	0.10			P. T. D. C. III.	
	W= A+	BC+BO	2		
		P'D +BC'	5'	~	
1	7 = D'				
	Z = D'	(0)	8		
_		10:50			
Proced	ure:-		14	160	
1. Verif	y the gate	23	+11	100	
2. make	e the mo	nections	asper	the circuit	الم
3. du	itch on V	and o	pply "	values com	bi
-100%	of input	amordi	og lo	the truth	44
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are d	esigned.		7	1 1	200
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3.1		19.5	1 1	7	_
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