ASSIGNMENT NO. 4

Title :- BCD Adder

Objective :- To learn different types of adder

Problem statement :- Design and Realization of BCD Adder using 4-bit Binary Adder (IC 7483).

Hardware and Software requirement :-
Digital Trainer Kit, IC 7483, 7432, 7408, Patch cord, +5V Power supply.

Theory :

- BCD Adder :- It is a circuit that adds two BCD digits and produces a sum of digits also in BCD. BCD Numbers we 10 digits, 0 to 9 are repsented in the binary form. i.e. each bit digit is represented as 4-bit binary number

Rules for BCD Addition

1. Add two numbers using rules of Binary addition
2. If the 4 bit sum is greater than 9 or if carry is generated then the sum is invalid. To correct add 0110. to sum.
3. If the 4-bit sum is less than 9 or equal to 9 then sum is in proper form.

Case1 : sum ≤ 9 & carry = 0

Add BCD digit 3 & 4

$$\begin{array}{r} 0011 \\ +\ 0100 \\ \hline 0111 \end{array}$$

Answer is valid BCD.

Case II: Sum > 9 & carry = 0

Add BCD digits 6 & 5

```
  0110
+ 0101
------
  1011
```

Invalid BCD so 0110 is added

```
  1011
+ 0110
------
1 0001
```

Valid BCD result = 11

Case III:

Sum ≤ 9 & carry ≠ 1

Add BCD digits 9 & 9

```
  1001
+ 1001
------
 10010
```

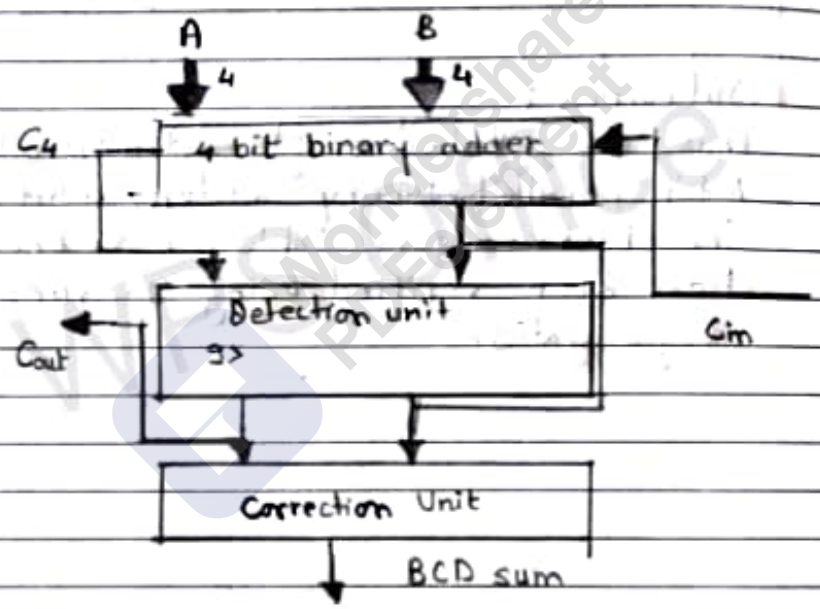
Invalid BCD so 0110 is added

```
 10010
+  0110
-------
 11000
```

Valid BCD result = 8

Design of BCD Adder :

1. 4 bit binary adder : Is used for initial addition. i.e. Binary addition of two 4 bit numbers.
2. Logic circuit : To sense if sum exceed 9 or carry = 1, this digital circuit will produce high output otherwise its output will be 0.
3. One more 4-bit adder to add (0110)$_2$ in the sum is greater than 9 or carry is 1



Truth table for BCD Adder

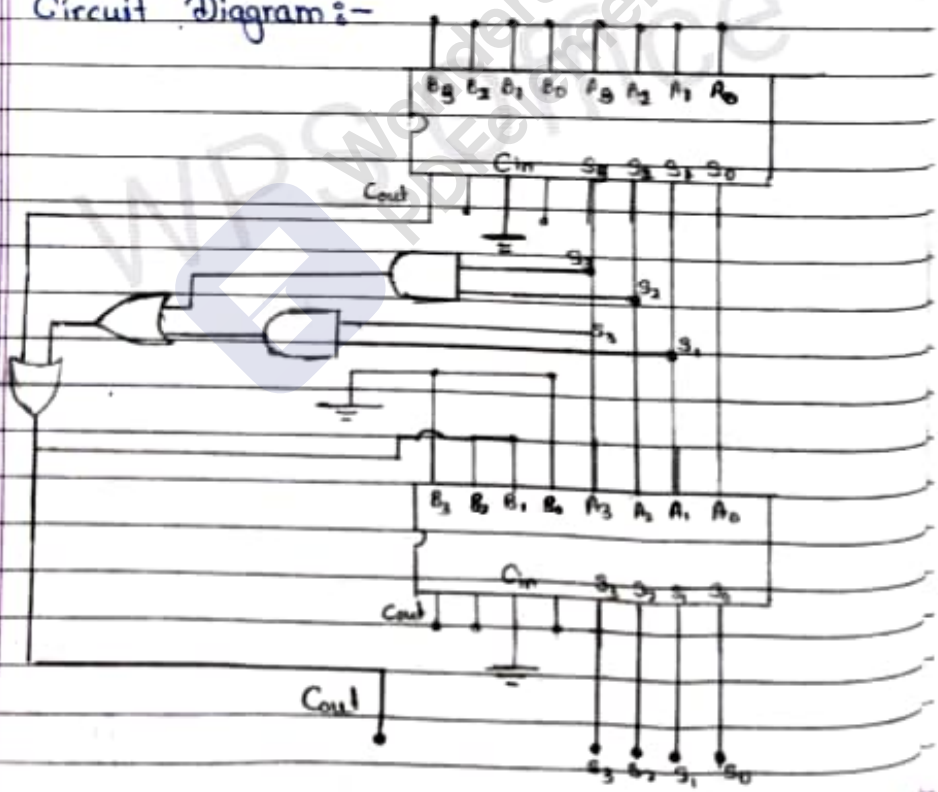
INPUT				OUTPUT
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

K-map :-

S_3S_2 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

$Y = S_3S_2 + S_3S_1$

Circuit Diagram :-



Observation table : of BCD Adder

INPUT								OUTPUT				
1st Operand				2nd Operand				MSD	LSD			
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Cout	S_3	S_2	S_1	S_0
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	1	0	0	1	0	1	1	0	0	0	1
1	0	0	1	1	0	0	1	1	1	0	0	0

Out comes :

Thus we studied single bit BCD adder using 4 bit parallel binary adder / 4 bit full adder the observation table has been verified have been verified using IC 7483 & some logic gates.