A REPORT ON
ANALOG ASSIGNMENT

ANALOG AND DIGITAL VLSI DESIGN
EEE F313

Submitted by

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Submitted in partial fulfilment of the course:
Analog and Digital VLSI Design

Under the Guidance of:
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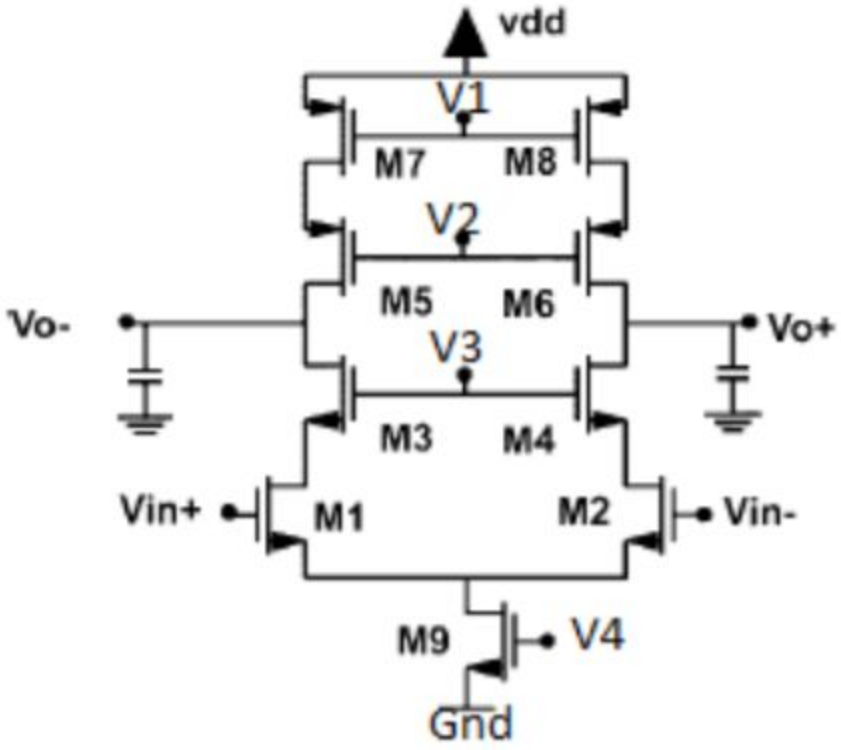
1 Problem Statement

Design a low power sum/ difference amplifier using telescopic OPAMP as shown in figure in **subthreshold region** with the required specifications

a) Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications.
b) Open loop gain(DC gain) ≥ 100 dB with slew rate≥ 100V/usec
c) UGB≥ 60MHz
d) Power consumption=< 1uW
e) Show a biasing circuitry to bias all the voltages in your design (except the input).
f) Also calculate the following parameters for your OPAMP: Bode plot for AC gain and phase margin, slew rate, ICMR, Differential output swing (dc + Transient), input offset voltage and power consumption.



2 Specifications

Parameter	Requirements
Technology	TSMC 180nm technology (Lmin = 350nm)
V_{DD}	2.5 V
Open loop gain	≥ 100 dB
Slew rate	≥100 V/us
UGB	≥ 60 MHz
Load capacitance C_L	≤1 pF
Current mirror ratios	≤20
Power dissipation	≤1 uW
Reference Current	Single Ideal Current Source of an arbitrary value, with positive node tied to V_{DD} or negative node tied to ground
Phase Margin	50 to 60 degrees

3 NetList

```
Telescopic op-amp in subthreshold

.lib ".\tsmc018.lib"

**Circuit**

Vdd 5 0 {vdd}

*---Telescopic op-amp---

M1 2a 1a 1 0 CMOSN W={w1} L={l}
M2 2b 1b 1 0 CMOSN W={w1} L={l}
M3 3a 2 2a 0 CMOSN W={w2} L={l}
M4 3b 2 2b 0 CMOSN W={w2} L={l}
M5 3a 3 4a 5 CMOSP W={w3} L={l}
M6 3b 3 4b 5 CMOSP W={w3} L={l}
M7 4a 4 5 5 CMOSP W={w4} L={l}
M8 4b 4 5 5 CMOSP W={w4} L={l}
M9 1 1g 0 0 CMOSN W={w0} L={l}

*---Gain boost stage---

M10 6a 3a 5 5 CMOSP W={w5} L={l}
M11 6b 3b 5 5 CMOSP W={w5} L={l}
M12 6a 1g 0 0 CMOSN W={w6} L={l}
M13 6b 1g 0 0 CMOSN W={w6} L={l}

*---Biasing circuit---

M14 1g 1g 0 0 CMOSN W={w7} L={l}
M15 2 2 1g 0 CMOSN W={w8} L={l}
M16 3 3 4 5 CMOSP W={w9} L={l}
M17 4 4 5 5 CMOSP W={w10} L={l}

Iref 3 2 58.1671n

*---External capacitors---

CE1 3a 0 1f
CE2 3b 0 1f
CL1 6a 0 0.1f
CL2 6b 0 0.1f
```

```
Cc1 2a 6a 25f
Cc2 2b 6b 25f

*---Source voltages for different analysis types---

Vin1 1a 0 ac sin(0.56 2m 10k)
Vin2 0 1b ac sin(-0.56 2m 10k)
*Vin1 1a 0 pulse(0 1 0.1m 1n 1n 5 5)
*Vin2 1a 1b 0
*Vin1 1a 0 0.56

.param vdd=2.5
.param l=0.35u
.param w0=5.5u
.param w1=10.33u
.param w2=5.8u
.param w3=1.0u
.param w4=0.3u
.param w5=0.7u
.param w6=15.4u
.param w7=5.5u
.param w8=3u
.param w9=17.988u
.param w10=0.8616u

*.op
*.ac dec 100 1 100g

*.tf V(6a) Vin1
*.tran 4ms 6ms 0.1ms
*.dc Vin1 0 2.5 0.1
*.temp 0 27 100
```

4 Schematic

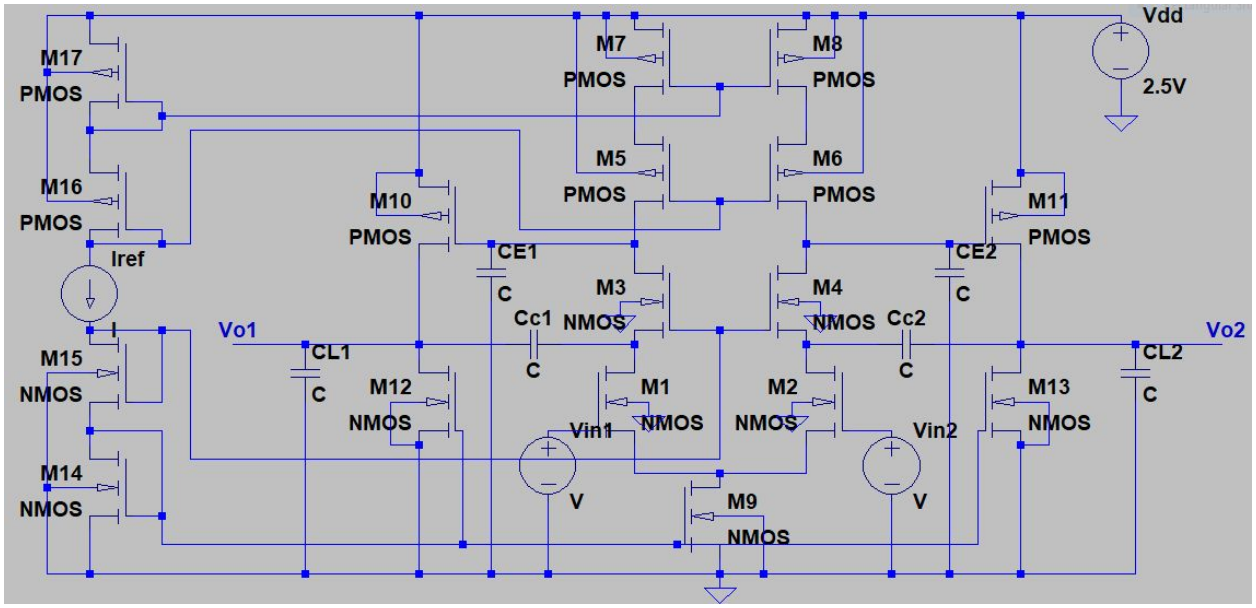


Figure 4.1. Schematic of the difference amplifier implemented

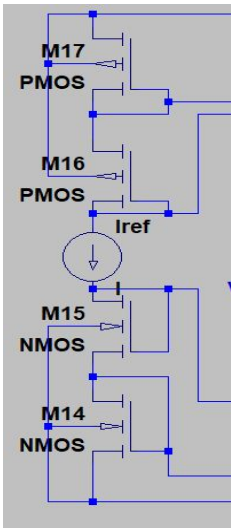


Figure 4.2- Biasing Circuit

5 W/L Tables for MOSFETS

MOS	W	W/L
M1,M2	10.33u	29.51
M3, M4	5.8u	16.57
M5,M6	1u	2.86
M7,M8	0.3u	0.86
M9	5.5u	15.71
M10,M11	0.7u	2.00
M12,M13	15.4u	44.00

Table 5.1- W/L Ratios for Telescopic OPAMP Circuit

MOS	W	W/L
M14	5.5u	15.71
M15	3u	8.57
M16	17.988u	51.39
M17	0.8616u	2.46

Table 5.2- W/L Ratios for Biasing Circuitry

6 Results

Open Loop Gain

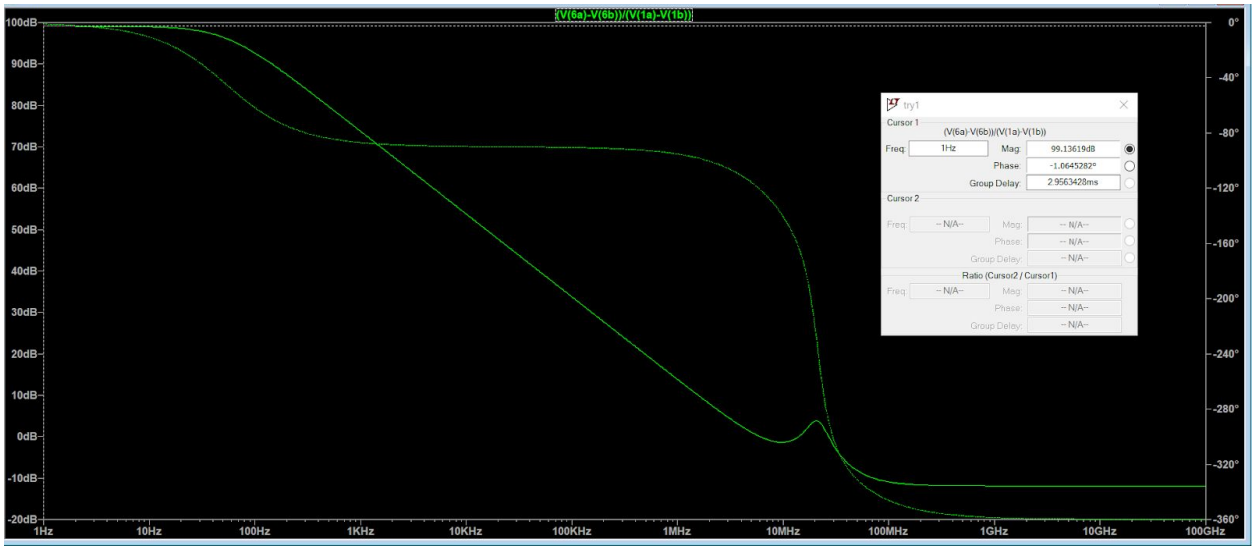


Figure 6.1- Bode Plot Open Loop Gain

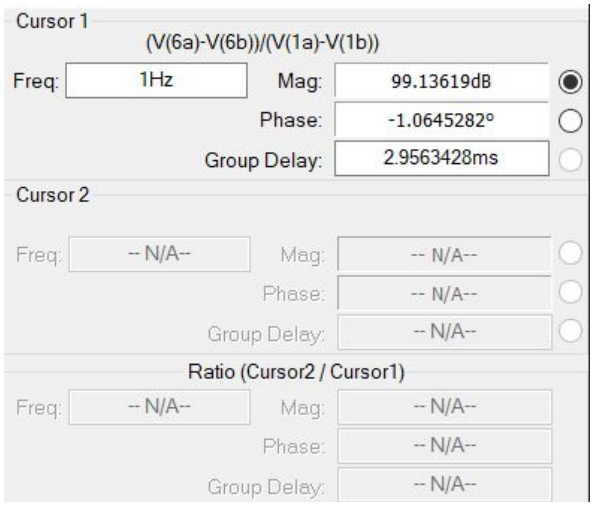


Figure 6.2- Pop up window to find Open Loop Gain

Phase Margin and UGB(Unity Gain Bandwidth)

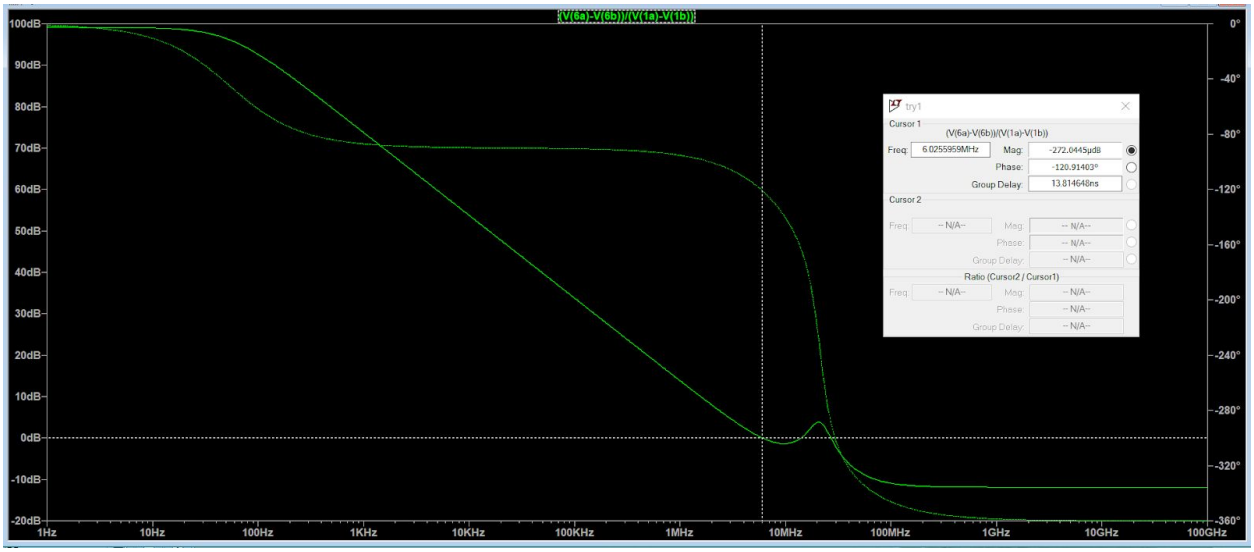


Figure 6.3- Plot to calculate Phase Margin and UGB

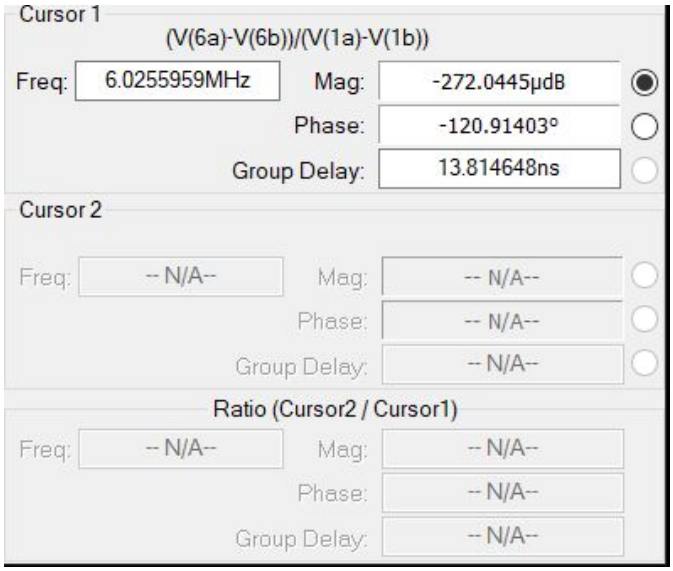


Figure 6.4- Pop up window to Calculate Phase Margin and UGB

Slew Rate

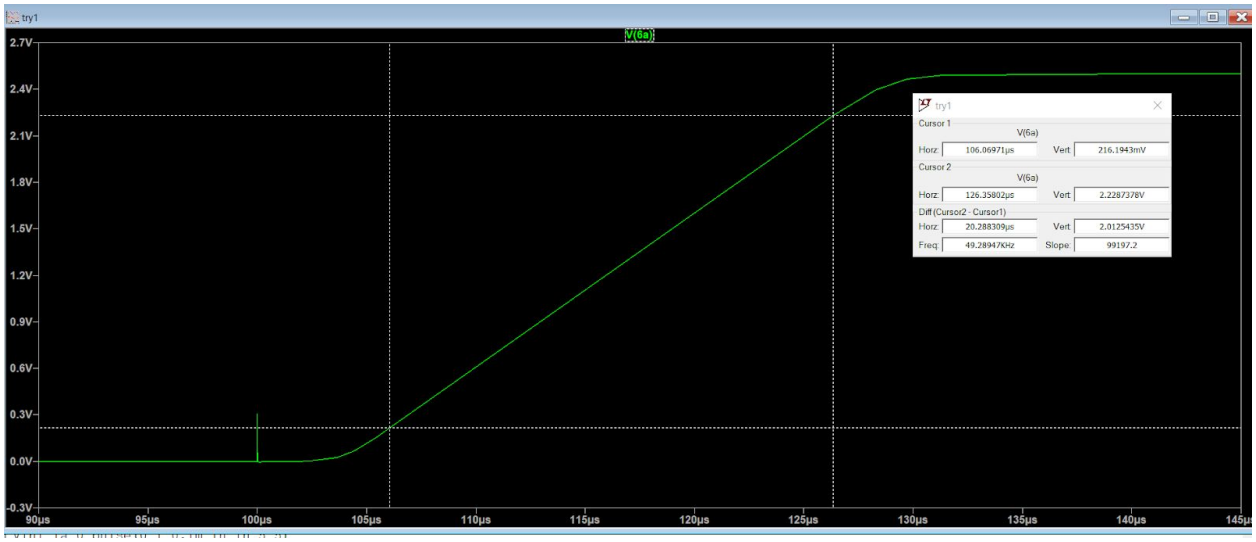


Figure 6.5- Plot to Calculate Slew Rate

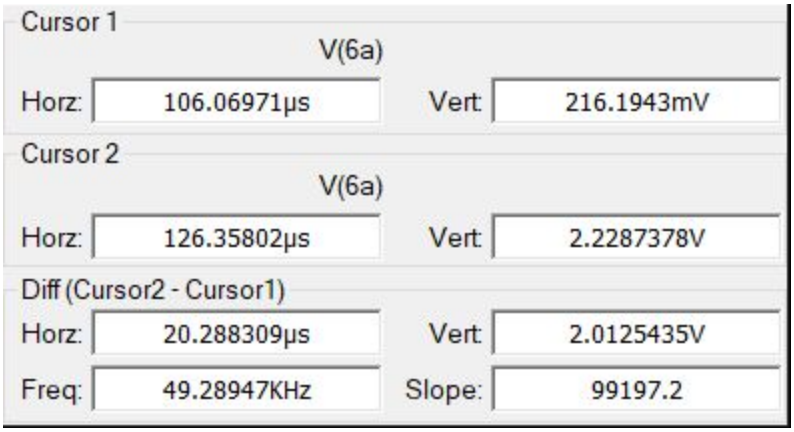


Figure 6.6- Pop up Window for calculating slew rate

ICMR

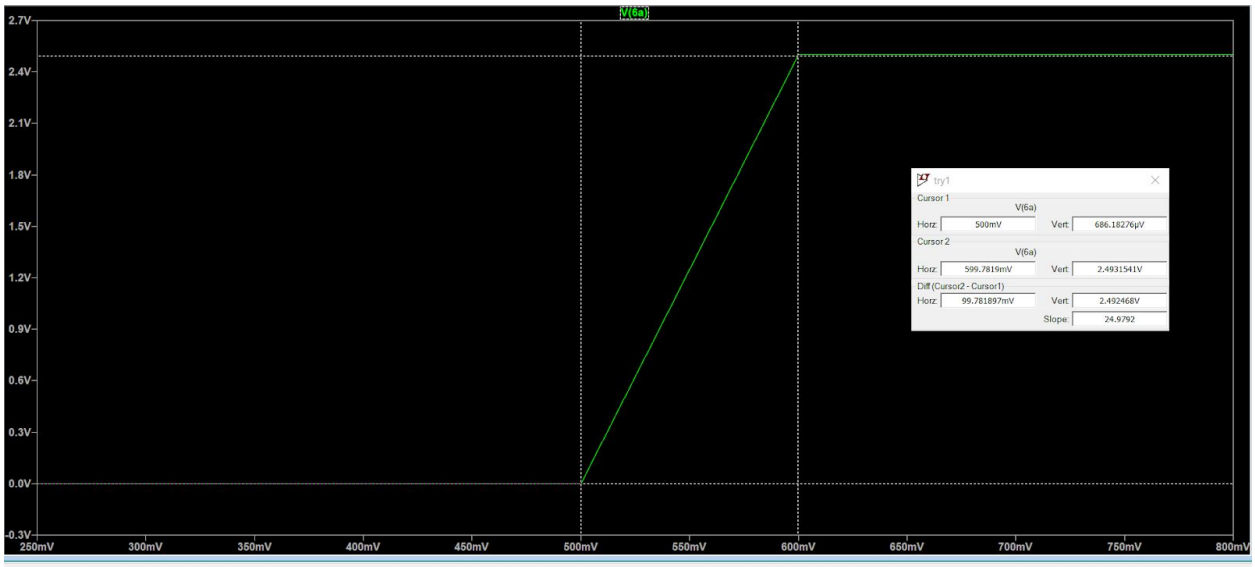


Figure 6.7- Plot to Calculate ICMR

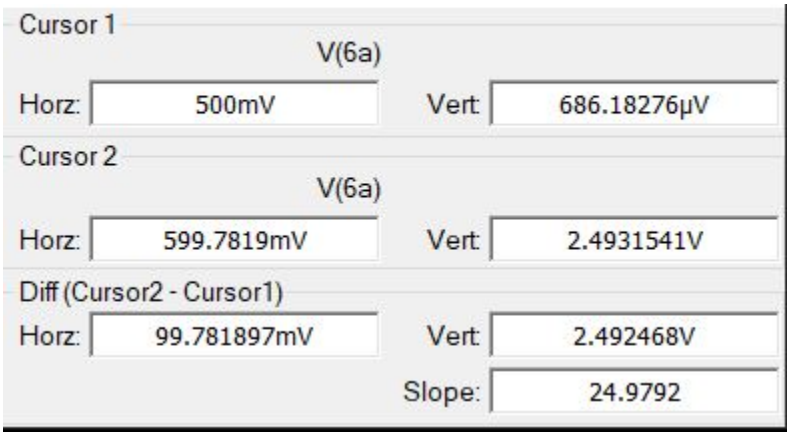


Figure 6.8- Pop up window to calculate ICMR

Input offset (changed circuit rails between Vdd/2 and -Vdd/2)

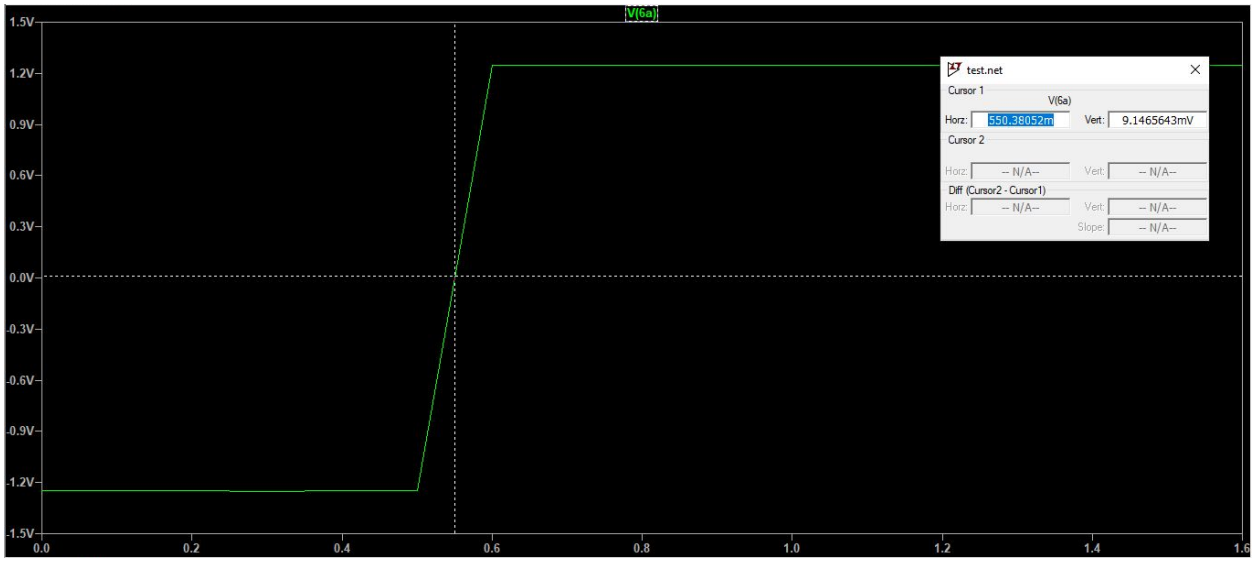


Figure 6.9- Plot for calculating input offset

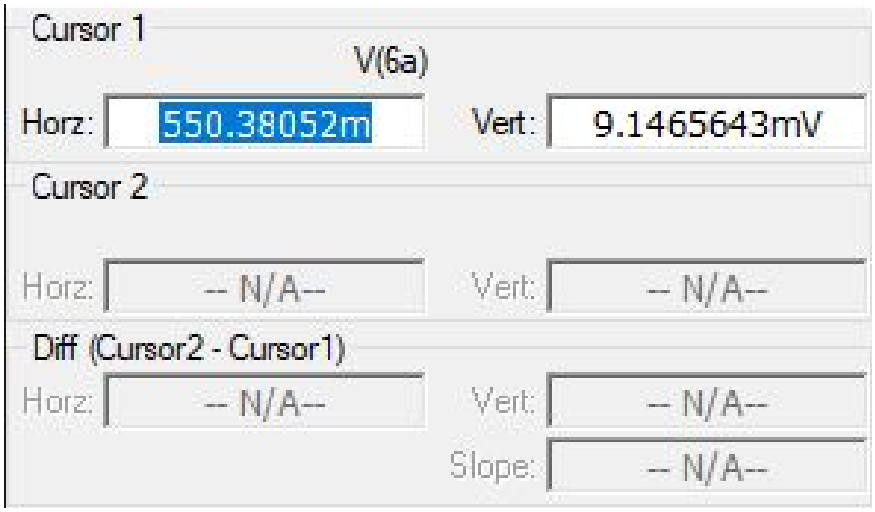


Figure 6.10- Pop up window to calculate input offset

Output Swing

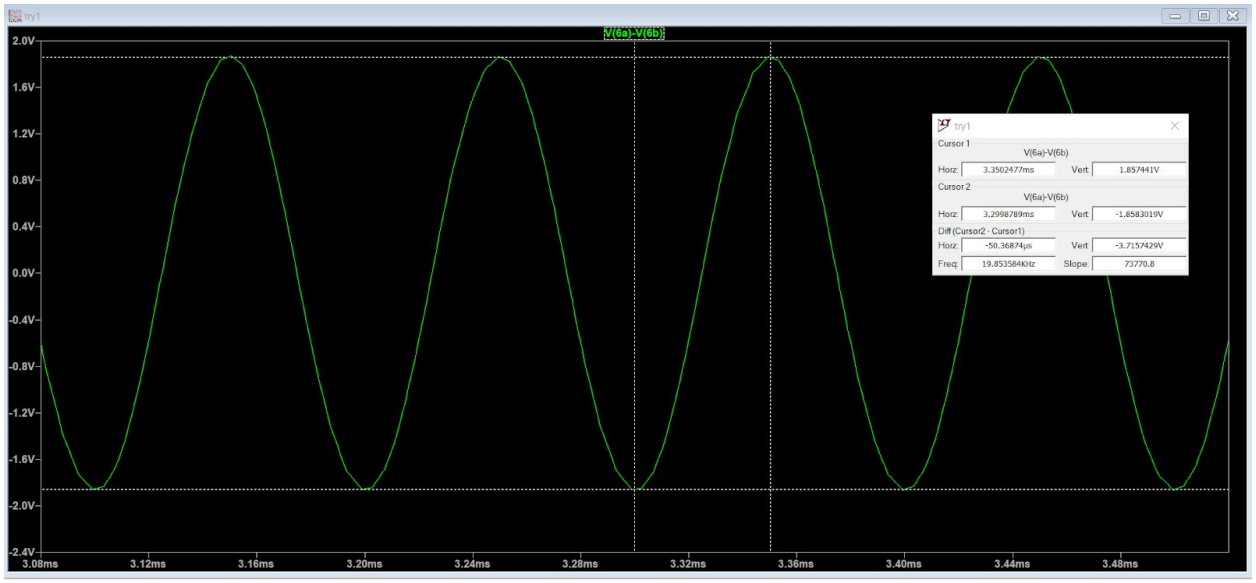


Figure 6.11- Plot for calculating Output Swing

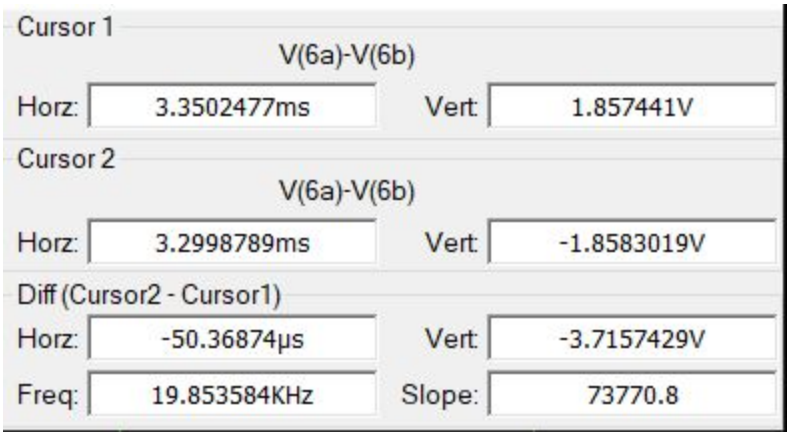


Figure 6.12- Pop up window to calculate Output Swing

DC Offset

```
V(6a):      1.79337      voltage
V(6b):      1.79337      voltage
```

Figure 6.13- DC output offset

Temperature Sensitivity

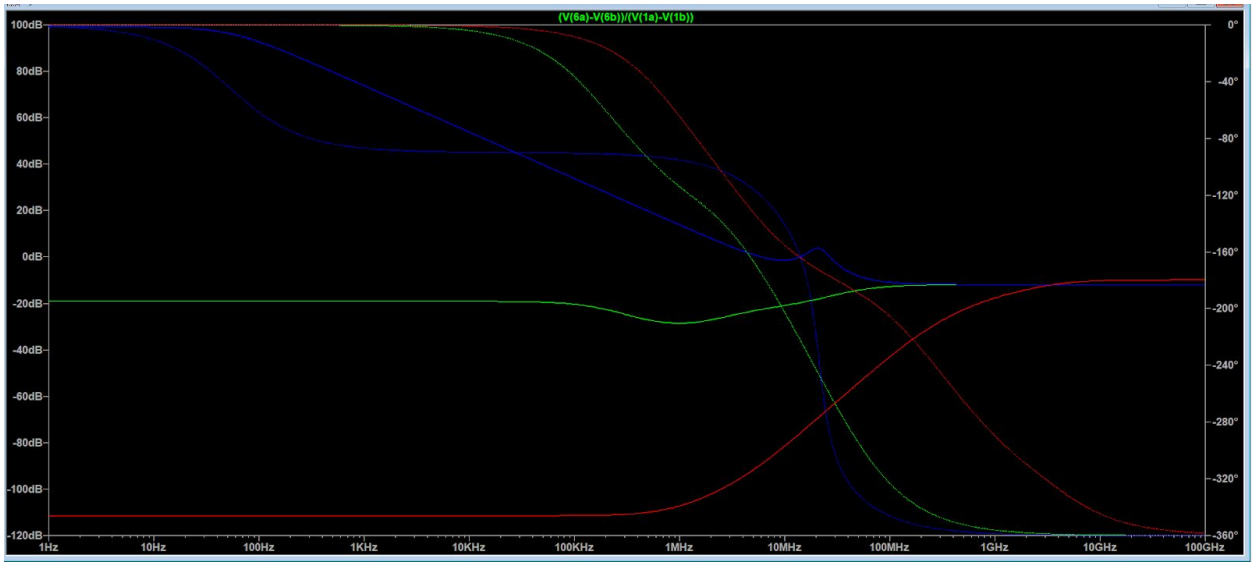


Figure 6.14- Plot to check Temperature Sensitivity

Power Consumption Calculation

Power consumed (P) = V_{DD} * I_d

= 0.6uA* 2.5V

= 1.5 uW

7 Conclusion

Parameter	**Obtained Value**	**Specified Value**
Open Loop Gain	99.14 dB	≥100 dB
Slew rate	0.1 V/us	≥100 V/us
UGB	6.02 MHz	≥60 MHz
Load capacitance C_L	0.1fF	≤1 pF
Current mirror ratios	*Refer to Table 5.2*	≤20
Power dissipation	1.5uW	≤1 uW
Reference Current	58.2nA	Single Ideal Current Source of an arbitrary value, with positive node tied to V_{DD} or negative node tied to ground
Phase Margin	59.09 degrees	50 to 60 degrees
Input offset	0.56V	-

Table 7.1- Comparison between required specifications and obtained specifications

8 Problems faced during the design

The design demanded that all the MOSFETs used must lie in the sub-threshold region. This put a restriction on the slope of the voltage transfer characteristic. Since the open-loop gain required was high(100dB), it was difficult to design an Op-Amp with the given specifications. All the MOSFETS needed to be biased accordingly and checked for sub threshold region operation. The biasing voltages were very sensitive and needed to be accurately designed. With the w/l of the Current Mirror limited to 20, the biasing circuitry also had to be optimally designed to get the required biasing voltages. In order to achieve the required Open-Loop Gain and Phase Margin, slew rate had to be compromised. Using a cascode topology by itself was observed to limit the voltage headroom available.

9 Innovation in Design

Our design involved MOS operation in the Subthreshold region for minimum power consumption. By using a Telescopic Topology, we have achieved a significant gain advantage. However, operation in the subthreshold imposed a restriction on the gain. Hence, we have added a common source stage acting as a gain booster. Due to this design innovation, the gain boost was enough for allowing MOSFETS of the Telescopic Stage to remain within subthreshold operation boundary while simultaneously providing an excellent voltage headroom at the output node. Simultaneously we have used a non-conventional coupling capacitance configuration (like given below) to improve the phase margin and UGB, however this has a major impact on delay.