**A REPORT ON**
**DIGITAL ASSIGNMENT**

**ANALOG AND DIGITAL VLSI DESIGN**
**EEE F313**

Submitted by


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Submitted in partial fulfilment of the course:
Analog and Digital VLSI Design

Under the Guidance of:
Dr. Anu Gupta


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## Problem Statement

Design a Mod-100 Decimal Counter at 1GHz with load capacitance of 1pF.

## Specifications

| Parameter | Value |
|---|---|
| Core Voltage (VDD) | 1.8 V |
| Length (L) | 180 nm |
| Frequency of Operation (f) | 1 GHz |
| Load capacitor (CL) | 1 pF |

## 1.Schematic

The project aims to design a Mod-100 Decimal Counter with the above-mentioned specifications. This can be achieved by designing two Mod-10 decimal counters and cascading them appropriately as explained in subsequently. In turn, each Mod-10 decimal counter can be designed with the help of Flip Flops. An asynchronous counter model (Ripple Counter) was selected for the purpose of the design. In asynchronous counters, each Flip Flop receives a different clock signal. This reduces the complexity of the design and minimizes the external combinational circuits required. However, due to different clock signals, the delay might increase. For the implementation of the counters, D flip flops have been used.

**Design of a D Flip Flop**

A D Flip Flop was designed at transistor level based on the pass- transistor logic, which focuses on using MOSFETs as switches. The logic levels are transferred between the nodes of the circuit and not through the supply. This reduces the number of transistors and power consumption. However, the difference between a high-level voltage and a low-level voltage reduces at each stage making subsequent transistors in series less saturated than the previous. To restore the voltage value, it is necessary to connect a conventional CMOS gate at the output of the pass transistor series combination. This has been incorporated in our design as shown in Figure 1.1.

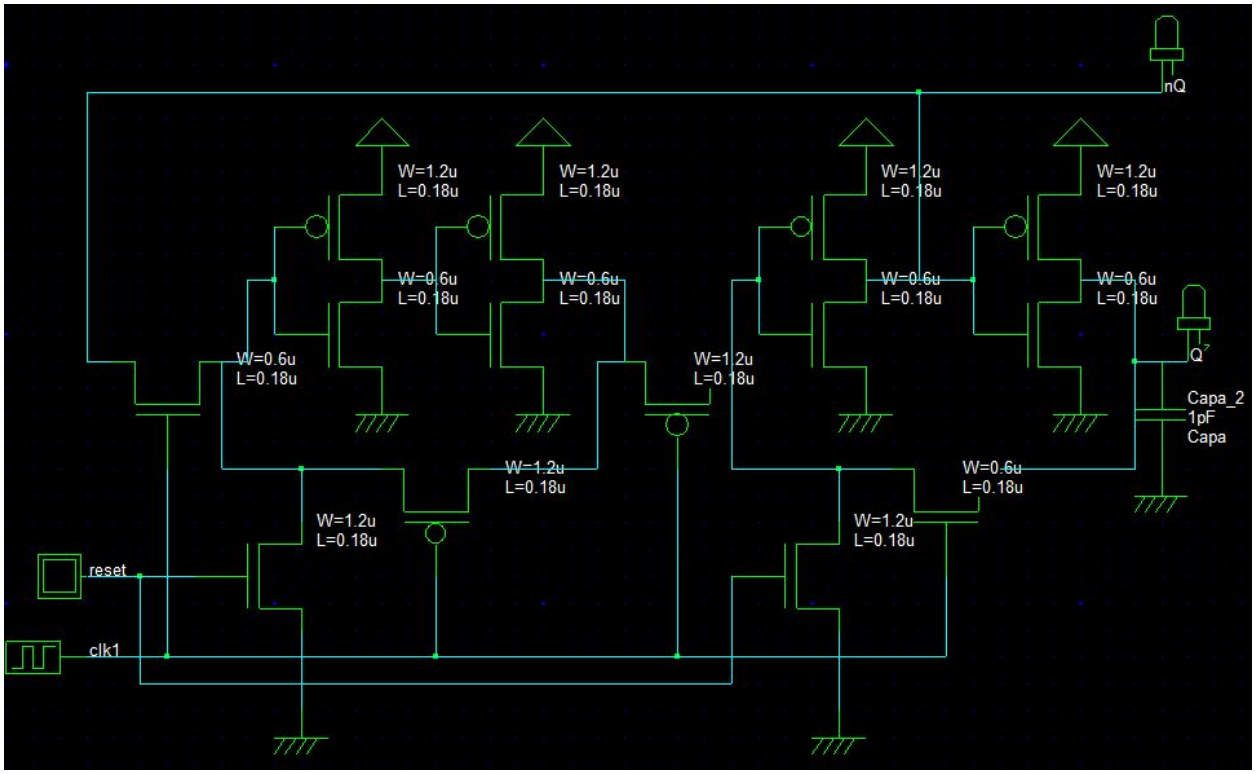


*Fig 1.1 D Flip Flop schematic from pass transistor logic*

**Design of Mod-10 Decimal Counter using D Flip Flops**

The number of Flip Flops used to design an Asynchronous Counter depends on the number of states. The maximum number of states that can be achieved using an asynchronous counter with n flip flops is 2^n. Consequently, the minimum number of flip flops needed for a mod-10 decimal counter is 4.

The four D Flip Flops are connected such that the output(Q) of one flip flop serves as a clock for the next. The block-level schematic for the design is as follows. The output which can be seen in the 7 segment display goes from 0 to 9 and resets back to 0. The reset signal can be used to start and restart the counter from 0.

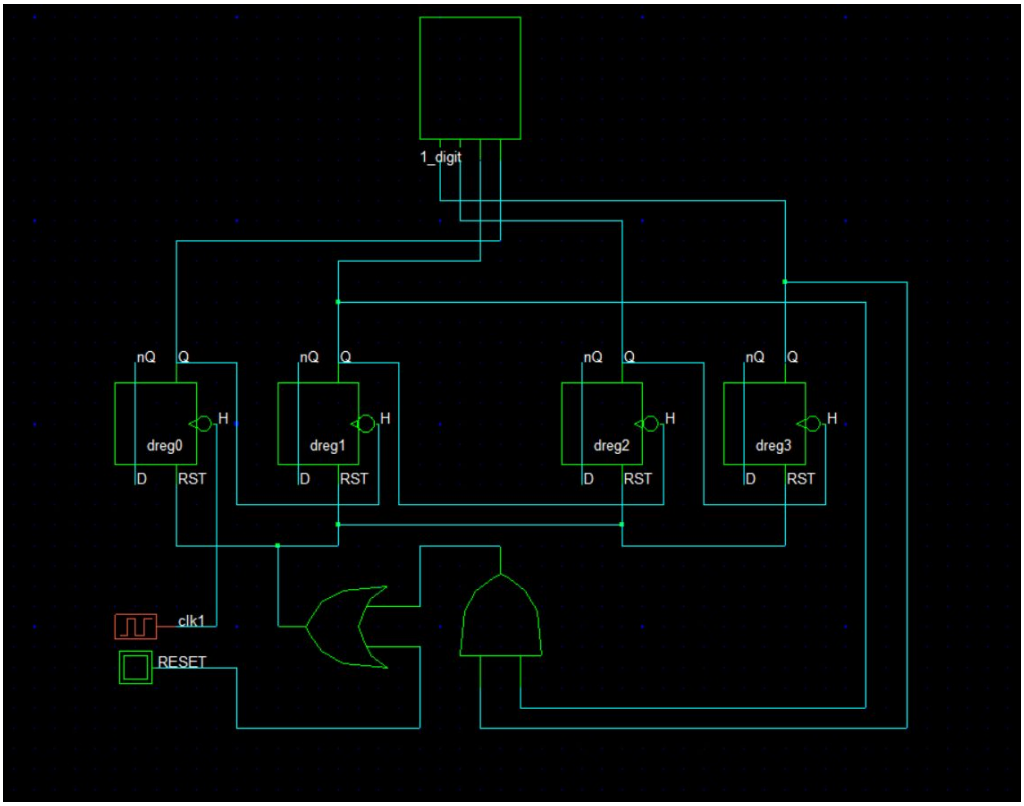


*Fig 1.2 Block level schematic of mod-10 decimal counter*

**Design of Mod-100 decimal counter from Mod-10 decimal counter**

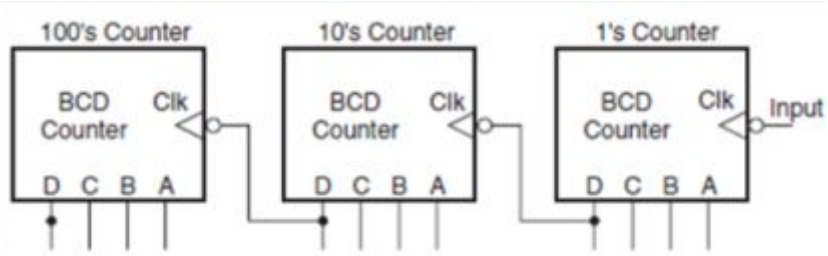


*Fig 1.3 Cascading of BCD counters*

A Mod-100 decimal counter is derived from two Mod-10 decimal counters cascaded as shown in the schematic below.

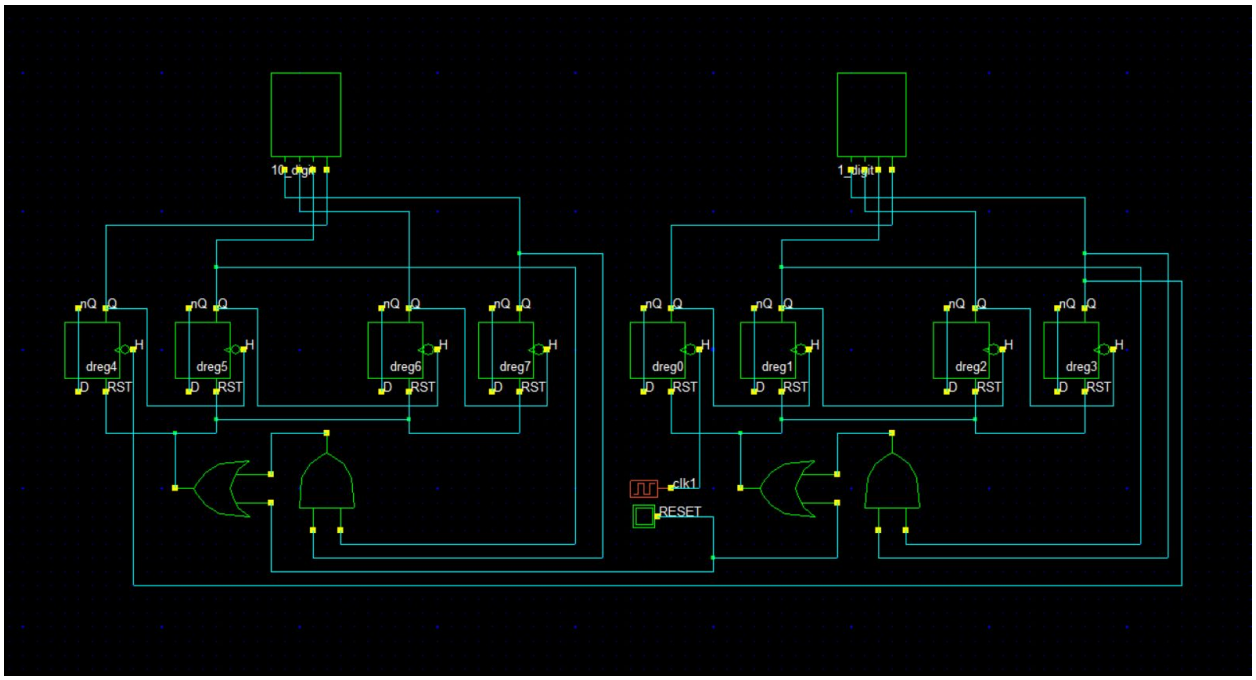


*Fig 1.4 Block level schematic of mod-100 decimal counter*

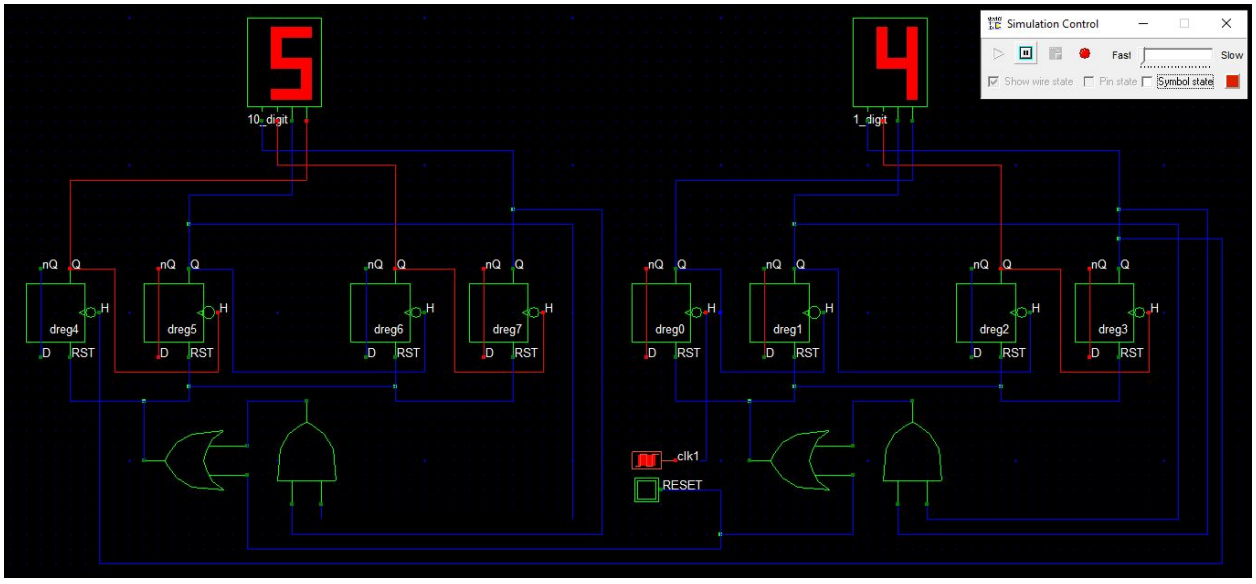


*Fig 1.5 Snapshot from the instant when the counter is at 54*

## 2. Layout

The layout of a D flip flop which gives a frequency half of the clock frequency, acting as a frequency divider. The layout is based on the schematic shown in Fig 1.1.

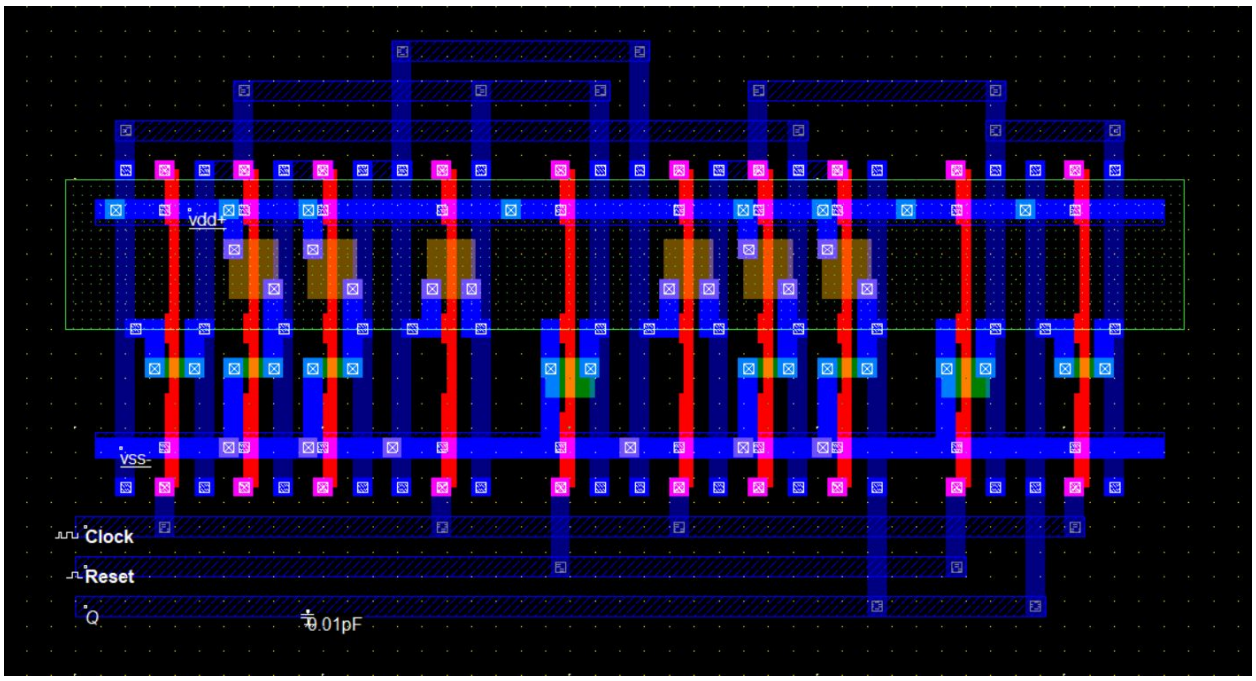


*Fig 2.1 D Flip-flop layout using pass transistor logic*

Total eight such D flip flops are generated to give the desired Mod-100 Decimal Counter. In the figure below, each level represents cascading of two D-flip flops. The bottom two levels along with the AND and OR gates to the left constitute one decade counter (notice that logical effort has been taken care of in AND and OR gates). Similarly, the top two levels constitute another decade counter cascaded with the lower one.

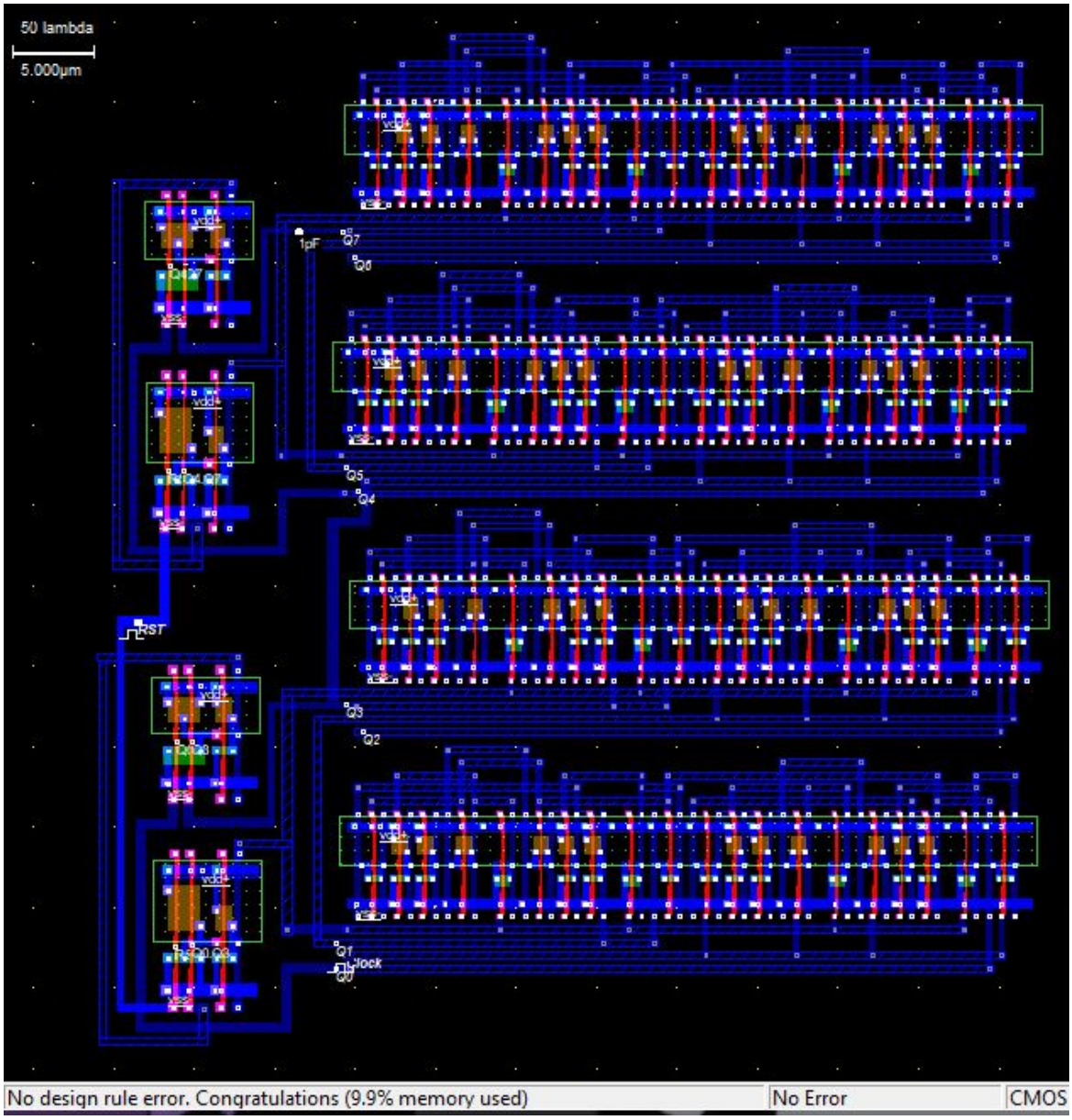


*Fig 2.2 Mod-100 counter based on Fig 1.4 and 2.1*

## 3. Results

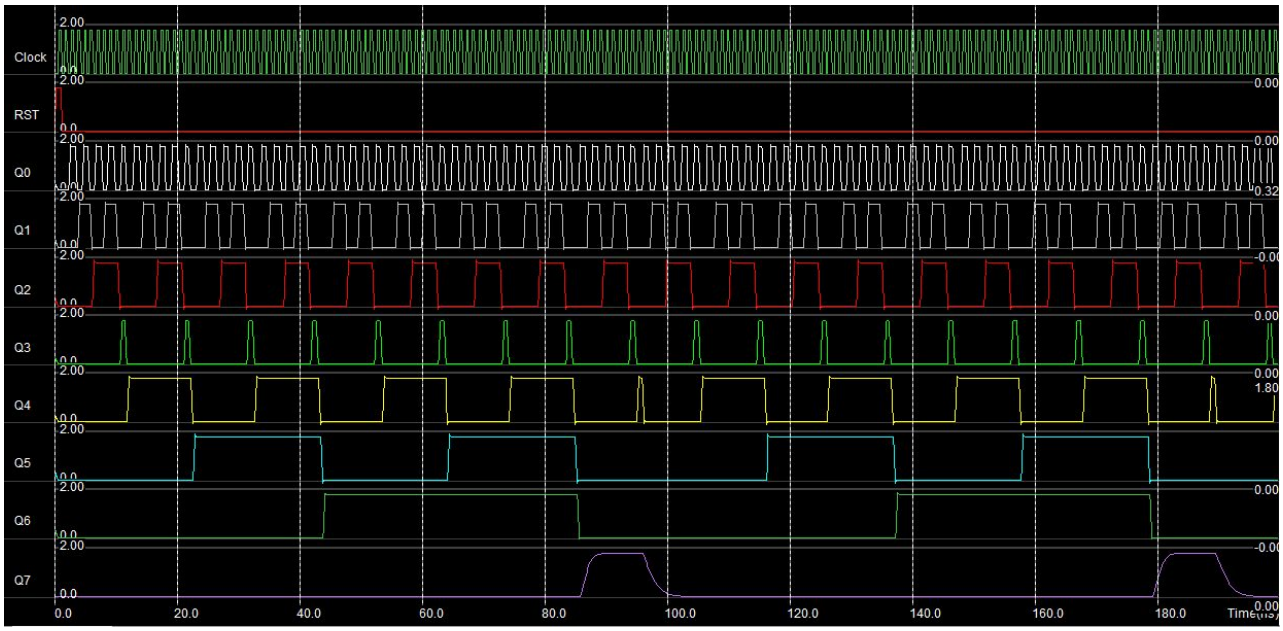


*Fig 3.1 : Output Waveforms at Timescale: 200ns*

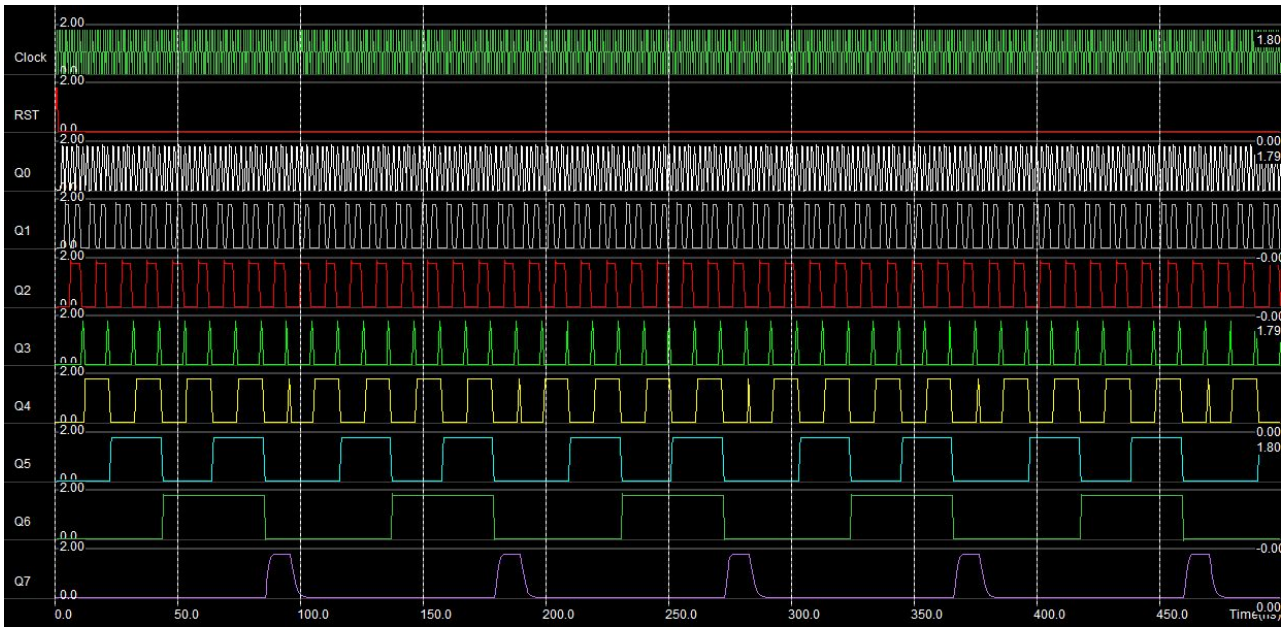


*Fig 3.2 : Output Waveforms at Timescale: 500ns*

**Propagation Delay**

tPLH is defined as the time delay between the V 50% -transition of the falling input voltage and the V 50%-transition of the rising output voltage.

tPHL is the time delay between the V 50%-transition of the rising input voltage and the V 50% -transition of the falling output voltage [3]. The average propagation delay is calculated by taking the average of tpLH and tpHL.

$$tp = (tPLH + tPHL)/2$$

The propagation delays between each consecutive output signal are calculated below.

1) **Propagation delay between Q0 and Clock signal**

   tp = (240 + 260)/2 ps

   = 250 ps

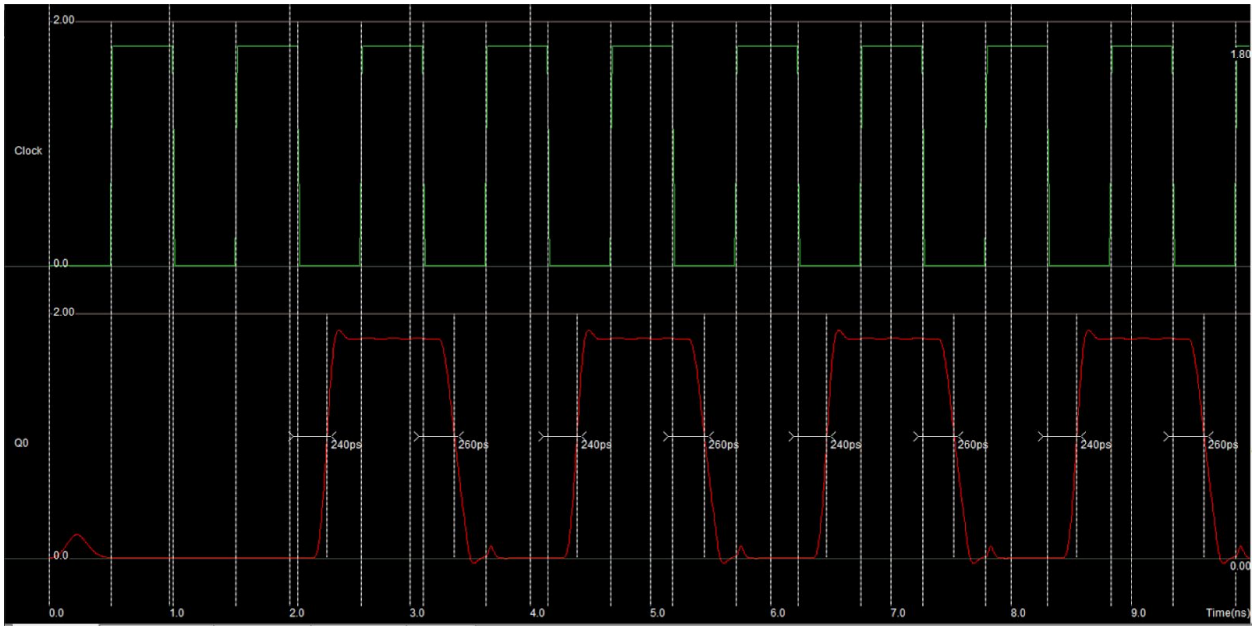


*Fig 3.3.1: Delay figures for Q0 and clk*

2) **Propagation delay between Q1 and Q0 signals**

   tp = (250 + 275)/2 ps

   = 262.5 ps

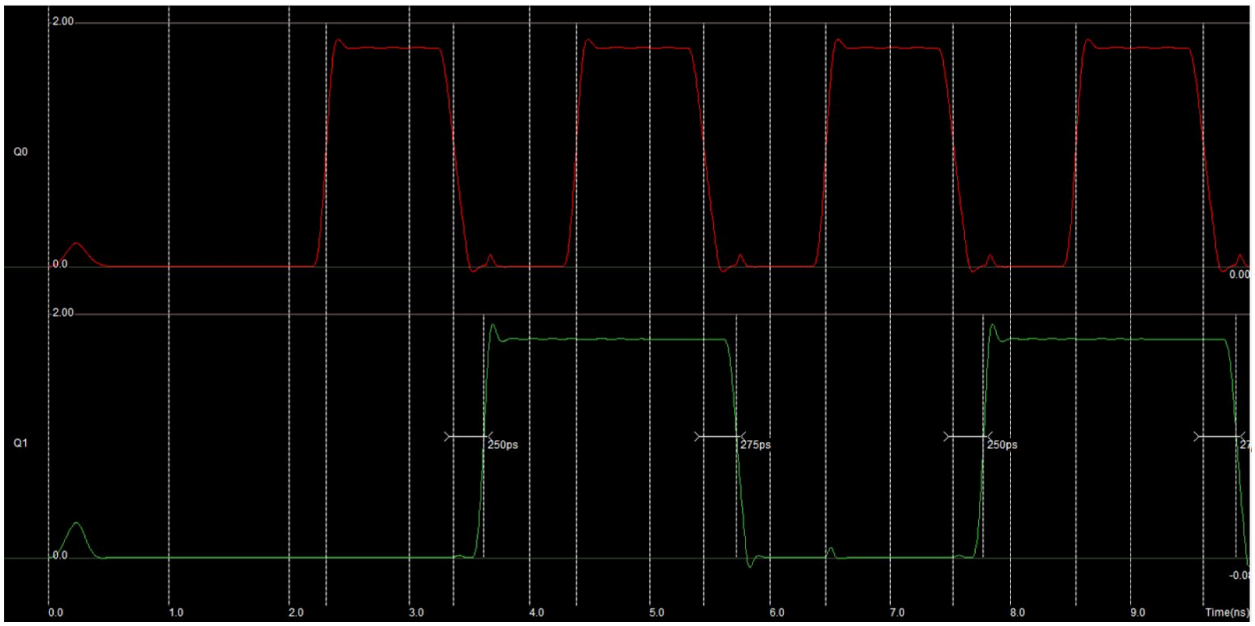


*Fig 3.3.2 : Delay figures for Q1 and Q0*

**3) Propagation delay between Q2 and Q1 signals**

tp = (240 + 245)/2 ps

= 242.5 ps

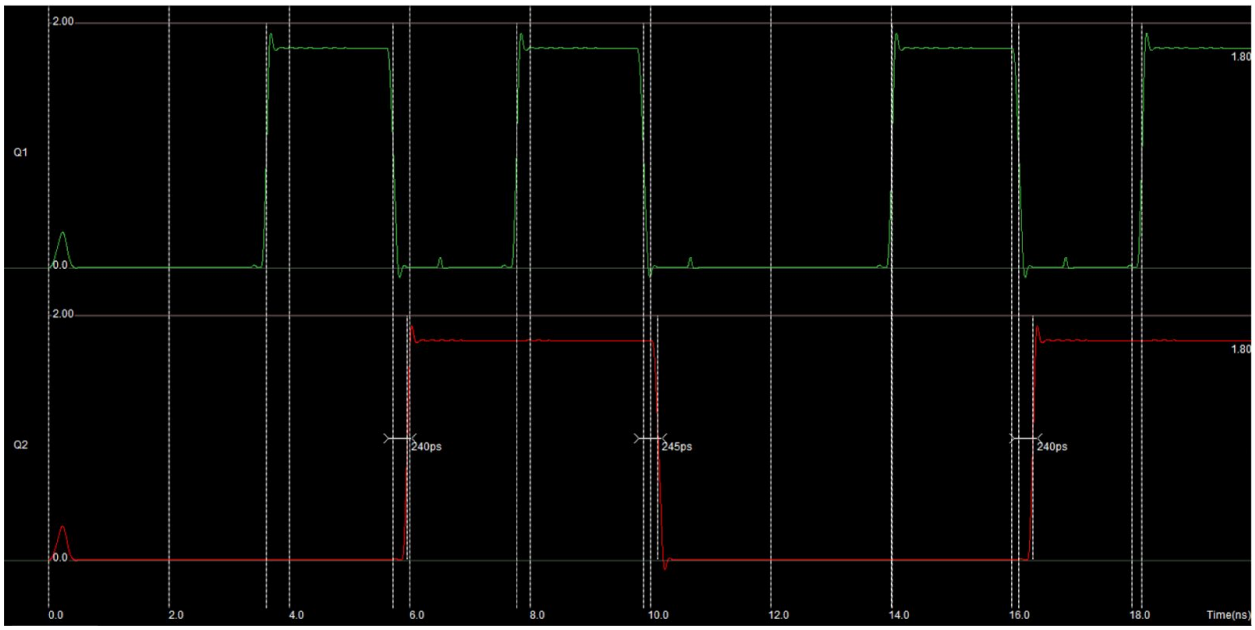


*Fig 3.3.3 : Delay figures for Q1 and Q2*

4) **Propagation delay between Q3 and Q2 signals (falling edge due to reset)**
tp = 255 ps

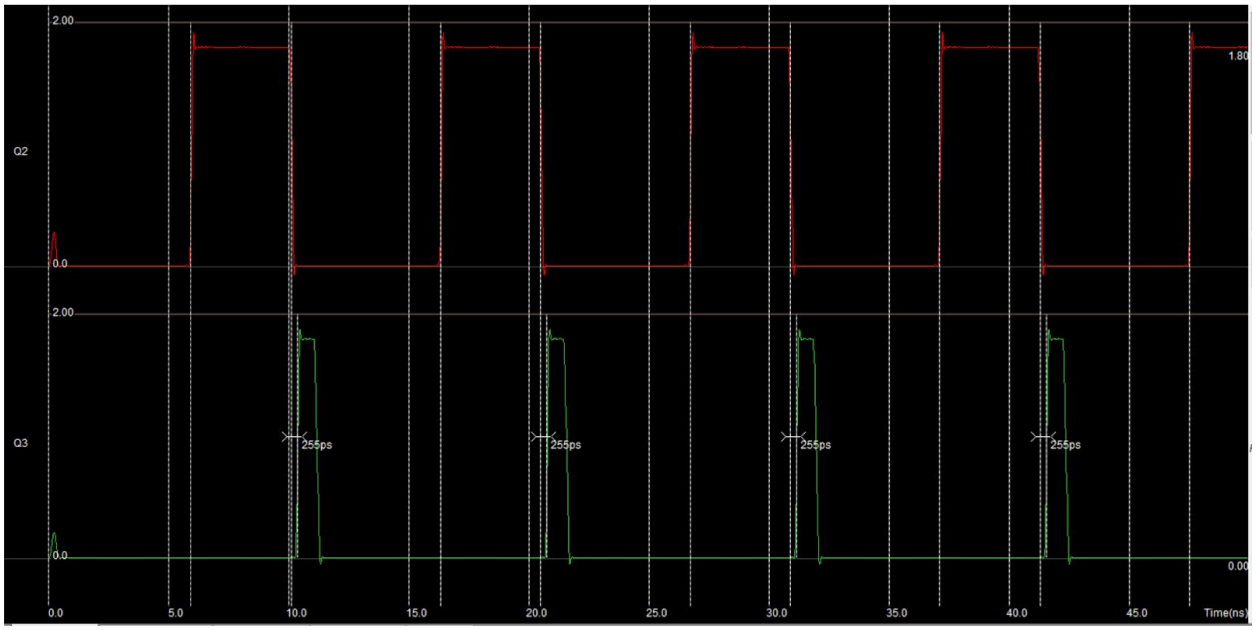


*Fig 3.3.4: Delay figures for Q2 and Q3*

5) **Propagation delay between Q4 and Q3 signals**
tp = (265 + 295)/2 ps
= 280 ps

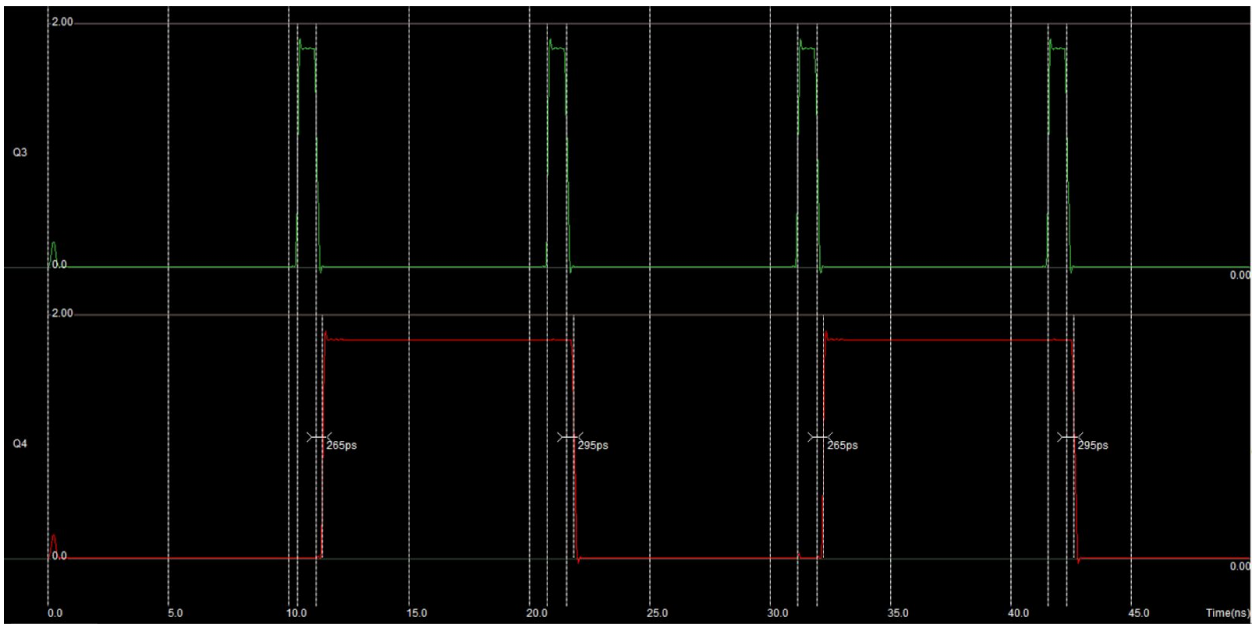


*Fig 3.3.5: Delay figures for Q3 and Q4*

6) **Propagation delay between Q5 and Q4 signals**

tp = (250 + 275)/2 ps

= 262.5 ps

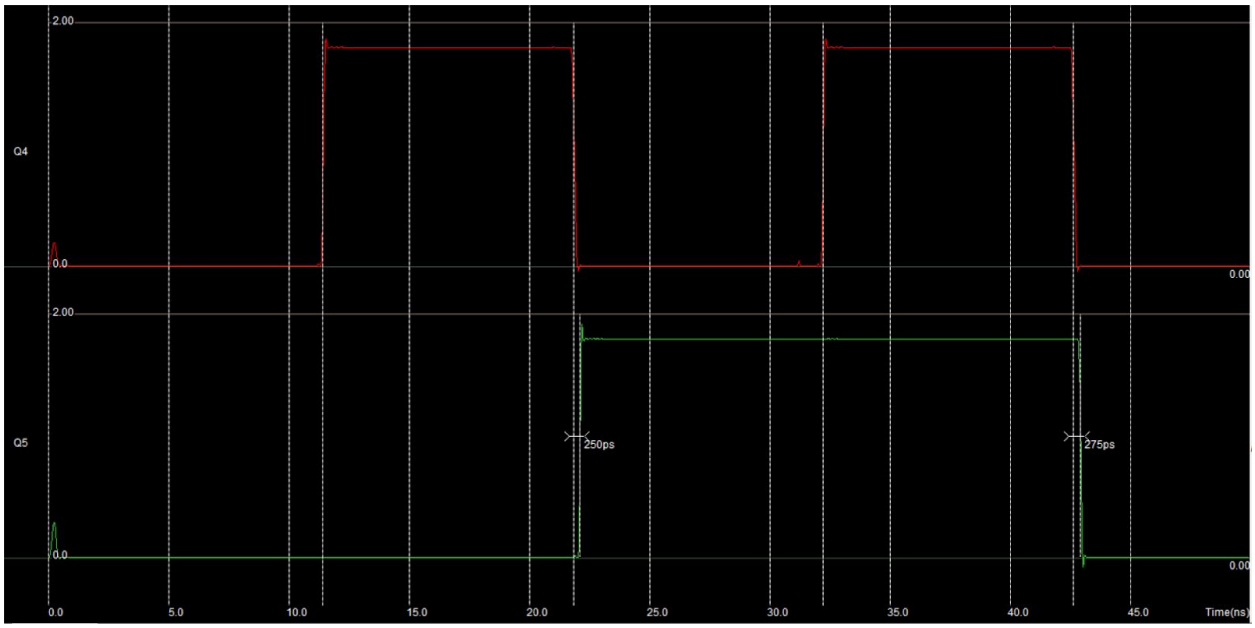


*Fig 3.3.6: Delay figures for Q4 and Q5*

7) **Propagation delay between Q6 and Q5 signals**

tp = (240 + 245)/2 ps

= 242.5 ps

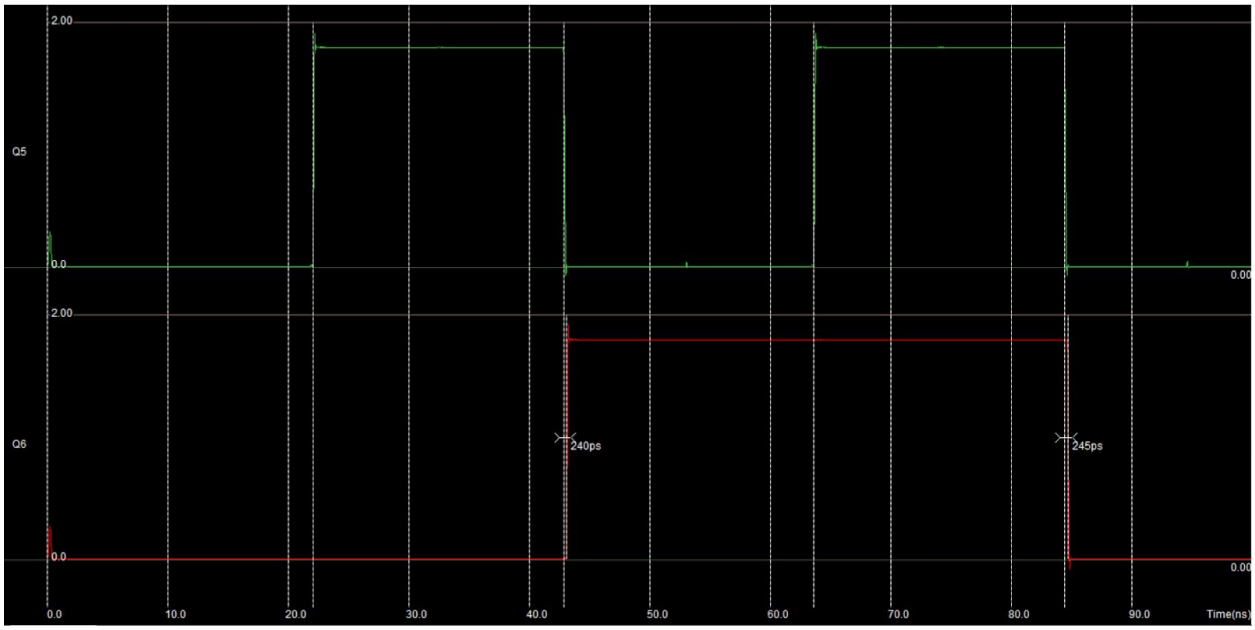


*Fig3.3.7: Delay figures for Q5 and Q6*

8) **Propagation delay between Q7 and Q6 (falling edge due to reset)**
tp = 370 ps

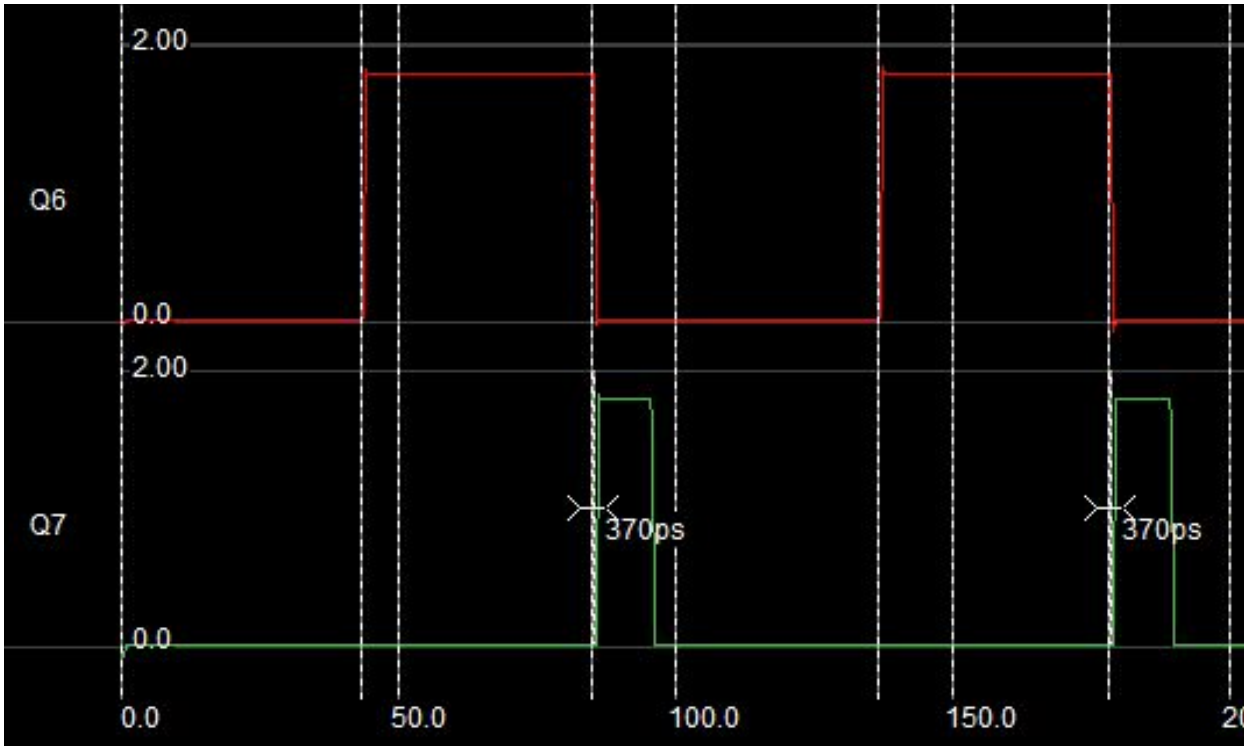


*Fig 3.3.8 : Delay figures for Q6 and Q7*

**Power Consumption**
The average power consumption for the circuit which can be obtained from the simulation is approximately 1.554 mW.

## 4. W/L Table for the Design

W for inverter NMOS was set to a minimum possible value of 0.6 um to reduce power consumption and transistor sizes for all transistors involved. The difference in delay was observed by increasing W for inverter NMOS on the implementation of the D Flip flop block. The difference in values noted for the delay was minimal (i.e., in the range of 5-15 ps) while the power consumption and area were drastically increased as a percentage of the previous values. Furthermore, since the design contains 136 transistors, it was decided to prioritize power consumption and area than delay so the W for inverter NMOS was finalized to be 0.6 um. The best possible choice of W/L of the pass transistors was taken [1][4] and the same for inverters and external gates was decided based on logical effort model of 2:1 inverter, 2:2:2:2 and 4:4:1:1 for NAND (used to make AND) and NOR (used to make OR) respectively (a:b:c:d denotes the relative aspect ratios of the transistors in the order from Vdd to ground).

**D Flip Flop:**

| Transistor | W Value | L Value | W/L Value |
|---|---|---|---|
| NMOS (Pass) | 1.2 um<br>0.6 um | 0.18 um | 6.667<br>3.333 |
| NMOS (Inverter) | 0.6 um | 0.18 um | 3.333 |
| PMOS (Pass) | 1.2 um | 0.18 um | 6.667 |
| PMOS (Inverter) | 1.2 um | 0.18 um | 6.667 |

**External gates:**

| | | | |
|---|---|---|---|
| NMOS (AND) | 1.2 um | 0.18 um | 6.667 |
| NMOS (OR) | 0.6 um | 0.18 um | 3.333 |
| PMOS (AND) | 1.2 um | 0.18 um | 6.667 |
| PMOS (OR) | 2.4 um | 0.18 um | 13.333 |

## 5. Conclusion

| Parameter | Obtained Value | Specified Value |
|---|---|---|
| Overall Propagation delay<br>(As per worst-case input combination, i.e., wrt Q7 and clk) | 2.165 ns | - |
| Power consumption | 1.554 mW | minimum |
| Area | 3705.6 um^2 | minimum |

## 6. Problems faced during Design

The design process began by breaking down the given problem into smaller problems which could be combined to solve the original problem. The design of Mod-100 decimal counter was thus reduced to a design of Mod-10 decimal counter.

The next task was to decide the type of counter to be implemented i.e. Synchronous or Asynchronous. While synchronous counters give better reliability in terms of delays and errors,

asynchronous counters reduce the external logic circuitry required. Considering the complexity of the entire design, it was decided to go ahead with an asynchronous counter.

Further, the design of the Mod-10 counter was reduced to the design of a single D flip flop. There were several ways to implement this including use of NAND gates alone, use of pass-transistor logic and transmission gates, use of transmission gates in a master-slave configuration, etc. and it was a major challenge to finalize the implementation.

The design had to be optimized in terms of delay, power consumption and area while maintaining the functionality after cascading, taking care of parasitic and load capacitance as well. This was a crucial step involving multiple trials. After several attempts of making flip flops and cascading, the functionality and the parameters subject to optimization were compared.

It was found that Pass-Transistor logic worked the best among these and was used for the further implementations. A mod-10 decimal counter was designed by cascading 4 such D flip flops and adding the required combinational logic. This was then cascaded to give a mod-100 decimal counter.

Additionally, the trade-off between circuit delay and area+power was a challenging decision and finally, the latter was given more importance than the former.

## 7. Innovation & Optimization

**Power Consumption:**
In order to decrease the power consumption, our design utilizes pass transistor logic. Since the pass transistors are not directly connected to the supply, the number of devices that draw current directly from the VDD supply is reduced, consequently reducing the power consumed.
**Propagation Delay:**
The propagation delays of the gates have been optimized by calculating the optimal W/L values using the Method of Logical Effort. Circuit area reduction by stacking instead of a completely spread out layout with components placed side-by-side also reduces delay by a good margin.
**Circuit Area:**
Pass Transistor Logic generally requires fewer transistors than CMOS logic to implement the same function. Moreover, the layout has been drawn opting minimum dimensions by stacking levels on top of each other, keeping in mind the spacings as permitted by the design rules, wherever possible. This has significantly diminished the circuit area as compared to a spread-out layout as mentioned before.

**References**
[1] H. Kumar, A. Kumar, A. Islam, “Comparative Analysis of D Flip-Flops in Terms of Delay and its Variability”. IEEE, 2015.
[2] M. Morris Mano, "Digital Design". Prentice-Hall, Inc.

[3] S. M. Kang, and Y. Leblebici, “CMOS Digital Integrated Circuits Analysis and Design”. McGraw-Hill, 2003.

[4] T. Thangam, P. Jeya Priyanka, V. Sangeetha, “Performance Improved Low Power D-Flip Flop with Pass Transistor Design and its Comparative Study”. IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 4, April 2015.