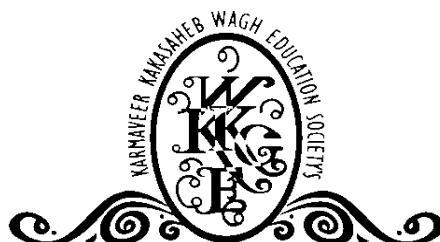


A
PROJECT REPORT
ON
**“IMPLEMENTATION OF IVR SYSTEM FOR COLLEGE
ASSISTANCE”**

SUBMITTED BY

KARTIKEY SUNIL BANDRE	B150133005
ANUJ RAJESH KABRA	B150133028
ATHARVAA HEMANT SAVALE	B150133057

**Under the Guidance of
Prof. R.V. CHOTHE**



**DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION
ENGINEERING,**

**K. K. WAGH INSTITUTE OF ENGINEERING EDUCATION &
RESEARCH, NASHIK.**

SAVITRIBAI PHULE PUNE UNIVERSITY

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Dissertation Approval Sheet

This is to certify that the project work titled “IMPLEMENTATION OF IVR SYSTEM FOR COLLEGE ASSISTANCE”, has been submitted in partial fulfillment of the Bachelor’s degree in Electronics and Telecommunication during the academic year of 2021-2022 by following students:

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This project confirms to the standards laid down by the Savitribai Phule Pune University and has been completed in satisfactory manner as a partial fulfillment for the Bachelor’s degree in Electronics and Telecommunication Engineering.

External Examiner

Internal Guide

Head of Department

Prof. R.V.Chothe

Prof. Dr. D. M. Chandwadkar

Plagiarism Certificate

This is to certify that the project work titled “IMPLEMENTATION OF IVR SYSTEM FOR COLLEGE ASSISTANCE”, is a part of project work carried out by “Kartikey Sunil Bandre, Anuj Rajesh Kabra and Atharvaa Hemant Savale” under the guidance of Prof. R.V.Chothe at K. K. Wagh Institute of Engineering Education and Research, Nashik, in the partial fulfillment of the requirements for Bachelor’s degree in Electronics and Telecommunication Engineering.

To the best of our knowledge, the work included in this report is an original work carried out by us independently. The percentage of Uniqueness is 90.8%. The results of the project work in part or whole have not been submitted to any other Institute/University for the award of any degree.

1. Kartikey Sunil Bandre
2. Anuj Rajesh Kabra
3. Atharvaa Hemant Savale

Name & Signature of the student

ACKNOWLEDGEMENT

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1. Kartikey Sunil Bandre
2. Anuj Rajesh Kabra
3. Atharvaa Hemant Savale

Name & Signature of the student

ABSTRACT

If you ever made calls to all those toll free numbers that starts with 1800(India) or 800 (for USA) and so on... ? What you hear ? A very pleasant voice, "Welcome to ..." Then you are prompted to press some key on your phone. Do you realize, you are not talking to a lady, but to a machine ? Now you have realized that intelligent lady is called IVRS. Interactive Voice Response (IVR) system is widely used now a days. Interactive Voice Response (IVR) systems allow callers to interact with the communications system over the telephone. IVR is used to enable the caller to retrieve information from a database, enter information into a database, or both. IVR systems allow the user to efficiently exchange information, reducing clerical processing. An IVR system talks to callers following a recorded script. It prompts a response to the caller and asks him to respond either verbally or by pressing a touchtone key, and supplies the caller with information based on responses made.

IVR system should store responses made by callers. Should be able to provide different responses to callers based on time of day called. In India where illiteracy and poverty are two major problems, this system can be used wherever there is a need to connect people with IT. This system provides the telephonic communication in the most commonly used languages i.e. Hindi, English and local languages. In addition to this, the software has a very easy to use. This solution provides a convenient approach to speak dynamic data like numerical digits in the language that user prefers. This system makes use of very less infrastructure in order to provide the services affordable by our rural community.

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Abbreviations

IVR- Interactive voice response

DTMF- Dual Tone Multi-Frequency

GSM- Global System for Mobile communication

LCD- Liquid Crystal display

CSR - Customer Service Representatives

IAAS- Infrastructure as a service

PAAS- Platform as a service

SAAS- Software as a service

EIG- Enterprise Integration Group

TTS- Text-To-Speech

USB- Universal Serial Bus

RAM- Random Access Memory

ROM- Read Only Memory

CMOS- Complementary Metal Oxide Semiconductor

UART- Universal Asynchronous Receiver Transmitter

IC- Integrated Circuit

GPRS- General Packet Radio Service

TTL- Transistor Transistor Logic

SIM- Subscriber Identity Module Card

USIM- Universal Subscriber Identity Module

PCB- Printed Circuit Boards

SMS- Short Message Service

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Interactive Voice Response System is an automated system which interacts with the users through voice. IVR Systems provide an efficient way for Institutions, Health Care, Telecommunication, Banking and other sectors which provide customer service on 24/7 basis. As human useful resource isn't always value-powerful and non-to be had always, this device compensates for the paintings to a maximum extent. An IVR System accepts combination of telephone input and touch-tone keypad selection and provides appropriate responses in the form of voice, fax, callback, e-mail, SMS etc. This system mainly used to provide the users access to the database for particular information in the organization. For example, banks and credit card companies use IVR systems so that their customers can receive up-to-date account information instantly and easily without speaking directly to a person.[1] The technologies used are DTMF (Dual Tone Multi-Frequency) Decoding and Speech recognition for getting the user's response in reply to the voice prompt. DTMF tones are generated through key press at the client's side. Two primary types of speech reputation are used in IVR are directed dialogues and Natural language dialogues. The voice may be pre-recorded or system-generated using a Text-to-Speech engine. [2]

IVR is used to allow the caller to retrieve information from a database, input information into a database, or both. IVR structures permit the person to professionally alternate facts, reducing clerical processing. IVRS provides a voice response to students and guide them to the information they require. The students can call up on the toll-free number and get any information regarding college admission by simply pressing certain button on his mobile as per the guidance of voice fed into computer. An IVRS machine talks to callers following a recorded draft. It prompts a response to the caller and asks him to take action by pressing a touchtone key, and supplies the caller with information based on responses made. [3]

Similarly, the proposed system can be also used at various Educational Institutions, by providing the registration number and password of a student, the parent can get details as the name of the student, aggregate of marks, other activities instantly through a SMS. [3]

1.2 NEED OF PROJECT

There are many successful examples where businesses have improved their operations and increased customer satisfaction through the implementation of an IVR system. An IVR system provides users with round-the-clock access to variables rather than static information. The use of a well-designed IVR system can help in reducing the number of calls that are to be answered by the Customer Service Representatives (CSR). At the same time, it increases customer satisfaction, as the customers are not restricted to the hour of operation of the business if they require routine information. They can call in 24 hours a day, seven days a week. [4]

A number of organizations today depend heavily on the IVR system for the successful operation of their business. Some of these are airline companies, banks and insurance companies, courier agencies, educational institutions, etc. Some of the traditional applications of the IVR are providing account balances, checking status of a package or claim, requesting or providing information, or allowing users to register for various activities. New and innovative applications are constantly being developed to streamline business processes. However, the selection of the right IVR system is important. It is essential to have caller-friendly and easy-to-understand voice scripts, prompts, and logical paths between responses. Only after a careful selection and planning of an IVR system will the expected benefits be realized.[5] It is estimated that 80% of the costs associated with a call-center are related to employees. Given the high personnel costs it is essential that an optimal number of call center staff be maintained and their time optimally utilized. However, even with a good IVR system, it is usually assumed that the caller will listen to all the choices before making a selection. This, however, is not always the case. Many callers do not wait to listen to all the choices. They simply press '0' to talk to a live person. This is based on the assumption the pressing '0' will in fact provide them this opportunity. [5]

Due to this tendency in the user behavior many IVR scripts are modified to give an option other than pressing '0' to users to speak to all call-center agents. Some others require users to press '0' twice before connecting them to a live operator. Research conducted by some business has also indicated that just switching the order of choices can make a big difference in encouraging or discouraging users from choosing certain options. There are standard industry guidelines that assist in designing a good IVR avoiding some of the pitfalls. However these standard guidelines have to be customized to suit the particular needs of the business. [6]

1.3 TARGET COMMUNITY OF PROJECT

This project is helpful for the college admission department to assist students during the admission process. The college will be able to gather data of students, and assist accordingly.

IVR systems can encompass telephony device, software program packages, a database and an assisting infrastructure.

1.4 OBJECTIVE OF PROJECT

To know the admission details of the college the student should have to approach the college. This may be very time consuming and if the student is living outside the state then it is very time consuming and costly. Interactive Voice Response (IVR) system is widely used now a days. Interactive Voice Response (IVR) systems allow callers to interact with the communications system over the telephone. IVR is used to enable the caller to retrieve information from a database, enter information into a database, or both. IVR systems allow the user to efficiently exchange information, reducing clerical processing. An IVR system talks to callers following a recorded script. It prompts a response to the caller and asks him to respond either verbally or by pressing a touchtone key, and supplies the caller with information based on responses made. IVR system will store responses made by callers in Data Base and it is able to provide different responses to callers based on time of day called.

1.5 GANTT CHART

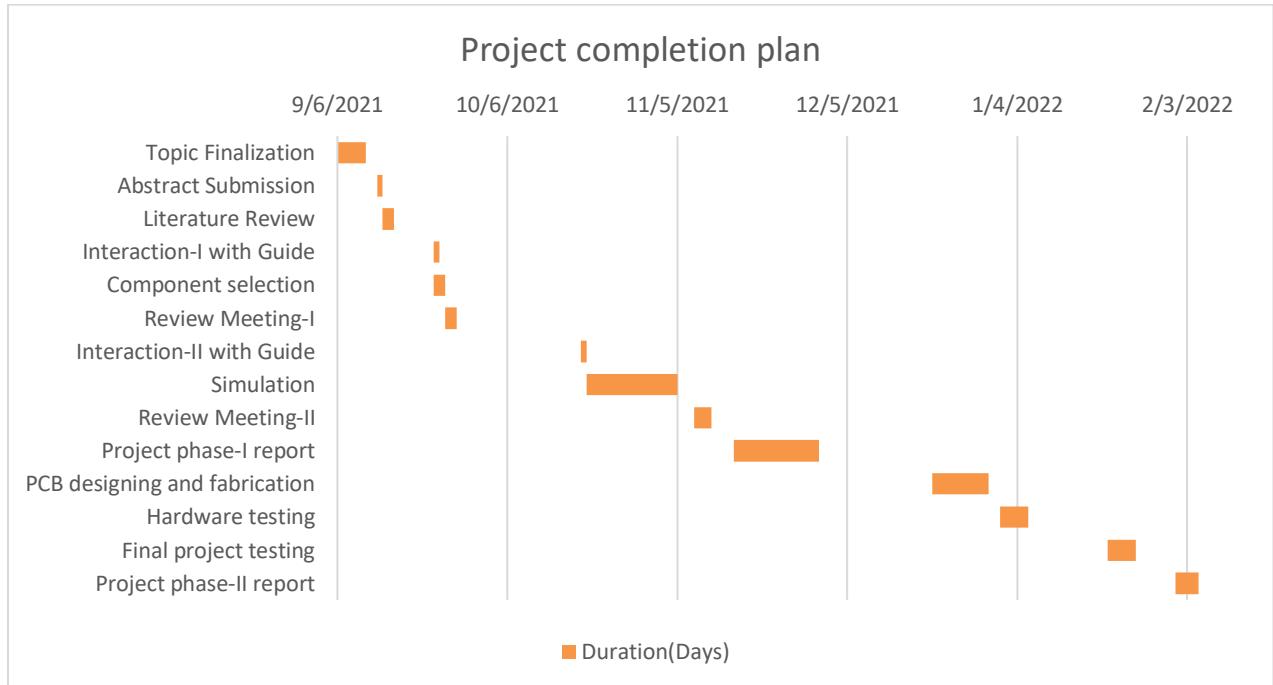


Fig 1.1 Gantt chart of Project completion plan

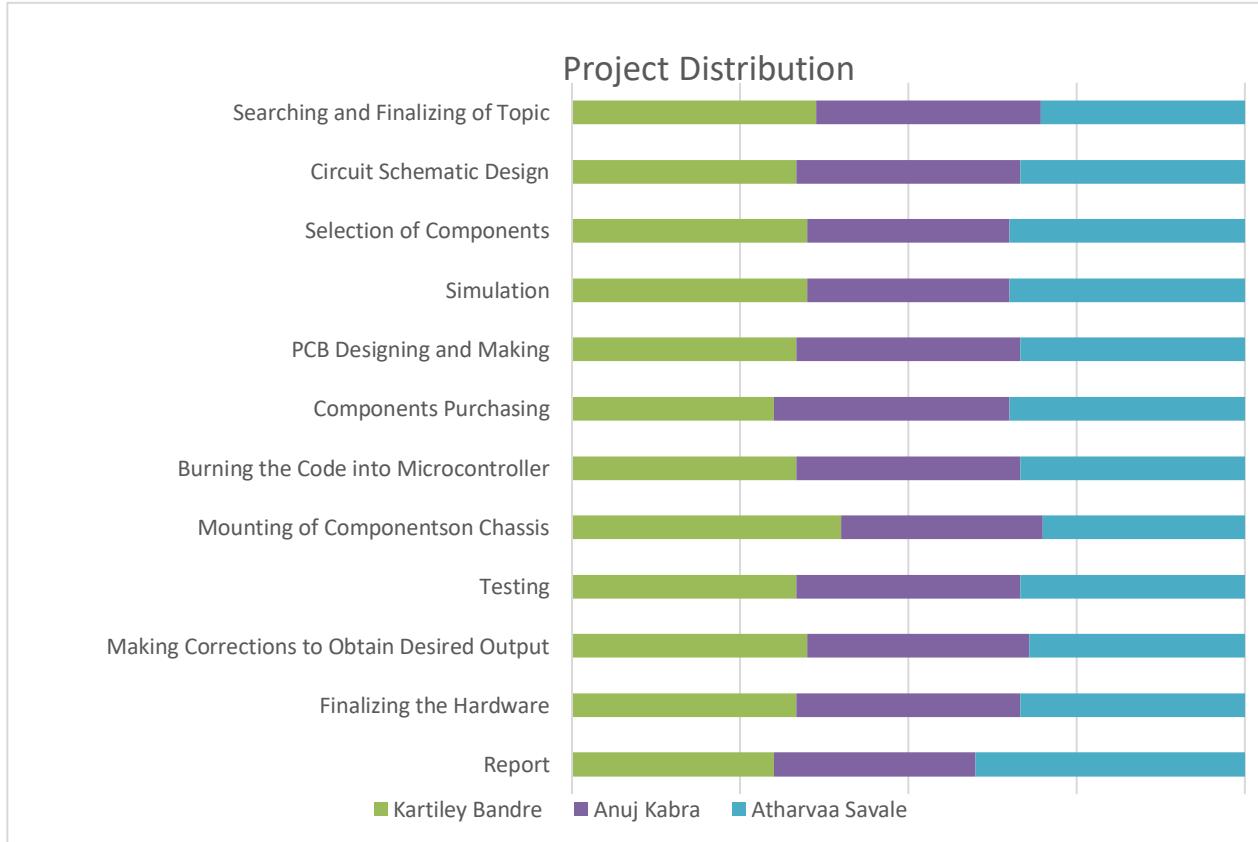


Fig 1.2 Gantt chart of work distribution among the group members

CHAPTER 2

LITERATURE SURVEY

- 1. Ms. Ayesha Mahamadshafi Attar, Ms. ShrutiSudhir Aitavade, Ms. Poonam Arjun Kalkhambkar , Ms. SofiyaRiyaj Nadaf, “ Interactive Voice Response System for College automation” e-ISSN: 2395- 0056 p-ISSN: 2395-0072: -**

For this application is prepared in such a way that they can be easily accessed through computers. In the same way our project's aim is to provide the entire information to the user at the tip of his fingers. Due to this project the traditional manual way of handling the customer queries will be handled in a more technological and automated way. This type of system performs operations similar to that of a human telephone operator. [1]

- 2. N.Chandrika, SK.Masthan, B.Venu madhav, J.Kranthi, P.Vyshnavi “Voice Based Student and College Information through IVRS” e-ISSN: 2395-0056 p-ISSN: 2395-0072:-**

The IVRS based information system has been designed in such a way that it reduces the manpower requirement, makes the interaction as easy and fast as possible. It has countless real world applications that can be used in various environments. [2]

- 3. V. G. Rajendran, S. Jayalalitha, Vemuri Sri Venkata Siva Sai “Smart IVR System Based on GSM for an Educational Institution” IEEE Conference Number – 33344: -**

This system helps the parents to know their son or daughter's performance at regular intervals. They can access the system at any time and also provide proper guidance at the correct time when their ward goes wrong and parents can access student's information [3]

4. A. Chotimongkol, N. Thatphithakkul and P. Prathombutr, "Smart IVR Service Platform," 2012 Annual SRII Global Conference, 2012, pp. 426-434, doi: 10.1109/SRII.2012.53.

The traditional IVR or Interactive Voice Response is a voice interface with a computer over a phone line. To avoid the burden to hold the IVR hardware and software, we introduce the Smart IVR which is organized in the same concept with a cloud computing. It includes an IaaS, a PaaS and a SaaS platform. The designed architecture of the IVR composes of APIs for a developer like a Text-to-Speech API in the PaaS layer. In the SaaS layer, one may build their own IVR dialog in a snap over a Dialog Management module. Unlike other cloud IVRs, the proposed IVR smartly handles the text information with the Dialog Management. It could link a dialog to a text message from various platforms such as RSS, Twitter, Facebook, Google Maps and database. The real case of IVR service innovations have been presented in the show case section and the discussion on Service Innovation is provided. [4]

5. P. S. Devi, D. Das, J. Stephen and V. K. Bhadran, "Web based and voice enabled IVRS for large scale Malayalam speech data collection," 2014 International Conference on Contemporary Computing and Informatics (IC3I), 2014, pp. 1112-1117, doi: 10.1109/IC3I.2014.7019717.

Speech corpora are vital resource in development and evaluation of automatic speech recognition systems, as well as for acoustic phonetic studies. Collecting a huge corpus is not an easy task. The lack of such resources is one of the reasons for the absence of good quality speech recognition systems in Indian languages. Here we have automated such process by developing web based tool for collecting broad band speech data and an IVR system with speech recognition for collecting narrow band speech data. The main features includes the full support for the typical recording, annotation and project administration workflow, easy editing of the speech content, with an advantage of a fully localizable user interface. This paper describes in detail the development of web based speech collection tool and an IVR system which will enable end-to-end building of speech corpus with minimum manual effort. [5]

2.1 Previous Research on IVR

There has not been much academic research done on the use of Interactive Voice Response technology. The most notable study done in this field was Brian Huguenard Ph.D. thesis at Carnegie Mellon University titled "Working memory failure in human -computer interaction: Modeling and testing simultaneous demands for information storage and processing." Various consulting firms and independent IVR vendors have carried out a number of studies on the effective design and implementation of IVR systems. However, these studies have mostly been done in the U.S. The current thesis was conducted in a Canadian context by utilizing a Canadian workers' insurance organization and the findings are not expected to be any different. However, there might be a chance that it might be different. This would provide guidelines for testing the effectiveness of scripts developed in this study by predicting their likeliness of being used by callers. [6]

2.1.1 Huguenard (1993)121

Brian Huguenard's study was related to the design of better human-computer interfaces through the use of a computational model, which would reduce the need for experimentation to test the impact of alternative designs on user performance. He developed and tested a computational model (P131 USER) for predicting Working Memory (WM) error rates in a particular type of human-computer interaction: phone based interaction. A working version of PHI USER was developed and used to generate predictions about the impact of three factors on WM failure:

- Structure of the interface menu hierarchy. This refers to the various steps users would have to navigate through in order to accomplish a particular task.
- Individual differences in cognitive abilities, which would affect the WM capacity. People with superior cognitive abilities would be expected to have a higher WM capacity and hence lower WM errors rate.
- And task, characteristics, which refers to task format and number of tasks a user is expected to perform. A complex task for which a user would have to input information or if a user wishes to perform a series of task would affect the WM errors rate.

The characteristic that is most relevant for the current research is the structure of the interface menu.

The research was based on the theory of WM (Just and Carpenter, 1992) that proposes that the storage and processing of information generate demands for WM resources. The predictions of the theory were tested on human subjects by requiring them to interact with a phone-based registration system of a University (Tele-registration). The empirical results provided strong evidence for the importance of storage demands, and moderate evidence for the importance of processing demands as predictor of WM failure in PBI. The results also provided evidence for the importance of individual memory differences in WM capacity as a predictor of WM failure in PBI. Based on the results of this study, Brian suggested several guidelines for the effective design of phone based interfaces. The results of Brian's study have an important bearing on the current research and his design guidelines as well as the best practices in the industry reviewed in the following sections were utilized in the development of an effective IVR script for the WCB.

The research conducted by Huguenard was based entirely on interaction with an automated phone-based system without live agent support. The nature of the current research is slightly different as the option to speak to a CSR at WCB is available during regular business hours, i.e., from 7 am to 7 pm Monday through Friday. However, the study is still helpful for the part where a client interacts with an IVR before speaking to a live agent exclusively interacts with an IVR system outside of business hours. [7]

2.1.2 Bradley et al (1996) PI

A major study on IVR systems in American companies was done by the Enterprise Integration Group (EIG), a consulting company in the U.S. The principal author of the report, that is available in the market for approximately U.S. \$3,000, was Gary Bradley who was assisted by a team of consultants from the EIG. The team developed a methodology to rate the IVR systems by compiling a list of over 3000 telephone numbers in the Directory selected at random for businesses they thought would likely have an IVR system. Researchers were trained in what features to look for and how to evaluate the IVR systems. They were then asked to call these numbers and evaluate the systems based on the pre-defined criteria. Results for each survey were closely monitored and reviewed by an IVR specialist. Each surveyor evaluated a variety of IVRs across multiple industries. [8]

During the actual evaluation process each surveyor called the telephone numbers assigned to them and recorded the total seconds required for the initial greeting and the first menu,

navigated all open menus in the application recording each individual option and the key(s) required to select it. They also accessed restricted menus where they could get hold of the required account numbers and codes through the help of friends, relatives, and team members. They also made written notes of their observations and posted their evaluations to a summary sheet.

This study utilized a standard scoring mechanism developed by an expert at EIG and divided the observations in four categories with a maximum attainable of 25 points adding up to a total of 100 points for an IVR system. These four categories were Voice Quality, Information Delivery, User Friendliness, and Ease of Operation.

A final count of 409 completed surveys was obtained as about 60% of the 3000 numbers enlisted turned out to be live answer, not 1VR. Another 25% were automated attendants who just perform basic operations like directory assistance and were not targeted by the study. These figures reveal that the IVR technology is untapped by a lot of businesses and there are tremendous opportunities for cost savings and process improvements by utilizing this technology. This also points towards the need for more research into this area to help businesses realize benefits from implementing a call center. [8]

The study came up with five general findings:

1. Most IVR applications lack a serious customer-oriented design. They are not easy to use and lack desirable features (such as letting the callers know the anticipated wait-time).
2. A large number of IVR applications offer an excessive number of menu options. This might actually inhibit the use of the IVR system as customers get frustrated with too many options.
3. State-of-the-art 1VR technology (that includes features like letting the users know the wait time, automatically faxing information, etc.) is not being aggressively deployed.
4. A large number of businesses are not utilizing the CTI technology. WCB is a case iii point.
5. And as a result of the preceding two points, enterprises are missing opportunities for proactive relationship management.

Based on these findings the research team developed a methodology for designing and implementing an IVR system in organizations. This process is a disciplined multi-step approach for either re-engineering existing applications or creating new applications. The EIG

team developed this methodology iteratively, seeking input from a wide variety of subject matter experts. The suggested guidelines for a good IVR system developed by the team consist of 12 steps. These steps are mostly related to simplified design that restricts menu choices to no more than three, and use of simple and straightforward language. These suggestions were tested in this study by requiring student subjects to respond to questions on 'ease of use' and 'ease of understanding' on the student questionnaire, during their interaction with the IVR simulation developed for WCB. In their steps, the EIG team also suggests testing and refining IVR prototypes, before putting it in a production mode. Due to copyright restrictions, details on the 12 steps cannot be disclosed in this thesis. In addition to the methodology the team also suggested specific application design and menu design criteria. This included recommended introduction in seconds, commands for return and cancel, and the choice of delimiter, among many others. These suggestions were reviewed and incorporated in the best practices which were utilized for the design of the IVR script for WCB in this study. [8]

2.2 Technologies Used.

DTMF signals (Entered from the telephone keypad) and natural language speech recognition interpret the callers response to voice prompts. Other technologies include the ability to speak complex and dynamic information such as an email, news report or weather information using text-to-speech (TTS). TTS is a computer generated synthesized speech that is no longer the robotic voice generally associated with computers. Real voices create the speech in tiny fragments that are spliced together (concatenated) before being played to the caller. [11]

All the three Microcontrollers will have the same internal architecture, but they differ in the following Aspects. 8031 has 128 bytes of RAM, two timers and 6 interrupts. 8051 has 4K ROM, 128 bytes of RAM, two timers and 6 interrupts. 8052 has 8K ROM, 256 bytes of RAM, three timers and 8 interrupts. Of the three microcontrollers, 8051 is the most preferable. Microcontroller supports both serial and parallel communication. In the concerned project 8052 microcontroller is used. After conclusion, here we have used at AT89S52 microcontroller in our project. [11]

2.3 Existing System.

To know the admission details of the college the student should have to approach the college. This may be very time consuming and if the student is living outside the state then it is very time consuming and costly. Many business applications employ this technology including telephone banking, order placement, caller identification and routing, balance inquiry, and airline ticket booking. A simple Voicemail system is different from an IVR in that it is person to person whereas an Interactive voice response system (IVRs) is person to computer. [11]

CHAPTER 3

DESIGN METHODOLOGY

3.1 PROJECT SPECIFICATION

- Operating Frequency:- 850/900/1800/1900 MHZ
- Input Power supply : 12V, 1A DC
- Mp3 module capacity :-1000 audio clips
- USB 2.0:- 9600 baud rate it will save txt file
- Operating temperature range:- -40°C to $+125^{\circ}\text{C}$
- Portable circuit
- Cost effective

3.2 BLOCK DIAGRAM AND DESCRIPTION

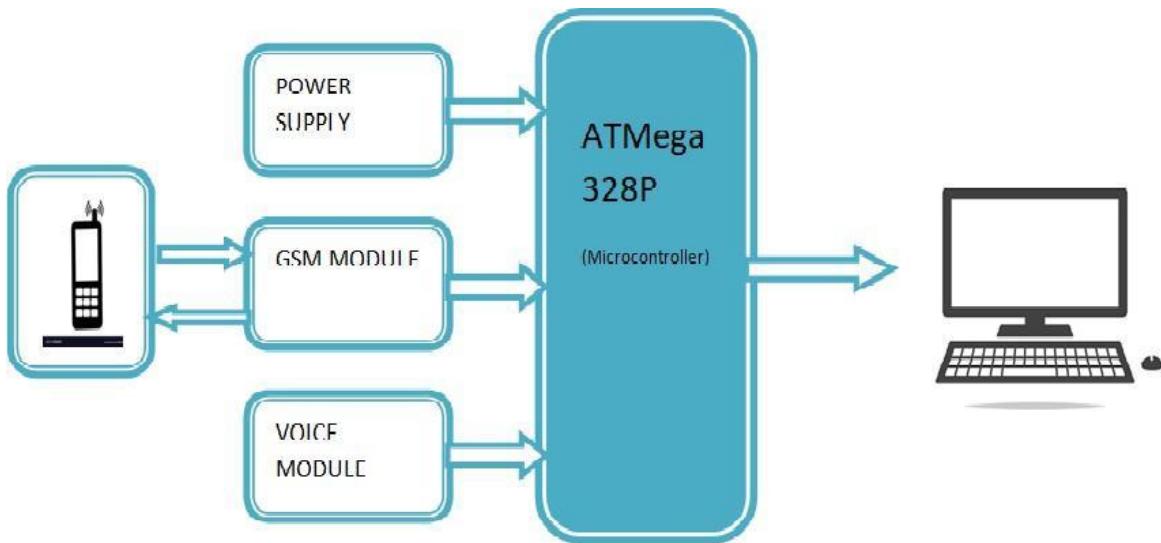


Fig. 3.2 Block Diagram

3.2 Block Description

The main blocks of my system are as follows:

- Microcontroller
- DTMF Decoder
- GSM Module
- Voice Module
- LCD Display

3.2.1 Microcontroller

The ATmega328P is a low-Power CMOS 8-bit microcontroller primarily based at the AVR improved RISC architecture. It is employs two I/O ports, two USARTs and an external interrupt. The main reason for adopting this microcontroller is availability of two USARTs; one is used for communicating with database and the other for Voice. DTMF Decoder gives an interrupt signal to microcontroller the use of certainly one of its outside interrupts and 4-bit BCD code corresponding to the important thing. It controls voice IC through port pins to generate required prompt message. It is also used to pick required message set off from voice IC by using creating a lively low sign at required pin. The alerts from microcontroller are basically in TTL common sense which have to be converted into USB kind to make the sign comprehensible to the records base gaining access to gadgets like computers or servers this is executed via using PL2303. Since ATmega328P is used in Arduino Uno and Arduino nano boards, you could immediately replace the arduino board with ATmega328 chip. For that first we likely need to install the Arduino bootloader into the chip. This IC with bootloader can be located on Arduino Uno board and burn this system into it. Once Arduino program is burnt into the IC, it could be removed and utilized in place of Arduino board, at the side of a Crystal oscillator and other additives as required for the task.

Pin No.	Pin name	Description	Secondary Function
1	PC6 (RESET)	Pin6 of PORTC	Pin by default is used as RESET pin. PC6 can only be used as I/O pin when RSTDISBL Fuse is programmed.
2	PD0 (RXD)	Pin0 of PORTD	RXD (Data Input Pin for USART) USART Serial Communication Interface [Can be used for programming]
3	PD1 (TXD)	Pin1 of PORTD	TXD (Data Output Pin for USART)

			USART Serial Communication Interface [Can be used for programming]
			INT2(External Interrupt 2 Input)
4	PD2 (INT0)	Pin2 of PORTD	External Interrupt source 0
5	PD3 (INT1/OC2B)	Pin3 of PORTD	External Interrupt source1 OC2B(PWM - Timer/Counter2 Output Compare Match B Output)
6	PD4 (XCK/T0)	Pin4 of PORTD	T0(Timer0 External Counter Input) XCK (USART External Clock I/O)
7	VCC		Connected to positive voltage
8	GND		Connected to ground
9	PB6 (XTAL1/TOSC1)	Pin6 of PORTB	XTAL1 (Chip Clock Oscillator pin 1 or External clock input) TOSC1 (Timer Oscillator pin 1)
10	PB7 (XTAL2/TOSC2)	Pin7 of PORTB	XTAL2 (Chip Clock Oscillator pin 2) TOSC2 (Timer Oscillator pin 2)

11	PD5 (T1/OC0B)	Pin5 of PORTD	T1(Timer1 External Counter Input) OC0B(PWM - Timer/Counter0 Output Compare Match B Output)
12	PD6 (AIN0/OC0A)	Pin6 of PORTD	AIN0(Analog Comparator Positive I/P) OC0A(PWM - Timer/Counter0 Output Compare Match A Output)
13	PD7 (AIN1)	Pin7 of PORTD	AIN1(Analog Comparator Negative I/P)
14	PB0 (ICP1/CLKO)	Pin0 of PORTB	ICP1(Timer/Counter1 Input Capture Pin) CLKO (Divided System Clock. The divided system clock can be output on the PB0 pin)
15	PB1 (OC1A)	Pin1 of PORTB	OC1A (Timer/Counter1 Output Compare Match A Output)
16	PB2 (SS/OC1B)	Pin2 of PORTB	SS (SPI Slave Select Input). This pin is low when controller acts as slave. [Serial Peripheral Interface (SPI) for programming]

			OC1B (Timer/Counter1 Output Compare Match B Output)
17	PB3 (MOSI/OC2A)	Pin3 of PORTB	MOSI (Master Output Slave Input). When controller acts as slave, the data is received by this pin. [Serial Peripheral Interface (SPI) for programming] OC2 (Timer/Counter2 Output Compare Match Output)
18	PB4 (MISO)	Pin4 of PORTB	MISO (Master Input Slave Output). When controller acts as slave, the data is sent to master by this controller through this pin. [Serial Peripheral Interface (SPI) for programming]
19	PB5 (SCK)	Pin5 of PORTB	SCK (SPI Bus Serial Clock). This is the clock shared between this controller and other system for accurate data transfer. [Serial Peripheral Interface (SPI) for programming]
20	AVCC		Power for Internal ADC Converter
21	AREF		Analog Reference Pin for ADC
22	GND		GROUND

23	PC0 (ADC0)	Pin0 of PORTC	ADC0 (ADC Input Channel 0)
24	PC1 (ADC1)	Pin1 of PORTC	ADC1 (ADC Input Channel 1)
25	PC2 (ADC2)	Pin2 of PORTC	ADC2 (ADC Input Channel 2)
26	PC3 (ADC3)	Pin3 of PORTC	ADC3 (ADC Input Channel 3)
27	PC4 (ADC4/SDA)	Pin4 of PORTC	ADC4 (ADC Input Channel 4) SDA (Two-wire Serial Bus Data Input/output Line)
28	PC5 (ADC5/SCL)	Pin5 of PORTC	ADC5 (ADC Input Channel 5) SCL (Two-wire Serial Bus Clock Line)

Table No: 1 Pin description of ATMEGA328P

Applications for ATMEGA328P:

- Used in ARDUINO UNO, ARDUINO NANO and ARDUINO MICRO boards.
- Industrial control systems.
- SMPS and Power Regulation systems.
- Digital data processing.
- Analog signal measuring and manipulations.
- Embedded systems like coffee machine, vending machine.
- Motor control systems.
- Display units.
- Peripheral Interface system.



Photo 3.2.1: ATMEGA328P

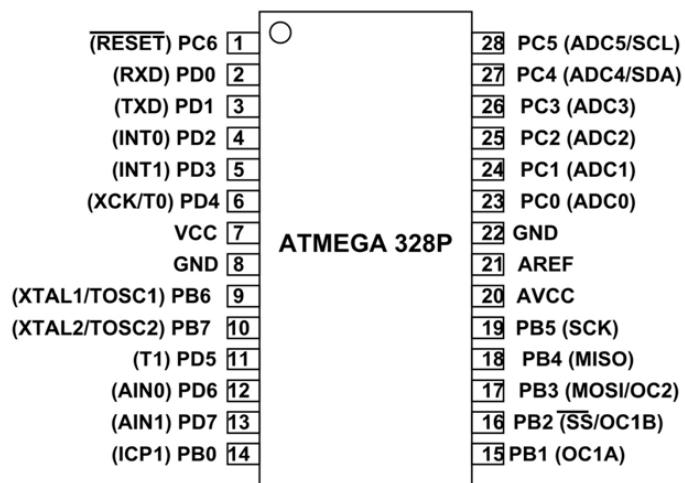


Fig. 3.2.1 Pin Diagram of ATMEGA328P

3.2.2 DTMF Decoder

The DTMF decoder is employed to identify the tone given from the keypad. This can be achieved by characterizing individual frequencies for each row and column of keypad so that when a key is pressed a dual tone multiple frequency (DTMF) is generated which is equal to sum of rows and columns frequencies. When a valid tone is detected then STD pin is pulled high. The detected tone which is given as 4-bit BCD code to one of input ports which represents corresponding key. The output coming from speaker of GSM module is connected to DTMF decoder. The signal coming from speaker of GSM module has very high amount of noise to achieve better performance a filter can be included between GSM module and DTMF decoder unit.

Advantages of Dual Tone Multi-Frequency

- By using this it is possible to get quick response
- It is inexpensive to construct.
- High reliability and fast efficient
- By using a single key we can control 6 devices.
- By using this we can control the home appliances wirelessly
- By using this the power consumption will be reduced and power efficiency will be increased.

The applications of DTMF (dual tone multiple frequency) mainly involve the following

- The dual tone multiple frequency(DTMF) is used to identify the dialed numbers in the telephone switching centers
- These are used to operate the remote transmitters in a terrestrial stations
- Dual tone multiple frequency (DTMF) is applicable in IVR systems, home automation, call centers, security systems, as well as industrial applications

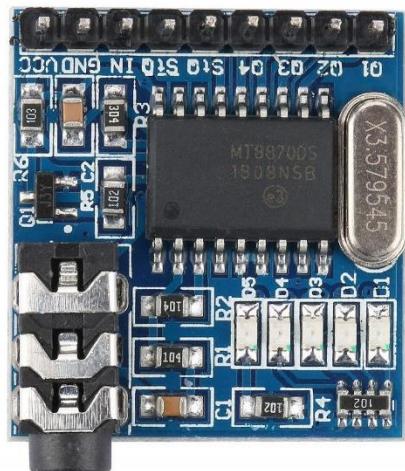


Photo 3.2.2: DTMF Decoder MT88700S

3.2.2 GSM Module

The SIM800A Quad-Band GSM/GPRS Module with RS232 Interface is a whole Quad-band GSM/GPRS answer in an LGA (Land grid array) type which can be embedded within the purchaser programs. SIM800A guide Quad-band 850/900/1800/1900 MHz, it may transmit Voice, SMS and facts records with low strength intake. With a tiny size, it may healthy into narrow and compact demands of custom layout. Featuring and Embedded AT, it lets in general value financial savings and rapid time-to-market for consumer applications.

The SIM800A modem has a SIM800A GSM chip and RS232 interface at the same time as allows easy reference to the laptop or laptop the use of the USB to the Serial connector or to the micro-controller using the RS232 to TTL converter. Once you join the SIM800A modem the use of the USB to RS232 connector, you want to discover the suitable COM port from the Device Manager of the USB to Serial Adapter.

Then you can open Putty or every other terminal software and open a connection to that COM port at 9600 baud rate, which is the default baud fee of this modem. Once a serial connection is open via the pc or your micro-controller you could start sending the AT commands. When you send AT commands for example “ATr” you have to get hold of returned a reply from the SIM800A modem pronouncing “OK” or different reaction depending on the command sent.

Features and Specifications of SIM800A Module:-

- SIM800A Quad Band GSM Module
- Bands: GSM 850MHz, EGSM 900MHz, DCS 1800MHz, PCS 1900MHz
- Coding schemes: CS-1, CS-2, CS-3, CS-4 Tx power: Class 4 (2W), Class 1 (1W)
- GPRS class 2/10.
- Control via AT commands (3GPP TS 27.007, 27.005 and SIMCOM enhanced AT command set).
- Voltage Supply Required- 9VDC to 12VDC with at least 2A Peak Current Capability
- High-Quality Product (Not hobby grade).
- 5V interface for direct communication with MCU kit.
- TTL Rx and TTL Tx and DB9 Connector Based RS232 Outputs
- Configurable baud rate.
- Built-in SIM Card holder.
- Built-in Network Status LED.
- Inbuilt Powerful TCP/IP protocol stack for internet data transfer over GPRS.
- Low power.
- Operating temperature: -40C to +85C
- External Finger type antenna

Applications:-

- Remote Data Monitor and Control.
- Water, gas and oil flow metering.
- AMR (automatic meter reading).
- Power station monitoring and control.
- Remote POS (point of sale) terminals.
- Traffic signals monitor and control.
- Fleet management.
- Power distribution network supervision.
- Central heating system supervision.
- Weather station data transmission.
- Hydro-logic data acquisition.
- Vending machine.
- Traffic info guidance.
- Parking meter and Taxi Monitor.
- Telecom equipment supervision (Mobile base station, microwave or optical relay station).



Photo 3.2.3: SIM800A GSM Module

3.2.3 Voice Module

The JQ6500 mp3 module is a simple module that can play typical stereo or mono MP3 files. The controlling of this module can be done through buttons or a serial communication protocol. This kind of module works through two dissimilar modes to activate it like serial communication & AD button control. In the first mode, the module is connected to a microcontroller whereas, in the second mode, the module is controlled through switches. JQ6500 MP3 Player module is available in two models like JQ6500-28p & JQ6500-16p. The JQ6500 28P model includes onboard memory and also includes a slot of Micro SD card. This slot is very helpful to upload your MP3 files into Micro SD, use an OS except for Windows because you simply require a standard Micro SD card formatted with FAT. This is the best option if you need to make a music player. JQ650016P mp3 modules include an onboard 2 Megabyte or 16Mbit Flash memory. Using Windows software into the device & come into view once you fix it to USB & MP3 files can be uploaded directly to your device. If you require fewer bitrates MP3s, then this is the best option. These modules are available in two versions, the pin out & functionality are similar, the only difference is that the original one like V2.1 includes a Micro-USB in place of a small USB connector.

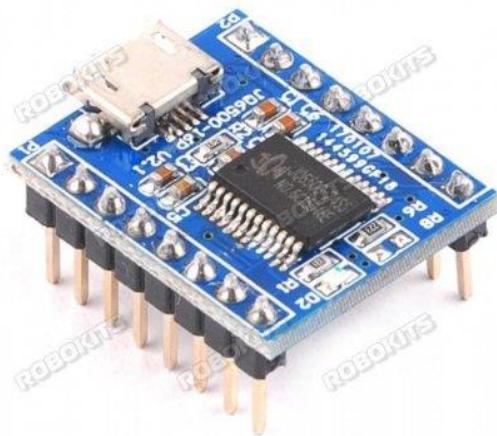


Photo 3.2.4: Voice Module

JQ6500 MP3 Player Module Pin Configuration

The pin configuration of the JQ6500 MP3 Player includes the following, this module has 16 pins where each pin & its functionality is described below.

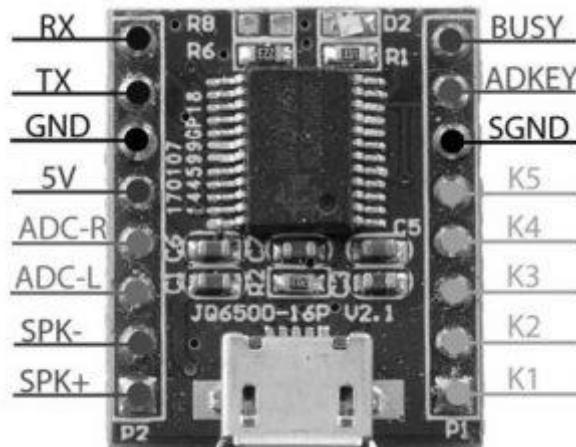


Fig 3.2.4: JQ6500 Pin Configuration

- Pin K1 is a Playback of Audio 1
- Pin K2 is a Playback of Audio 2
- Pin K3 is a Playback of Audio 3
- Pin K4 is a Playback of Audio 4
- Pin K5 is a Playback of Audio 5
- Pin SGND is a Ground
- Pin ADKEY is an AD port
- Pin BUSY is a Play Indicator

- Pin RX UART is a serial data input
- Pin TX UART is a serial data output
- Pin GND is called Ground
- Pin VCC 5V is used for power supply
- Pin ADC_R is an Amplifier or Headphones (Right Channel)
- ADC_L Pin is Amplifier or Headphones (Left Channel)
- SPK- pin is a negative terminal of the speaker
- SPK+ pin is a positive terminal of the speaker

Features of JQ6500 Module

The features of JQ6500 include the following.

- The sampling rate supported by JQ6500 is like 8 KHz / 11.025 KHz / 12 KHz /16 KHz / 22.05 KHz / 24/32 KHz / 44.1 KHz / 48 KHz
- Output is 24-bit DAC, the support of dynamic range is 90dB & SNR is 85dB
- Operates in three control modes like parallel port, serial port, & AD button
- It supports FAT16 & FAT32 file systems, where the major supports are 32G TF card, 32G U disk, 64M bytes of NOR FLASH
- To play the particular music, it can be controlled by the serial port of the microcontroller
- The sorting of audio data can be done through the folder, equal to 100 folders, where each folder can be allocated with hundreds of songs
- Adjustable with 30 level & 10 EQ
- Specifications
- The specifications of JQ6500 include the following.
- It supports all types of bit rates like 11172-3 & ISO13813-3 sampling rate with audio decoding.
- It supports different sound effects like Jazz, Normal, Classic, Rock, Pop, etc
- Humidity ranges from 5% to 95%
- UART Interface: TTL level, Standard serial port, baud rate can be set
- Operating temperature ranges from -40°C to 70°C
- Input voltage: Power supply ranges from 3.2V to 5V, but power supply like 4.2V is the best
- Normal DIP16 package
- The Rated current is 20ma

3.2.4 LCD Display

The term LCD stands for liquid crystal show. It is one form of electronic display module used in an intensive range of packages like numerous circuits & devices like cellular phones, calculators, computer systems, TV sets, and so on. These displays are mainly favored for multi-segment light-emitting diodes and seven segments. The primary blessings of using this module are inexpensive; honestly programmable, animations, and there are no obstacles for showing custom characters, unique and even animations, and so forth.



Photo 3.2.5: LCD display

LCD 16×2 Pin Diagram

The 16×2 LCD pinout is shown below.

- Pin1 (Ground/Source Pin): This is a GND pin of display, used to connect the GND terminal of the microcontroller unit or power source.
- Pin2 (VCC/Source Pin): This is the voltage supply pin of the display, used to connect the supply pin of the power source.
- Pin3 (V0/VEE/Control Pin): This pin regulates the difference of the display, used to connect a changeable POT that can supply 0 to 5V.
- Pin4 (Register Select/Control Pin): This pin toggles among command or data register, used to connect a microcontroller unit pin and obtains either 0 or 1(0 = data mode, and 1 = command mode).
- Pin5 (Read/Write/Control Pin): This pin toggles the display among the read or writes operation, and it is connected to a microcontroller unit pin to get either 0 or 1 (0 = Write Operation, and 1 = Read Operation).

- Pin 6 (Enable/Control Pin): This pin should be held high to execute Read/Write process, and it is connected to the microcontroller unit & constantly held high.
- Pins 7-14 (Data Pins): These pins are used to send data to the display. These pins are connected in two-wire modes like 4-wire mode and 8-wire mode. In 4-wire mode, only four pins are connected to the microcontroller unit like 0 to 3, whereas in 8-wire mode, 8-pins are connected to microcontroller unit like 0 to 7.
- Pin15 (+ve pin of the LED): This pin is connected to +5V
- Pin 16 (-ve pin of the LED): This pin is connected to GND.



Fig 3.2.5: LCD-16×2-pin-diagram

Features of LCD16x2

- The features of this LCD mainly include the following.
- The operating voltage of this LCD is 4.7V-5.3V
- It includes two rows where each row can produce 16-characters.
- The utilization of current is 1mA with no backlight
- Every character can be built with a 5×8 pixel box
- The alphanumeric LCDs alphabets & numbers
- Is display can work on two modes like 4-bit & 8-bit

- These are obtainable in Blue & Green Backlight
- It displays a few custom generated characters

3.3 HARDWARE DESIGN (SELECTION CRITERIA)

1) Selection of DTMF Decoder

This is the most important task for our project. As the number pressed by the caller is necessarily to be decoded before sending it to the microcontroller, a DTMF decoder is needed. For our project, we have used DTMF decoder IC MT8870. Its features are:-

- Complete DTMF Receive
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality

2) Selection of Microcontroller

To achieve this task we first analyzed our needs. Those were: -

- To achieve fast operation
- To achieve great sensitivity

So for these we decided to select microcontroller AtMega328P-. As it is having enough amount of RAM for such simple operations of reading. It supports high speed operation and has greater sensitivity while put into scanning mode of its inputs. Actually AtMega328P is used because we wanted to have serial communication between microcontroller and computer. This supports short distance serial communication. We are using Atmega328P in IC format due to readymade availability of this. Some capacitors must set up along peripherals pins of this IC which we've related in our real circuit. Need of these capacitors is due to fact that AtMega328P datasheet shows need of such capacitors in order to pull data from one point to another point.

3) Selection of Computer

Basically, we're going to put in force a Visual Basic Code and a hardware relying on these VB instructions. So even as deciding on a pc, we taken into consideration a few points like whether or not Microsoft's Visual Basic 6.Zero is set up in this gadget or now not, then gadget's RAM and Hard disk space essential to aid VB surroundings, then secondary elements like color screen for stimulating GUI and appealing model. Also, as our assignment wished a voice card as the output tool, a private laptop with a voice card was selected.

4) Selection of GSM

The SIM800 is a GSM/GPRS-only modem module. It can use both a 2G-simplest SIM or a 3G/4G USIM (which offers compatibility for 2G besides).It will only work on 2G GSM radio networks so you have to check that in your country - for example it won't work on the AT&T or Jio networks.

You will however need to test the card. Some newer SIMs use lower voltages and better frequencies and might not work with older modems or telephones. The reciprocal is likewise true, a more recent phone may not offer an excessive sufficient voltage or low sufficient frequency for an older SIM.

These days no operator issues 2G SIMs anymore since their cryptographic algorithms (COMP128–1, 2 or 3) were pretty weak and are generally not accepted on 3G networks. Any card you may buy is as a minimum USIM and would be able to authenticate on any 2G GSM, 3G UMTS or 4G LTE as well as 5G Non-Standalone.

As a side note LTE and 5G need minimum an USIM to work. The GSM authentication algorithm does not provide the data required for these networks.

5) Selection of Voice module

This module is a brilliant and cheaper approach to add audio on your tasks. The use of an inner flash memory has the advantage of no longer requiring SD cards or other media to keep your audio files; in comparison its potential (16Mbit = 2MByte) makes it more appropriate to breed sound consequences / guide voices than to make a music participant.

This sort of module is very simple to apply and it is able to be controlled manually the usage of

control keys otherwise serial protocol on an average UART serial interface. Using smooth serial instructions, the playing of song may be completed. This module is very simple to apply due to some features like reliability, balance, and so forth. This IC is custom designed uniquely like a cost-effective solution for the right voice playing subject.

3.4 SOFTWARE DESIGN

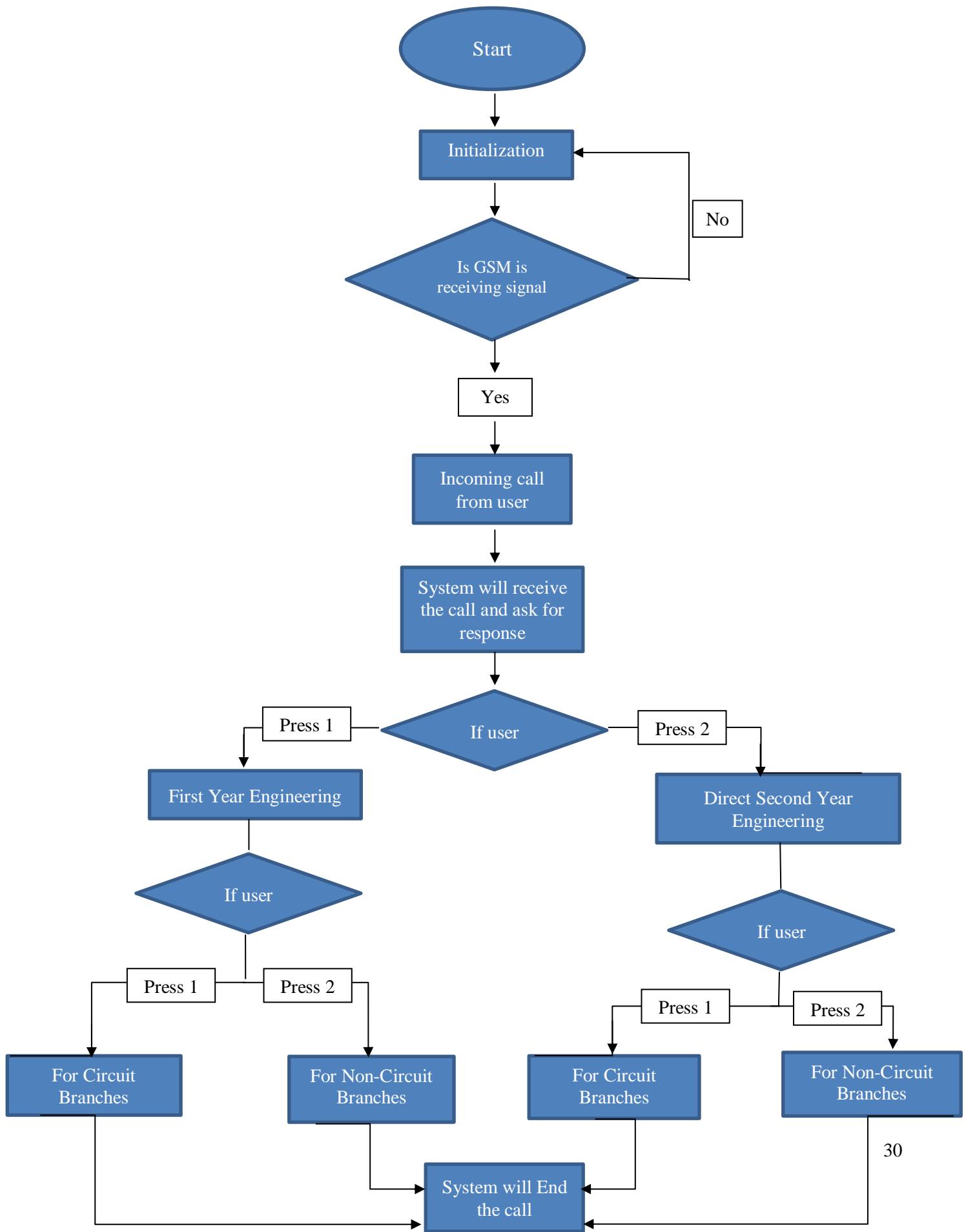
3.4.1 Modern Tools

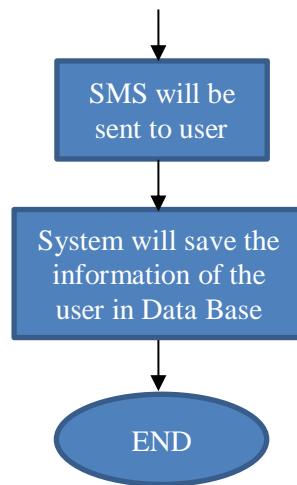
1. Proteus 8.0
2. Arduino IDE
3. CoolTerm

3.4.2 Algorithms

- Start
- Initialization
- If GSM is receiving signal then Incoming call from user
- Else goes back to initialization
- System will receive the call and ask for response
- If user Press 1 for First Year Engineering or else user Press 2 for Direct Second Year Engineering
- Then Press 1 For Circuit Branches or else Press 2 For Non-Circuit Branches
- System will End the call
- SMS will be send to the user
- System will save the information of the user in database
- End

3.4.3 Flowchart





3.5 PCB DESIGN AND LAYOUT

3.5.1 CIRCUIT DIAGRAM

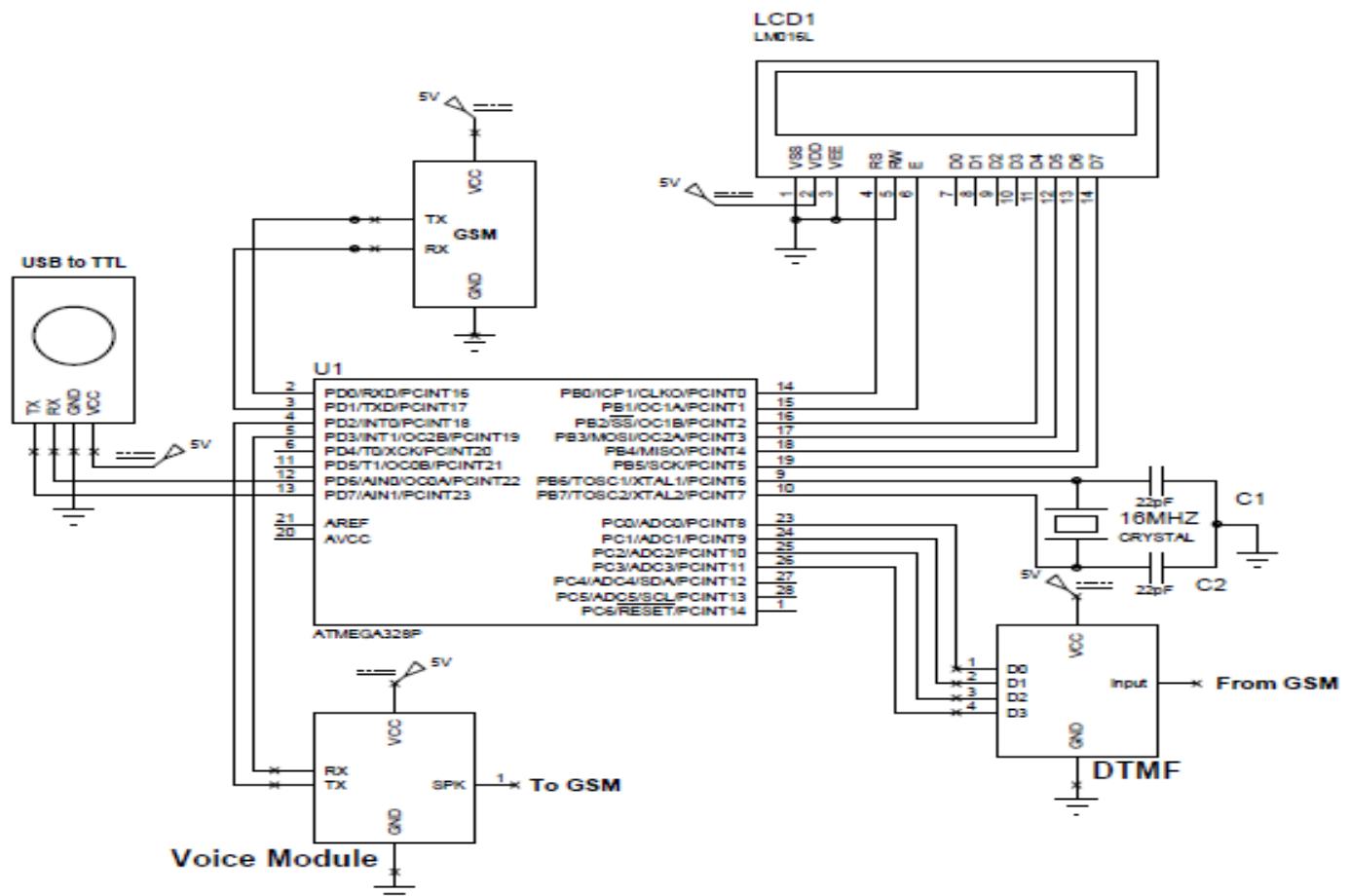


Fig 3.5.1 Circuit Diagram

3.5.2 PCB LAYOUT

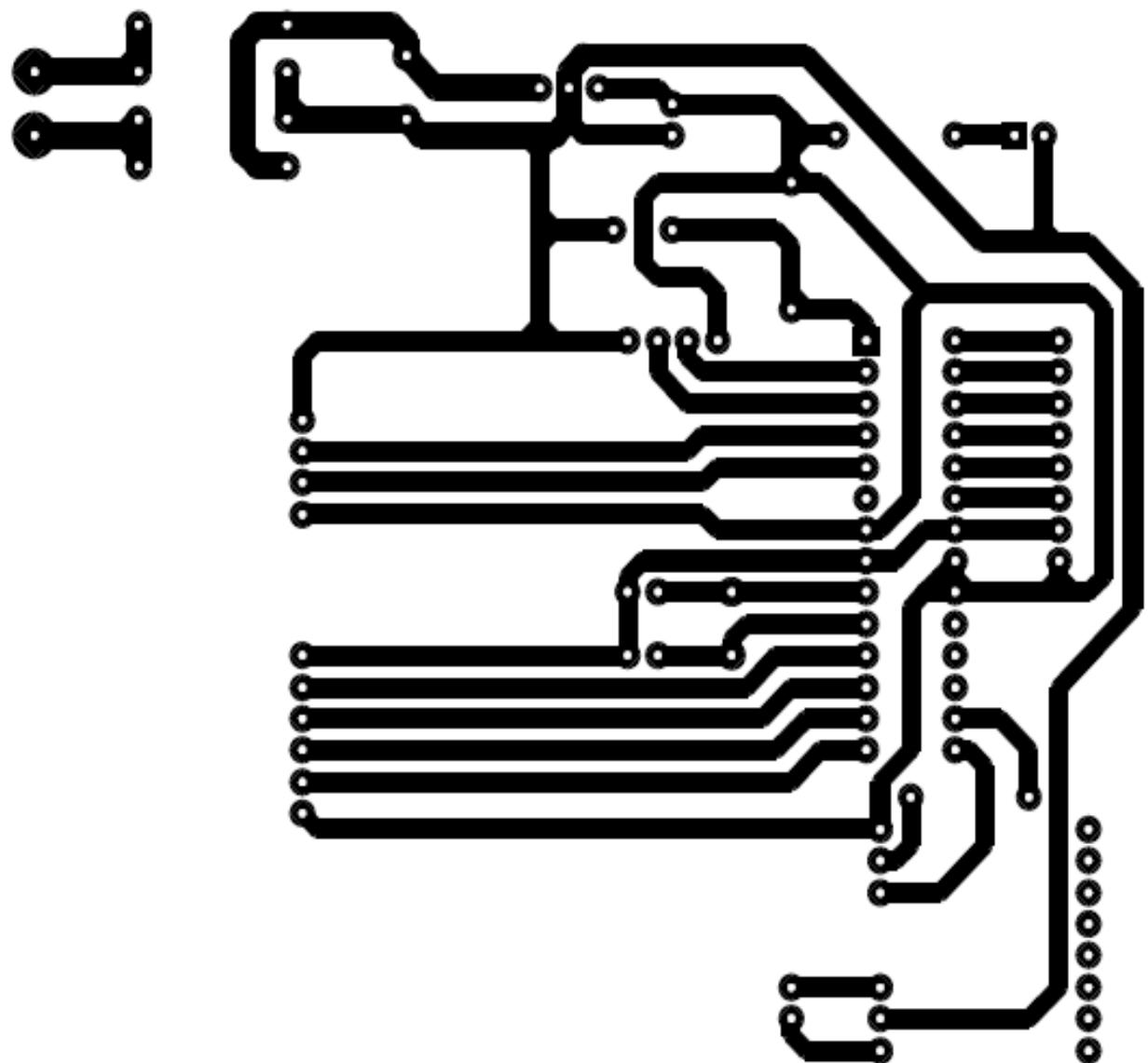


Fig 3.5.2: PCB Layout

3.5.3 PCB DESIGN

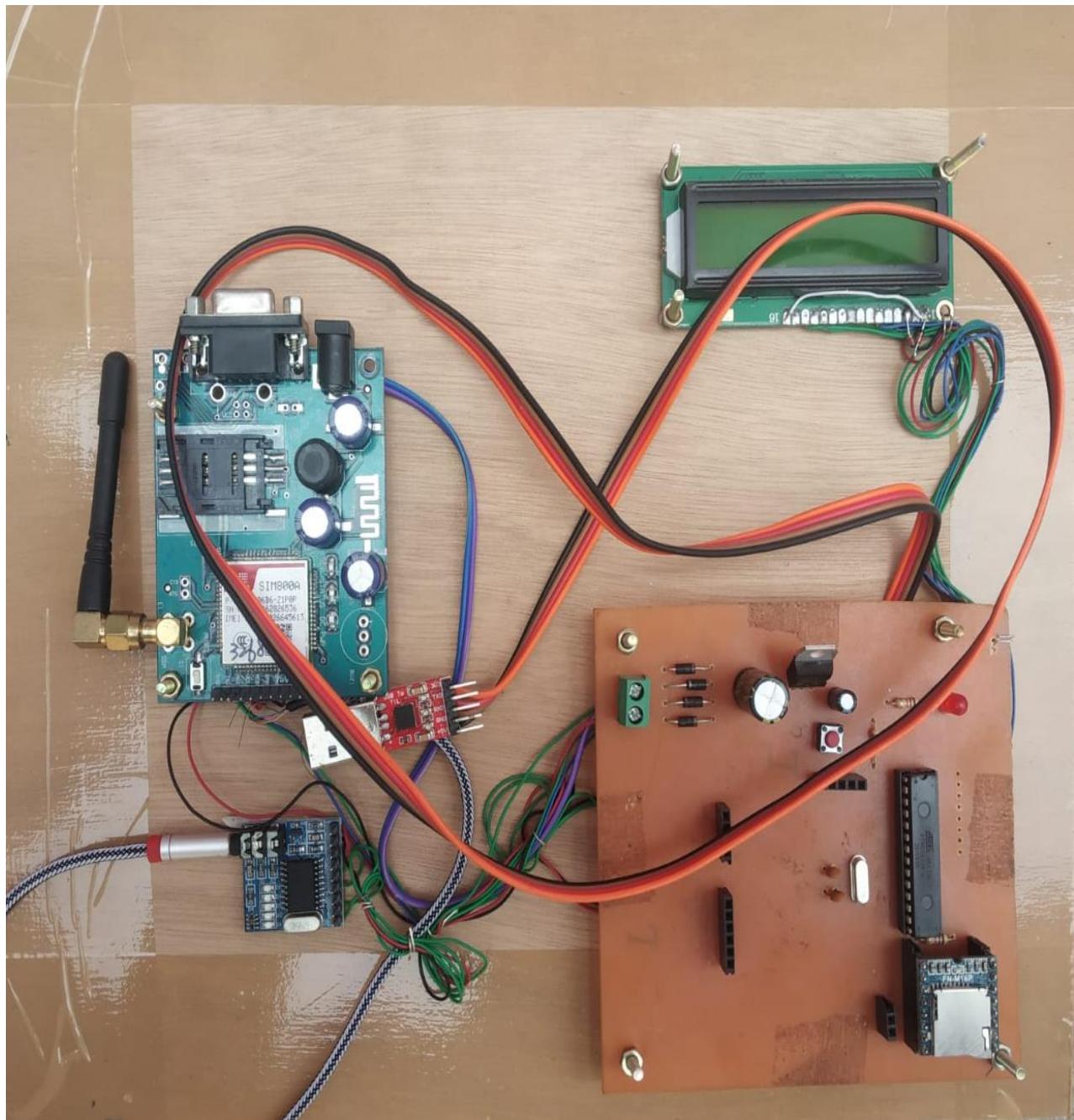


Photo 3.5.3 PCB Design

3.6 Noise immunity of system & Environment related aspects

The system is designed to operate at normal working condition and within a clean working environment. If it is operated in a high temperature environment then it will affect the reliability of the system.

CHAPTER 4

Test procedure and Results

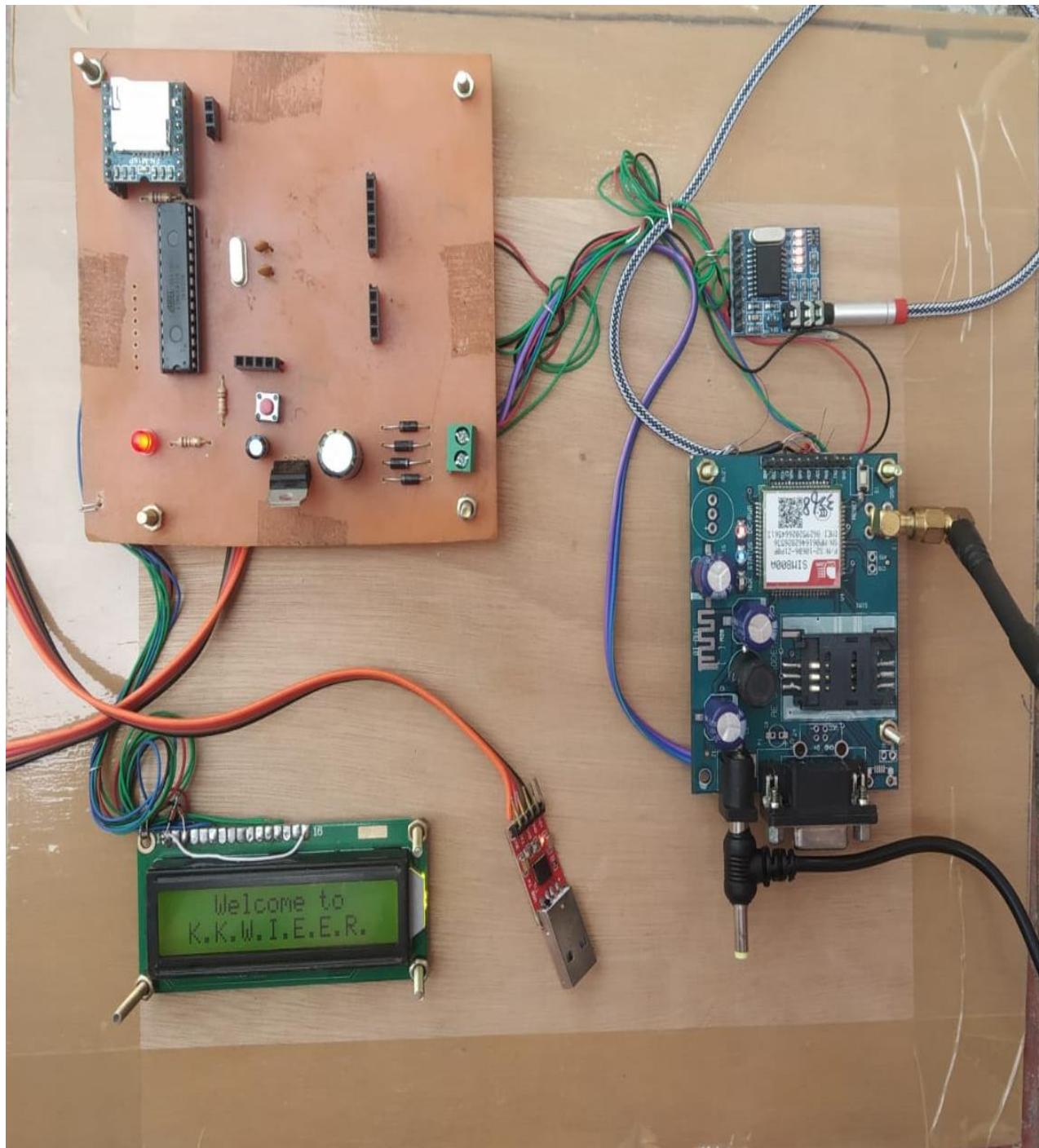


Photo 4.1 Welcome message displayed on LCD
When call is received by the GSM welcome message is displayed on LCD

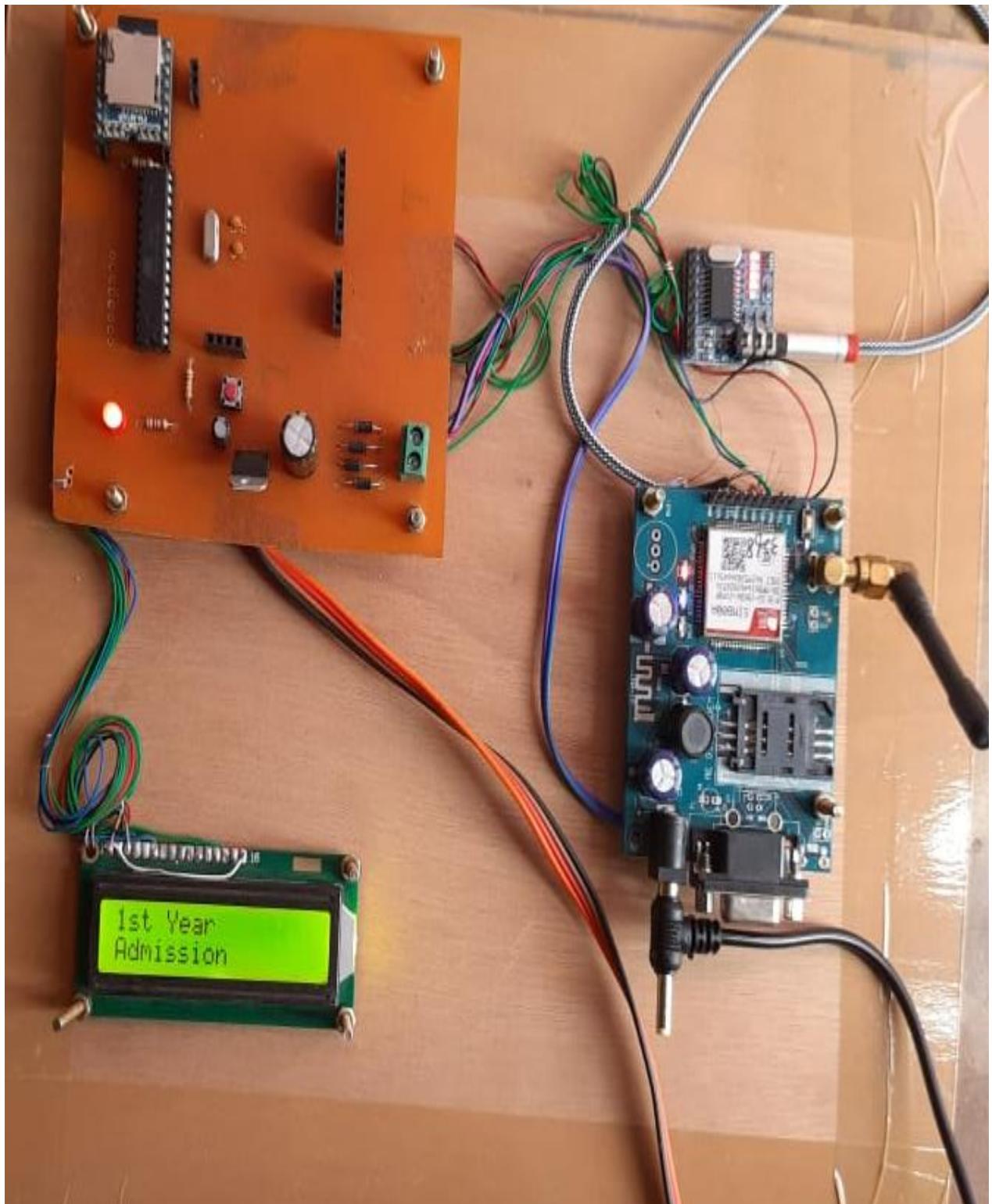


Photo 4.2 Response 1st year admission enquiry

User has Pressed 1 for the 1st year admission enquiry

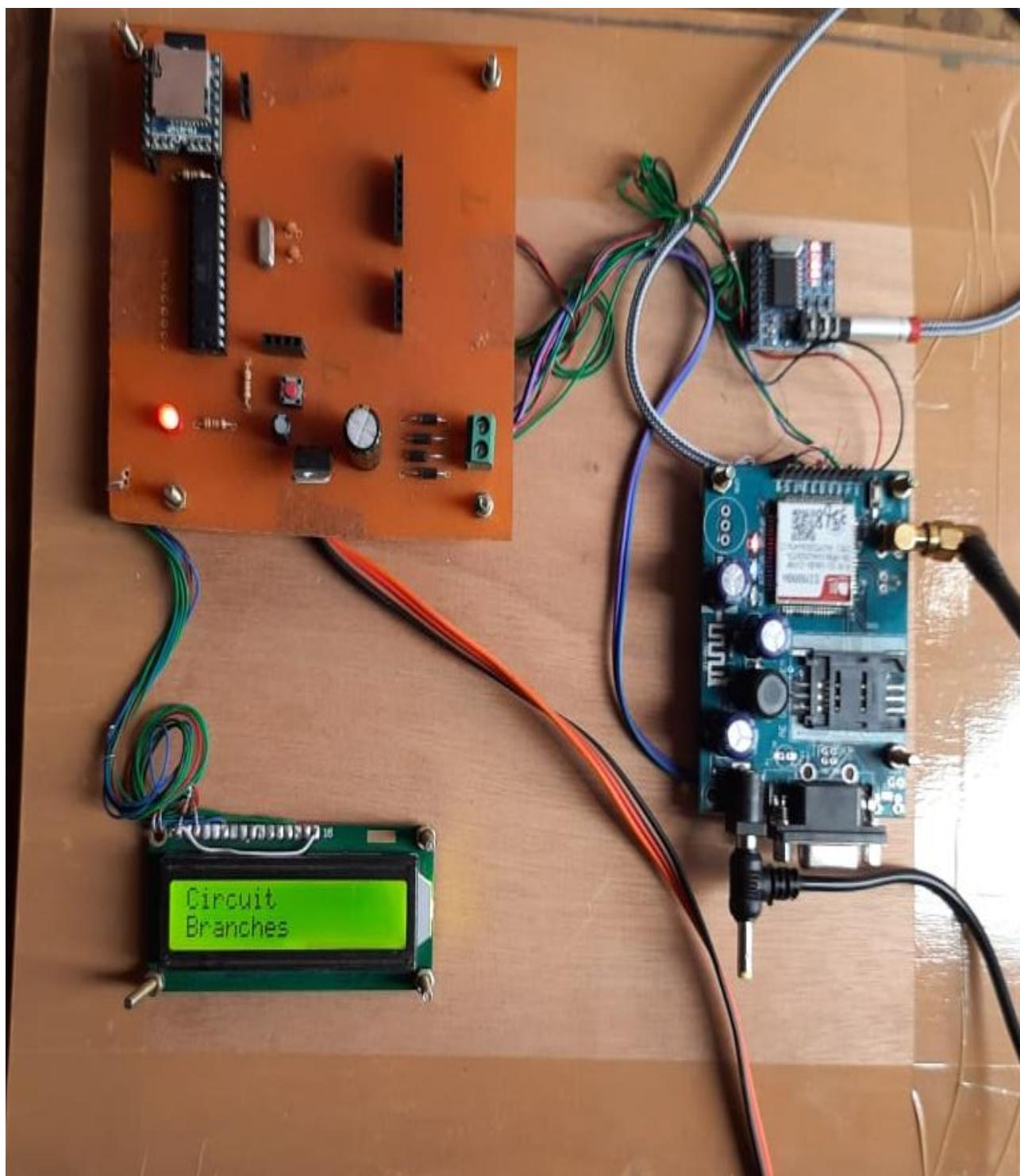


Photo 4.3 Response Circuit Branches
User has Pressed 1 for the Circuit Branches admission enquiry

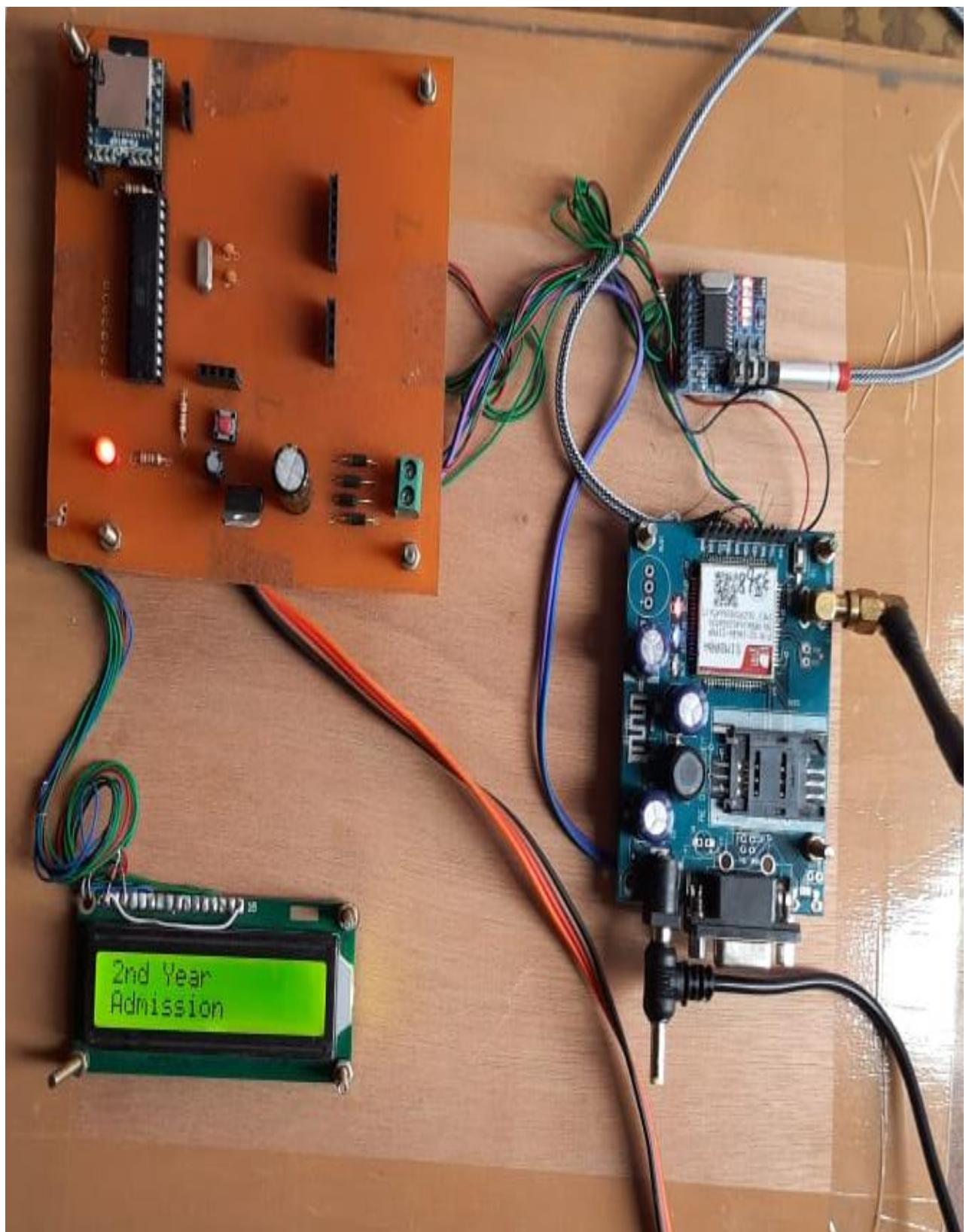


Photo 4.4 Response for Direct 2nd year admission enquiry
User has Pressed 2 for the Direct 2nd year admission enquiry

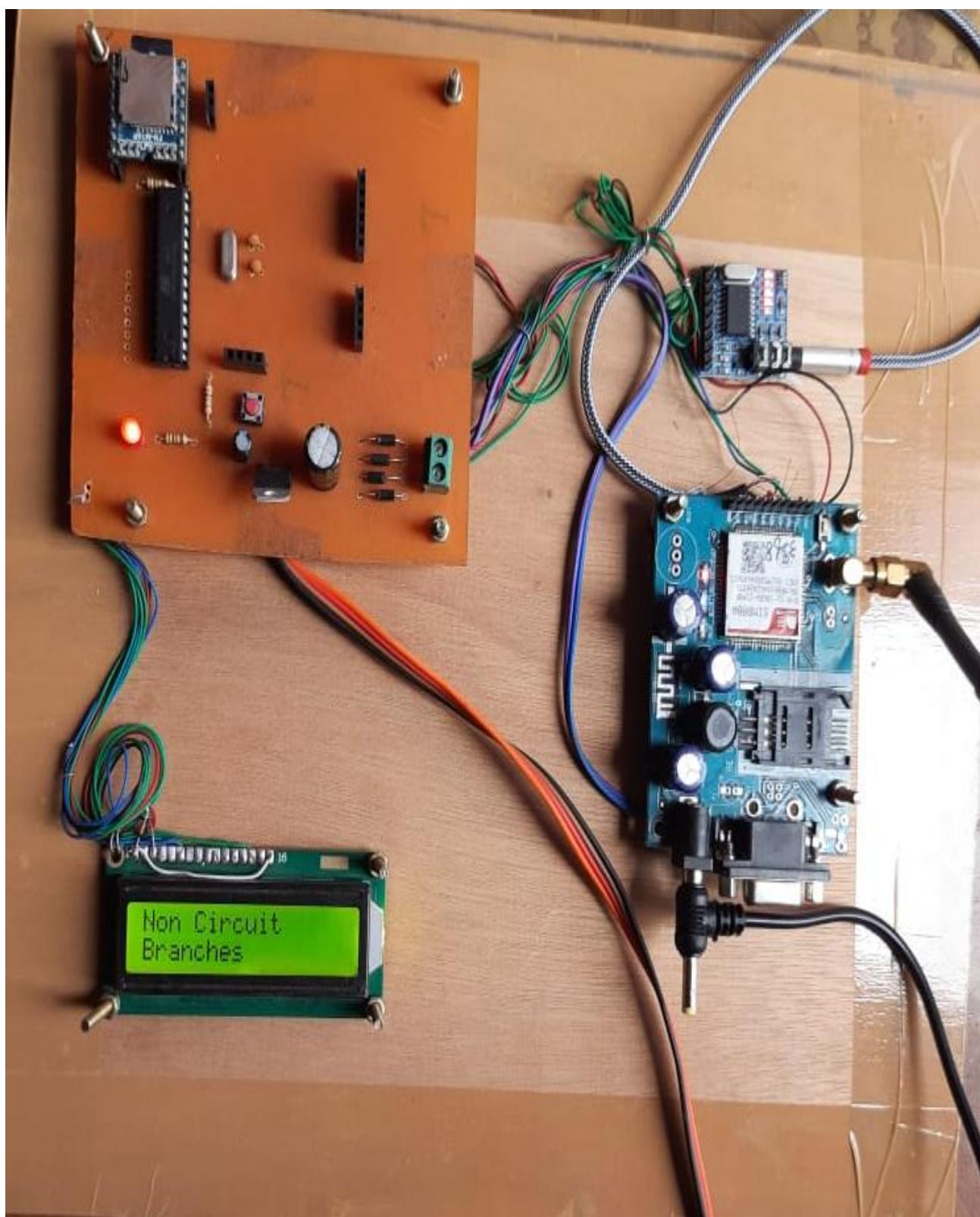


Photo 4.5 Response Non-Circuit Branches
User has Pressed 2 for the 2nd year admission enquiry

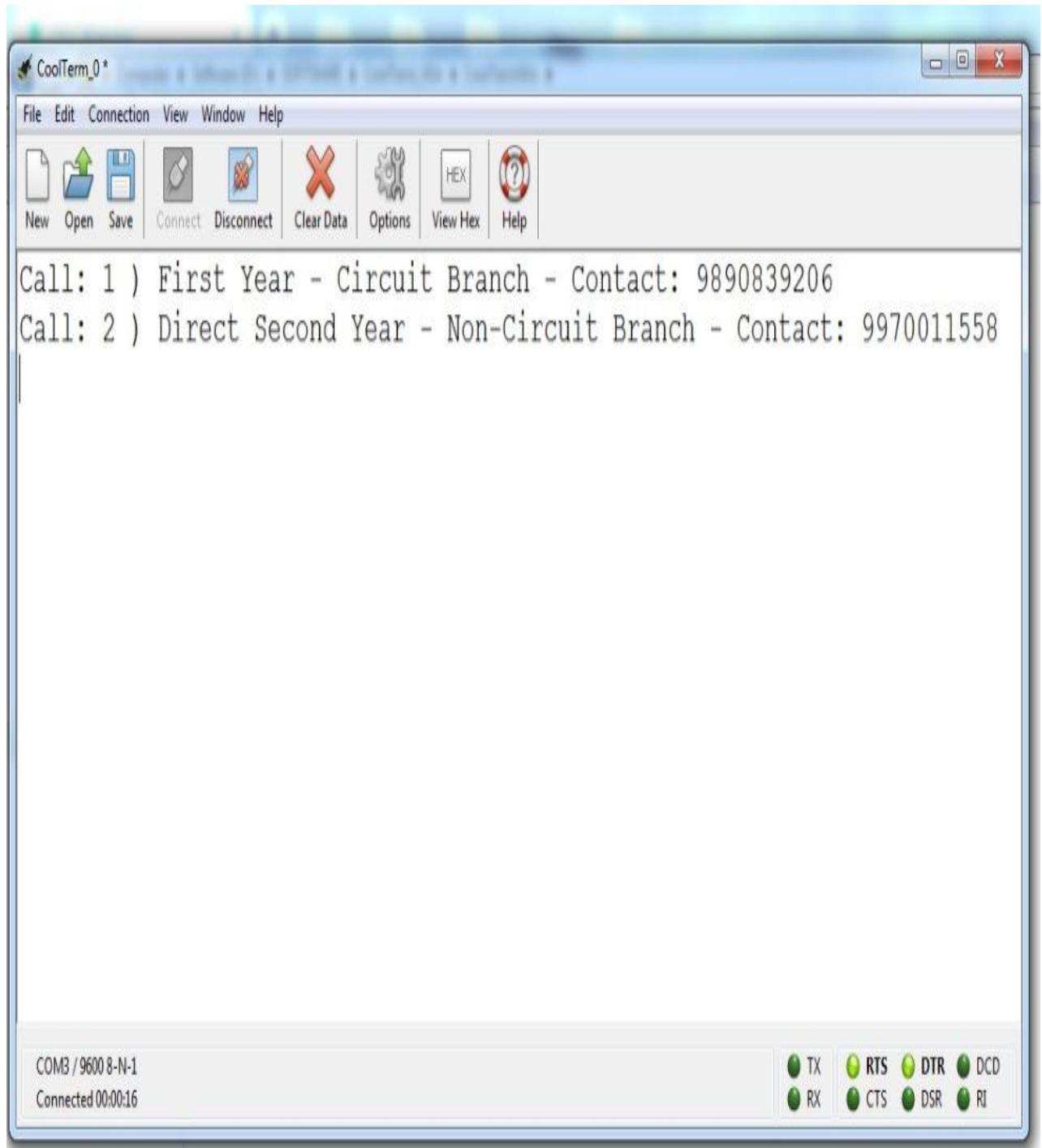


Photo 4.6 Data based on response
Information of Users' response is saved in Data Base

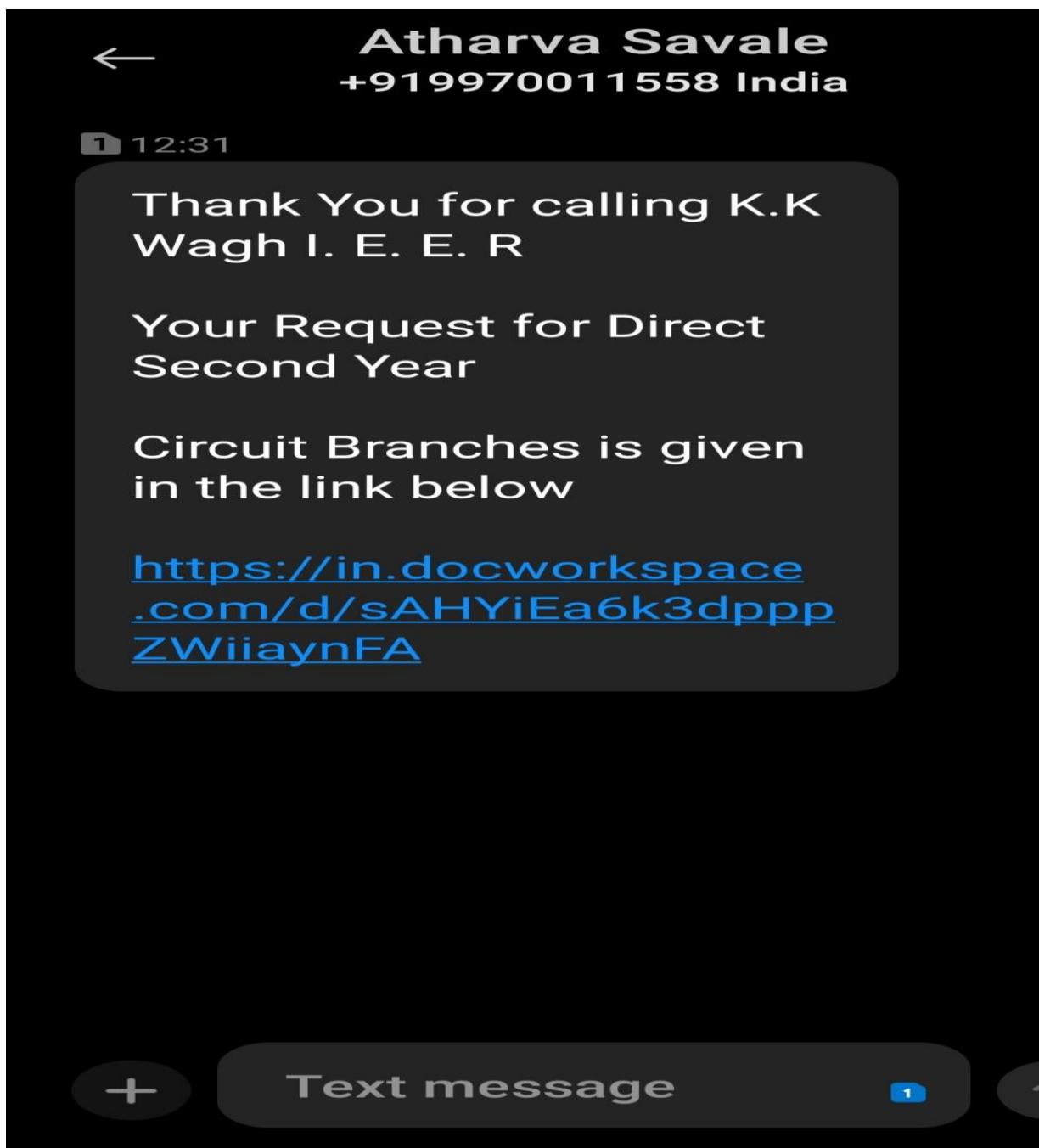
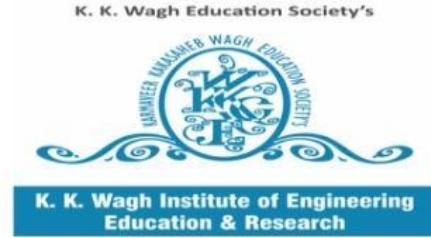


Photo 4.7 SMS sent on mobile number

When User end the call, system will send SMS to the User



Direct Second Year Circuit Branches:

Direct Second Year Admission:

<https://engg.kkwagh.edu.in/admission/index/22>

Circuit Branches:

Electronics and Telecommunication:

https://engg.kkwagh.edu.in/academic_programme/department/2

Electrical: https://engg.kkwagh.edu.in/academic_programme/department/3

Computer

https://engg.kkwagh.edu.in/academic_programme/department/1

IT:

https://engg.kkwagh.edu.in/academic_programme/department/8

FAQ:

https://engg.kkwagh.edu.in/admission_faq



Photo 4.8 Link open for Direct Second year circuit branch

When user open the link user will get information according to response made

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

This System helps the students to get the admission related information for enquiry from anywhere and anytime by just dialing the certain number. It will also be helpful for the college for gathering the information of the student related to the admission and storing the information in database.

IVR System has been a rearmost technology, each provides the foundation for furnishing accessible new IVRS services for guests as well as reduced functional costs, better client satisfaction and retention increase return on investment and a stronger request presence for the IVRS services provider. A speech interface can give frequently more flexible navigation labors that are less complex and more hierarchical touch tone menu options.

IVRS may be used in organizations to know about various departments, mode of working and levels of control. Hardware circuitry of IVRS is a very compact and it can be used as a card in computer. By the wide spread of internet it is possible to know the information from anywhere in the world with the advanced features of Interactive Voice Response System.

Now a days, everything needs to be done from the comfort of home or office. For this purpose application is prepared so that they can be easily accessed through computers. In the same way our project's aim is to provide an entire information to the user at the tip of their fingers.

5.2 FUTURE SCOPE

This project aims to solve the problem by creating an IVR System for College Assistance. The concept of Interactive Voice Response System can be used in various colleges like Engineering, medical, pharmacy, arts and many more, as the colleges not only need to be fast and responsive, but also need to provide students with an easily accessible information by sending the SMS with an link of information.

In future, the concept of IVR System can be used in different transport departments like Bus transport, Metro rail, Railways and Airports as the transport companies not only need to be quick and responsive, but also need to provide customer with an easily accessible detail information system providing:

- Information Enquiry
- Schedule Enquiry
- Tele- ticketing Systems

So, in near future, all the detail information regarding routes, timings etc. will be known through the IVR System. Also, this concept may be implemented in Cinema halls and Multiplexes where the caller will get to know the timings of his favourite movies as well as they can book his tickets through this system.

The above ideas can be further extended by taking speech as a input and then recognizing it using Speech Recognition technique. Even the detail information can be provided by voice by using Text-to-Speech conversion technique or by pre-recorded voice. User may have facility to make a Call or just send an SMS with Register number and Password to get details. Facility can be made such that user selects the response mode i.e. through SMS or Voice.

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APPENDIX

APPENDIX A: Course Detail Sheet for project

Course Detail Sheet

Programme: 2015			Class: B.E(E&TC)				AY 2021-22 Sem. I&II			
Course Code: 404188 & 404195			Course Project Phase-I and Project Phase-II							
Course Teacher: Project Guides			Department: Electronics and Telecommunication Engineering							
Teaching Scheme			Examination Scheme							
Theory	Practical	Tutorial	Theory			Lab				
(hrs/week)	(hrs/week)	(hrs/week)	Online / Insem	Endsem	Sessional	Term Work	Practical	Oral		
----	----	2+6 hrs	---	---	---	150	---	50+50		
Abstract: By learning this subject students will be able to Identify complex problem and define the methodology to solve the problem. Construct, analyze and approach problem solution as a team, plan, and co-ordinate and control the complex and diverse activities in project. Design appropriately using a modular construction approach to solve the problem as per specifications and implement the selected methodology to solve the problem by selecting the correct hardware according to specifications and software for simulation and programming and develop leadership skills by aligning with the objective of the project and lead the team towards its goal										
Prerequisite: All Subjects of E&TC Engineering										

Delivery Methods (DM)

Chalk & Talk	ICT Tools	Group Discussion	Industrial/ Field Visit	Expert Talk	Survey	Mini project	Lab
--	√	--	--	--	√	--	--

Course Outcomes (COs)

Course Outcome	After successful completion of course students will be able to
CO1	Define, analyze and solve complex real life problem.
CO2	Work in collaborative team as a member or leader.
CO3	Apply project management techniques.
CO4	Identify and apply appropriate tools.
CO5	Communicate effectively in verbal and written form.
CO6	Imbibe ethical practices.

Learning objective for CO1**Students will be able to:**

- | | |
|---|--|
| 1 | Identify specification of the problem. |
| 2 | Structure the problem. |
| 3 | Identify the appropriate methodology to solve the problem. |
| 4 | Define the methodology to solve the problem. |

Learning objective for CO2**Students will be able to:**

- | | |
|---|---|
| 1 | Adapt the vital skills of compromise and collaboration. |
| 2 | Construct , analyzes and approach problem solution as a team |
| 3 | Fully understand the role of each individual in a group to accomplish the goal. |
| 4 | Develop leadership skills by aligning with the objective of the project and lead the team towards its goal. |

Learning objective for CO3**Students will be able to**

- | | |
|---|---|
| 1 | Plan, co-ordinate and control the complex and diverse activities in project |
| 2 | Predict any problems and find solution for it |
| 3 | Plan the progress to result in total completion of the project. |

Learning objective for CO4**Students will be able to**

- | | |
|---|--|
| 1 | Design appropriately using a modular construction approach to solve the problem as per specifications. |
| 2 | Implement the selected methodology to solve the problem. |
| 3 | Select the correct hardware according to specifications. |
| 4 | Select the correct software for simulation and programming. |
| 5 | Validate the result and draw conclusion. |

Learning objective for CO5**Students will be able to**

- | | |
|---|---|
| 1 | Present the work done by proper documentation |
| 2 | Present paper in national / international conferences, project exhibitions & competitions |

Learning objective for CO6**Students will**

- | | |
|---|--|
| 1 | Develop professional practice. |
| 2 | Recognize how to do the project to its best. |
| 3 | Develop ethical Practices. |

Mapping of Course Objectives to Course Outcomes:

Course Objective	Course Outcomes					
	1.	2.	3.	4.	5.	6.
C-I	•					
C-II		•				
C-III			•			

C-IV					•		
C-V						•	
C-VI							•

Program Outcomes (POs):

Engineering Graduates will be able to:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSO):

1. Analyze and design electronic systems for hybrid engineering application.
2. Implement functional blocks of hardware, software or hardware-software co-design for signal processing and communication applications.

Mapping of Course Outcome (CO) with
Program Outcome (PO) and Program Specific Outcome (PSO)
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)
If there is no correlation, put “-“

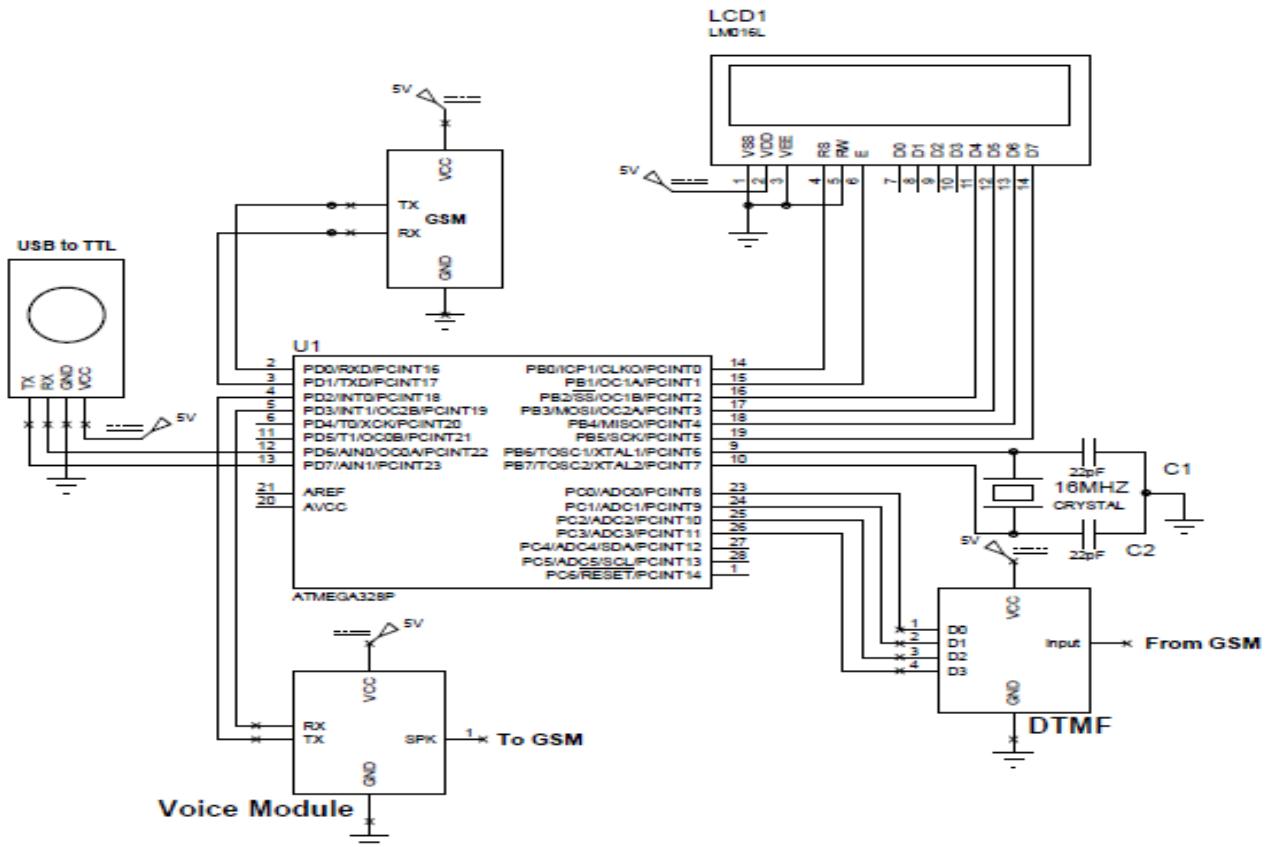
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO404188.1 & CO404195.1	3	3	3	3	-	2	2	-	-	-	-	-	3	3
CO404188.2 & CO404195.2	-	-	-	-	-	-	-	-	3	-	2	-	-	-
CO404188.3 & CO404195.3	-	-	-	-	-	-	-	-	-	-	3	2	-	-
CO404188.4 & CO404195.4	2	2	-	3	3	-	-	-	-	-	-	2	-	-
CO404188.5 & CO404195.5	-	-	-	-	-	-	-	-	-	3	-	-	-	-
CO404188.6 & CO404195.6	-	-	-	-	-	-	-	3	-	-	-	-	-	-
Average	2.5	2.5	3	3	3	2	-	3	3	3	2.5	2	3	3

Course-PO matrix

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
404188 & 404195	2.5	2.5	3	3	3	2	-	3	3	3	2.5	2	3	3

Note: Pos mapping level in “*” will be defined my respective guide based on the project topic

APPENDIX B: Circuit Schematic



APPENDIX C: Bill of Material

Components	Cost
Atmega328 P	225
Crystal	120
Bridge rectifier 4 x diode 1N4007	20
Capacitor 1000 pf and 100 pf	20
Voltage regulator 7805	20
Resister 1k ohm and 10k ohm	20
Led	12
16 x 2 LCD display	220
Box connector	30
Reset Button	10
DTMF	220
GSM	480
USB to TTL	150
Voice module	500
TOTAL	2047

APPENDIX D: Certificate of Paper Presentation/Project Competition.



**K. K. WAGH EDUCATION SOCIETY'S
K. K. Wagh Institute of Engineering Education and Research**

CERTIFICATE OF PARTICIPATION

This is to certify that Mr./Ms. Kartikey Bandre had participated for the **Project Competition** in the event **Telekinesis**, organised by E&TC Department on May 5th, 2022 at K. K. Wagh Institute of Engineering Education and Research, Nashik.

Dr. S. A. Ugale (Patil)

UG Co-Ordinator
K.K.W.I.E.E.R, Nashik

Dr. D. M. Chandwadkar

Head of Department
K.K.W.I.E.E.R, Nashik

Dr. K. N. Nandurkar

Principal
K.K.W.I.E.E.R, Nashik



K. K. WAGH EDUCATION SOCIETY'S
K. K. Wagh Institute of Engineering Education and Research

CERTIFICATE

OF PARTICIPATION

This is to certify that Mr./Ms. Anuj Kabra had participated for the **Project Competition** in the event **Telekinesis**, organised by E&TC Department on May 5th, 2022 at K. K. Wagh Institute of Engineering Education and Research, Nashik.

Dr. S. A. Ugale (Patil)

UG Co-Ordinator
K.K.W.I.E.E.R., Nashik

Dr. D. M. Chandwadkar

Head of Department
K.K.W.I.E.E.R., Nashik

Dr. K. N. Nandurkar

Principal
K.K.W.I.E.E.R., Nashik



K. K. WAGH EDUCATION SOCIETY'S
K. K. Wagh Institute of Engineering Education and Research

CERTIFICATE

OF PARTICIPATION

This is to certify that Mr./Ms. Atharvaa Savale had participated for the **Project Competition** in the event **Telekinesis**, organised by E&TC Department on May 5th, 2022 at K. K. Wagh Institute of Engineering Education and Research, Nashik.

Dr. S. A. Ugale (Patil)
UG Co-ordinator
K.K.W.I.E.E.R., Nashik

Dr. D. M. Chandwadkar
Head of Department
K.K.W.I.E.E.R., Nashik

Dr. K. N. Nandurkar
Principal
K.K.W.I.E.E.R., Nashik

APPENDIX E: Report for Plagiarism Check

Plagiarism Certificate

This is to certify that the project work titled “IMPLEMENTATION OF IVR SYSTEM FOR COLLEGE ASSISTANCE”, is a part of project work carried out by “Kartikey Sunil Bandre, Anuj Rajesh Kabra and Atharvaa Hemant Savale” under the guidance of Prof. R.V.Chothe at K. K. Wagh Institute of Engineering Education and Research, Nashik, in the partial fulfillment of the requirements for Bachelor’s degree in Electronics and Telecommunication Engineering.

To the best of our knowledge, the work included in this report is an original work carried out by us independently. The percentage of Uniqueness is 90.8%. The results of the project work in part or whole have not been submitted to any other Institute/University for the award of any degree.

1. Kartikey Sunil Bandre
2. Anuj Rajesh Kabra
3. Atharvaa Hemant Savale

Name & Signature of the student

RESULTS

Completed: 100% Checked | Plagiarism: 0% | Unique: 100%

Sentence Wise Result | Document View | Matched Sources

Unique	Description
Unique	An IVR application offers prerecorded voice responses for suitable conditions, keypad sign good judg...
Unique	Using pc telephony integration (CTI), IVR structures can hand off a call to a man or women who can ...
Unique	IVR systems also utilizes dual-tone multi-frequency (DTMF) signals as a line of communication betwe...
Unique	The computer uses a telephony board or card to recognize DTMF alerts.

Activate Windows
Go to Settings to activate Windows.

Plagiarism for Introduction

RESULTS

Completed: 100% Checked | Plagiarism: 0% | Unique: 100%

Sentence Wise Result | Document View | Matched Sources

Unique	Description
Unique	There are many successful examples where businesses have improved their operations and increa...
Unique	An IVR system provides users with round-the-clock access to variables rather than static information.
Unique	The use of a well-designed IVR system can help in reducing the number of calls that are to be ans...
Unique	At the same time, it increases customer satisfaction, as the customers are not restricted to the hou...
Unique	They can call in 24 hours a day, seven days a week. I2!

Learn a language without even trying.
Learn Languages While Browsing

Plagiarism for Objective of Project

RESULTS

Completed: 100% Checked

11% Plagiarism 89% Unique

Sentence Wise Result Document View Matched Sources

Plagiarized Interactive Voice Response System is an automated system which interacts with the users ... Compare

Unique IVR Systems provide an efficient way for Institutions, Health Care, Telecommunication, Banking an...

Unique As human useful resource isn't always value-powerful and non-to be had always, this device comp...

Unique An IVR System accepts combination of telephone input and touch-tone keypad selection and provi...

Plagiarism for Conclusion

RESULTS

Completed: 100% Checked

0% Plagiarism 100% Unique

Sentence Wise Result Document View Matched Sources

Unique Interactive Voice Response (IVR) is an automatic telephony system that interacts with callers, gather...

Unique An IVR system (IVRS) accepts a aggregate of voice smartphone enter and contact-tone keypad selec...

Unique IVR systems can encompass telephony device, software program packages, a database and a assisti...

Plagiarism for Future Scope

APPENDIX F: Data Sheets

8-bit AVR Microcontroller with 32K Bytes In-System Programmable Flash

DATASHEET

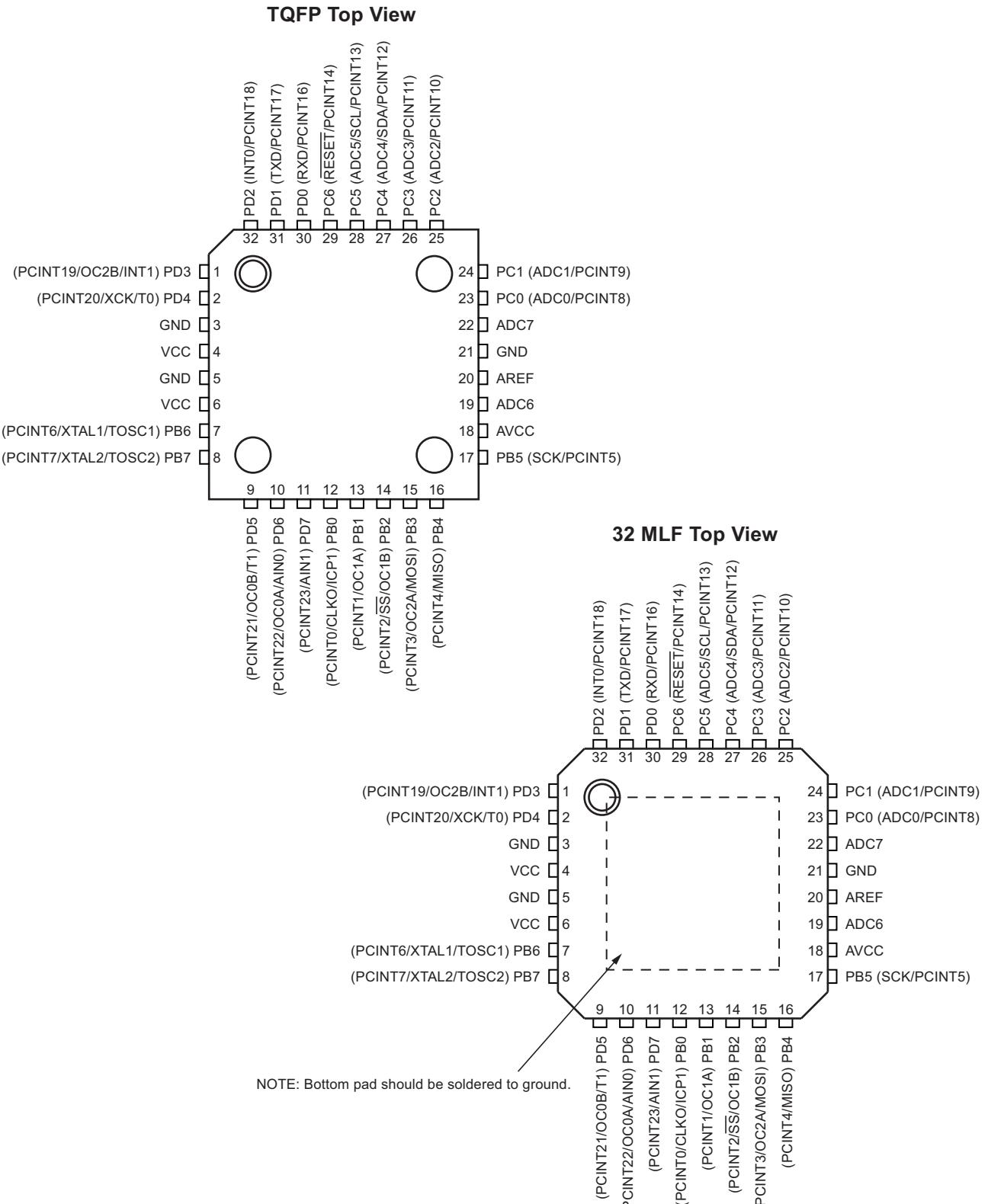
Features

- High performance, low power AVR® 8-bit microcontroller
- Advanced RISC architecture
 - 131 powerful instructions – most single clock cycle execution
 - 32 × 8 general purpose working registers
 - Fully static operation
 - Up to 16MIPS throughput at 16MHz
 - On-chip 2-cycle multiplier
- High endurance non-volatile memory segments
 - 32K bytes of in-system self-programmable flash program memory
 - 1Kbytes EEPROM
 - 2Kbytes internal SRAM
 - Write/erase cycles: 10,000 flash/100,000 EEPROM
 - Optional boot code section with independent lock bits
 - In-system programming by on-chip boot program
 - True read-while-write operation
 - Programming lock for software security
- Peripheral features
 - Two 8-bit Timer/Counters with separate prescaler and compare mode
 - One 16-bit Timer/Counter with separate prescaler, compare mode, and capture mode
 - Real time counter with separate oscillator
 - Six PWM channels
 - 8-channel 10-bit ADC in TQFP and QFN/MLF package
 - Temperature measurement
 - Programmable serial USART
 - Master/slave SPI serial interface
 - Byte-oriented 2-wire serial interface (Phillips I²C compatible)
 - Programmable watchdog timer with separate on-chip oscillator
 - On-chip analog comparator
 - Interrupt and wake-up on pin change
- Special microcontroller features
 - Power-on reset and programmable brown-out detection
 - Internal calibrated oscillator
 - External and internal interrupt sources
 - Six sleep modes: Idle, ADC noise reduction, power-save, power-down, standby, and extended standby

- I/O and packages
 - 23 programmable I/O lines
 - 32-lead TQFP, and 32-pad QFN/MLF
- Operating voltage:
 - 2.7V to 5.5V for ATmega328P
- Temperature range:
 - Automotive temperature range: -40°C to +125°C
- Speed grade:
 - 0 to 8MHz at 2.7 to 5.5V (automotive temperature range: -40°C to +125°C)
 - 0 to 16MHz at 4.5 to 5.5V (automotive temperature range: -40°C to +125°C)
- Low power consumption
 - Active mode: 1.5mA at 3V - 4MHz
 - Power-down mode: 1µA at 3V

1. Pin Configurations

Figure 1-1. Pinout



1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB7:0) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting oscillator amplifier.

If the internal calibrated RC oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of port B are elaborated in [Section 13.3.1 “Alternate Functions of Port B” on page 65](#) and [Section 8. “System Clock and Clock Options” on page 24](#).

1.1.4 Port C (PC5:0)

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC5..0 output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

1.1.5 PC6/RESET

If the RSTDISBL fuse is programmed, PC6 is used as an input pin. If the RSTDISBL fuse is unprogrammed, PC6 is used as a reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [Table 28-4 on page 261](#). Shorter pulses are not guaranteed to generate a reset.

The various special features of port C are elaborated in [Section 13.3.2 “Alternate Functions of Port C” on page 68](#).

1.1.6 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port D pins that are externally pulled low will source current if the pull-up resistors are activated. The port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The various special features of port D are elaborated in [Section 13.3.3 “Alternate Functions of Port D” on page 70](#).

1.1.7 AV_{CC}

AV_{CC} is the supply voltage pin for the A/D converter, PC3:0, and ADC7:6. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC6..4 use digital supply voltage, V_{CC}.

1.1.8 AREF

AREF is the analog reference pin for the A/D converter.

1.1.9 ADC7:6 (TQFP and QFN/MLF Package Only)

In the TQFP and QFN/MLF package, ADC7:6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

1.2 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of actual ATmega328P AVR® microcontrollers manufactured on the typical process technology. automotive min and max values are based on characterization of actual ATmega328P AVR microcontrollers manufactured on the whole process excursion (corner run).

1.3 Automotive Quality Grade

The ATmega328P have been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. This data sheet contains limit values extracted from the results of extensive characterization (temperature and voltage). The quality and reliability of the ATmega328P have been verified during regular product qualification as per AEC-Q100 grade 1. As indicated in the ordering information paragraph, the products are available in only one temperature.

Table 1-1. Temperature Grade Identification for Automotive Products

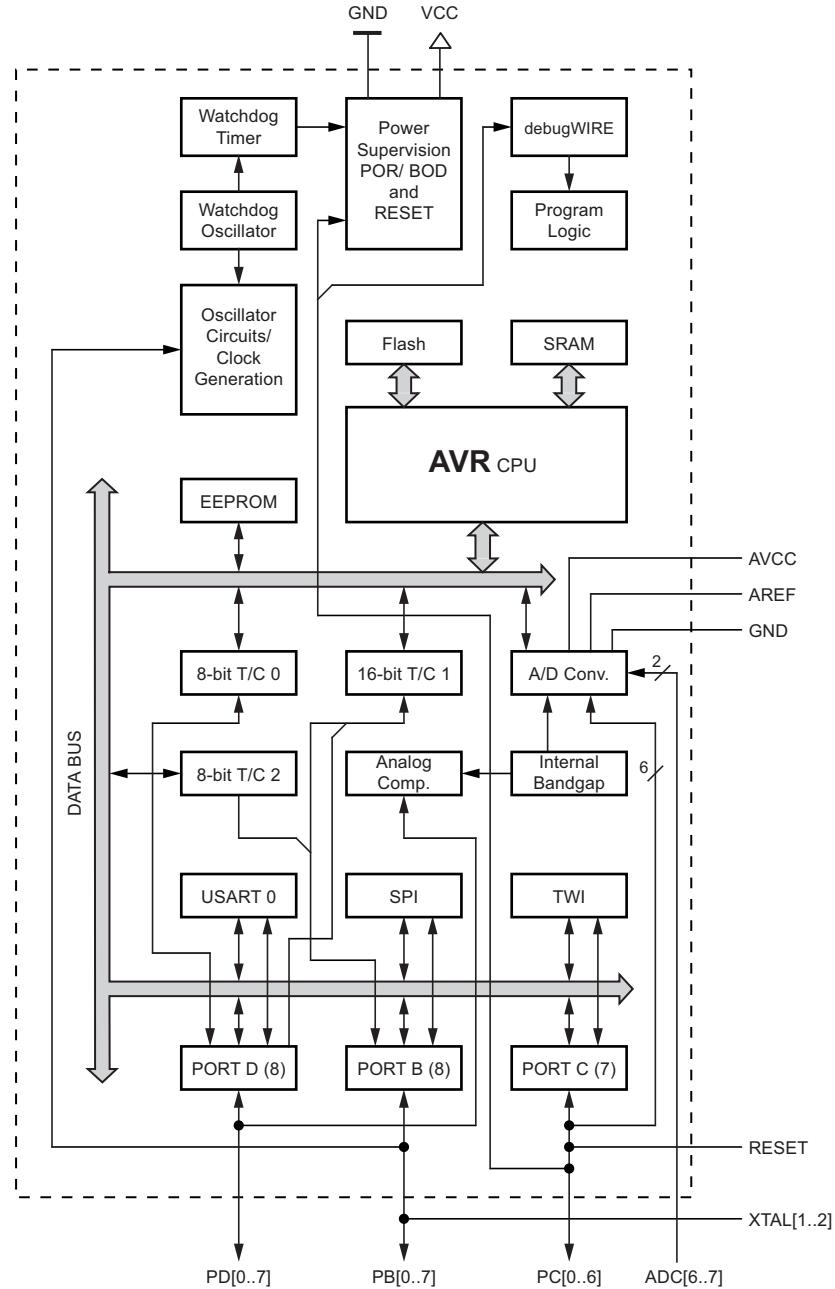
Temperature	Temperature Identifier	Comments
-40°C; +125°C	Z	Full automotive temperature range

2. Overview

The Atmel® ATmega328P is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega328P achieves throughputs approaching 1MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel® ATmega328P provides the following features: 32K bytes of in-system programmable flash with read-while-write capabilities, 1K bytes EEPROM, 2K bytes SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte-oriented 2-wire serial interface, an SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and QFN/MLF packages), a programmable watchdog timer with internal oscillator, and five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire serial interface, SPI port, and interrupt system to continue functioning. The power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset. In power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC noise reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel high density non-volatile memory technology. The on-chip ISP flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional non-volatile memory programmer, or by an on-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the application flash memory. Software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8-bit RISC CPU with in-system self-programmable flash on a monolithic chip, the Atmel ATmega328P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega328P AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

4. Data Retention

Reliability qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

5. About Code Examples

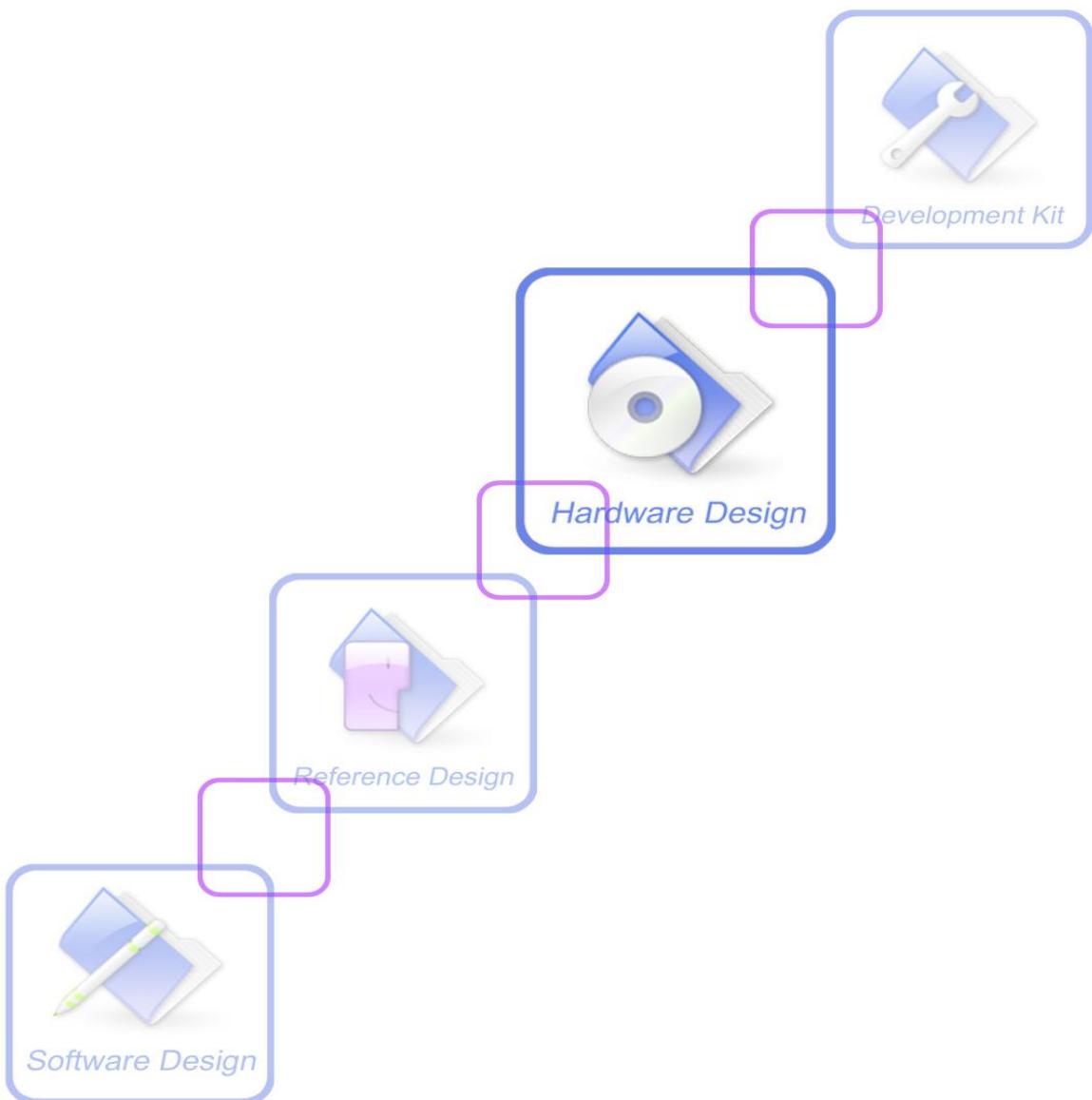
This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.



A company of SIM Tech

SIM800A_Hardware Design_V1.02



1 Introduction

This document describes SIM800A hardware interface in great detail.

This document can help users understand both the interface specifications and the electrical and mechanical details of SIM800A quickly. With the help of this document and other SIM800A application notes or user guide, users can use SIM800A to design various applications quickly.

2 SIM800A Overview

Designed for global market, SIM800A is a Dual-band GSM/GPRS module that works on frequencies EGSM 900MHz and DCS 1800MHz . SIM800A features GPRS multi-slot class 12/ class 10 (optional) and supports the GPRS coding schemes CS-1, CS-2, CS-3 and CS-4.

With a tiny configuration of 24*24*3mm, SIM800A can meet almost all the space requirements in users' applications, such as smart phone, PDA and other mobile devices.

SIM800A is a SMT package with 68 pads, and provides hardware interfaces as below:

- One full function UART port
- One USB port for debugging and firmware upgrading
- Audio channel which includes a microphone input and a receiver output
- One SIM card interface
- Support up to 4*5 Keypads
- One display interface
- One I2C master interface for peripheral management
- Programmable general purpose input and output
- Two PWM output
- One ADC input
- Bluetooth antenna interface
- GSM antenna interface

SIM800A is designed with power saving technique so that the current consumption is as low as 0.55mA in sleep mode.

SIM800A integrates TCP/IP protocol and extended TCP/IP AT commands which are very useful for data transfer applications. For details about TCP/IP applications, please refer to *document^[2]*.

2.1 SIM800A Key Features

Table 1: SIM800A key features

Feature	Implementation
Power supply	3.4V ~ 4.4V
Power saving	Typical power consumption in sleep mode is 0.55mA (AT+CFUN=0)

Frequency bands	<ul style="list-style-type: none"> ● SIM800A Dual-band: EGSM 900, DCS 1800 ● SIM800A can search the 4 frequency bands automatically. The frequency bands also can be set by AT command “AT+CBAND”. For details, please refer to document ^[1] ● Compliant to GSM Phase 2/2+
Transmitting power	<ul style="list-style-type: none"> ● Class 4 (2W) at EGSM 900 ● Class 1 (1W) at DCS 1800
GPRS connectivity	<ul style="list-style-type: none"> ● GPRS multi-slot class 12 (default) ● GPRS multi-slot class 1~12 (option)
Temperature range	<ul style="list-style-type: none"> ● Operation temperature: -40 °C ~ +85 °C ● Storage temperature -45 °C ~ +90 °C
Data GPRS	<ul style="list-style-type: none"> ● GPRS data downlink transfer: max. 85.6 kbps ● GPRS data uplink transfer: max. 85.6 kbps ● Coding scheme: CS-1, CS-2, CS-3 and CS-4 ● Integrate the TCP/IP protocol. ● Support Packet Broadcast Control Channel (PBCCH)
USSD	<ul style="list-style-type: none"> ● Unstructured Supplementary Services Data (USSD) support
SMS	<ul style="list-style-type: none"> ● MT, MO, CB, Text and PDU mode ● SMS storage: SIM card
FAX	Group 3 Class 1
SIM interface	Support SIM card: 1.8V, 3V
External antenna	Antenna pad
Audio features	<p>Speech codec modes:</p> <ul style="list-style-type: none"> ● Half Rate (ETSI 06.20) ● Full Rate (ETSI 06.10) ● Enhanced Full Rate (ETSI 06.50 / 06.60 / 06.80) ● Adaptive multi rate (AMR) ● Echo Cancellation ● Noise Suppression
Serial port and USB	<p>Serial port:</p> <ul style="list-style-type: none"> ● Full modem serial port ● Can be used for AT commands or data stream ● Support RTS/CTS hardware handshake ● Comply with GSM 07.10 Multiplexer Protocol ● Support auto baud detect from 1200 bps to 115200bps <p>USB:</p> <ul style="list-style-type: none"> ● For debugging and upgrading firmware
Phonebook management	Support phonebook types: SM, FD, LD, RC, ON, MC.
SIM application toolkit	GSM 11.14 Release 99
Real time clock	Support RTC
Physical characteristics	<p>Size: 24*24*3mm</p> <p>Weight: 3.1g</p>
Firmware upgrading	Upgrade firmware via USB port

Table 2: Coding schemes and maximum net data rates over air interface

Coding scheme	1 timeslot	2 timeslot	4 timeslot
CS-1	9.05kbps	18.1kbps	36.2kbps
CS-2	13.4kbps	26.8kbps	53.6kbps
CS-3	15.6kbps	31.2kbps	62.4kbps
CS-4	21.4kbps	42.8kbps	85.6kbps

2.2 Operating Modes

The table below summarizes the various operating modes of SIM800A.

Table 3: Overview of operating modes

Mode	Function
Normal operation	GSM/GPRS SLEEP Module will automatically go into sleep mode when the sleep mode is enabled and there is no on air or hardware interrupt (such as GPIO interrupt or data on serial port). In this case, the current consumption of module will reduce to the minimal level, and the module can still receive paging message and SMS.
	GSM IDLE Software is active. Module has been registered to the GSM network and is ready to communicate.
	GSM TALK Connection between two subscribers is in progress. In this case, the power consumption depends on network settings such as DTX off/on, FR/EFR/HR, hopping sequences, antenna.
	GPRS STANDBY Module is ready for GPRS data transfer, but no data is currently sent or received. In this case, power consumption depends on network settings and GPRS configuration.
	GPRS DATA There is GPRS data transfer (PPP or TCP or UDP) in progress. In this case, power consumption is related with network settings (e.g. power control level), uplink/downlink data rates and GPRS configuration (e.g. used multi-slot settings).
Power off	Normal power off by sending the AT command “AT+CPOWD=1” or using the PWRKEY. The power management unit shuts down the power supply for the baseband part of the module, and only the power supply for the RTC is remained. Software is not active. The serial port is not accessible. Power supply (connected to VBAT) remains applied.
Minimum functionality mode	AT command “AT+CFUN” can be used to set the module to a minimum functionality mode. In this mode, the RF function and SIM card function can be disabled, but the serial port is still accessible. The power consumption in this mode is lower than normal mode.

2.3 SIM800A Functional Diagram

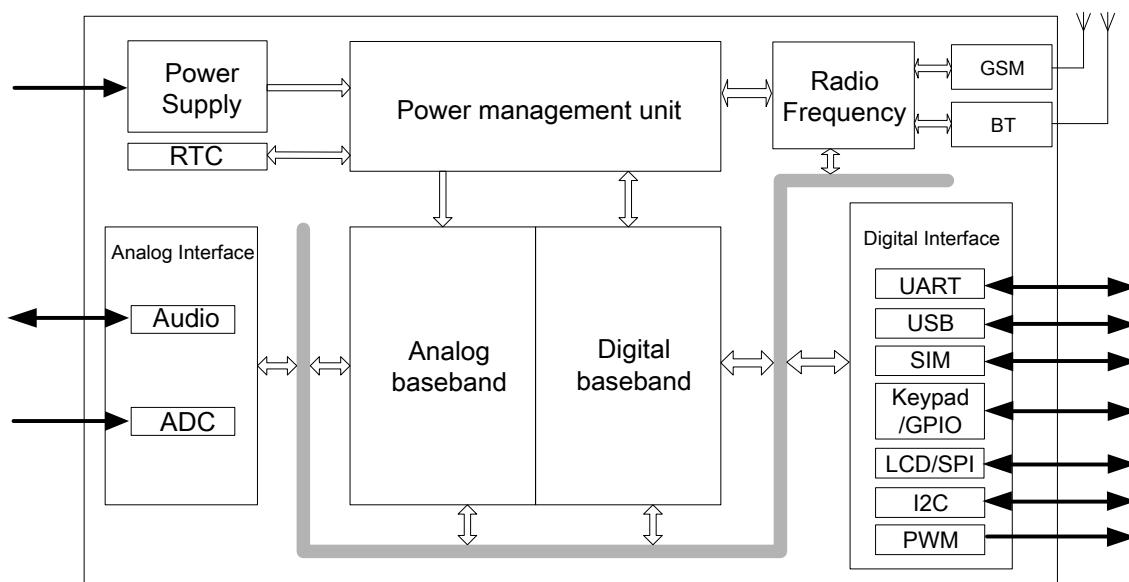


Figure 1: SIM800A functional diagram

3 Package Information

3.1 Pin out Diagram

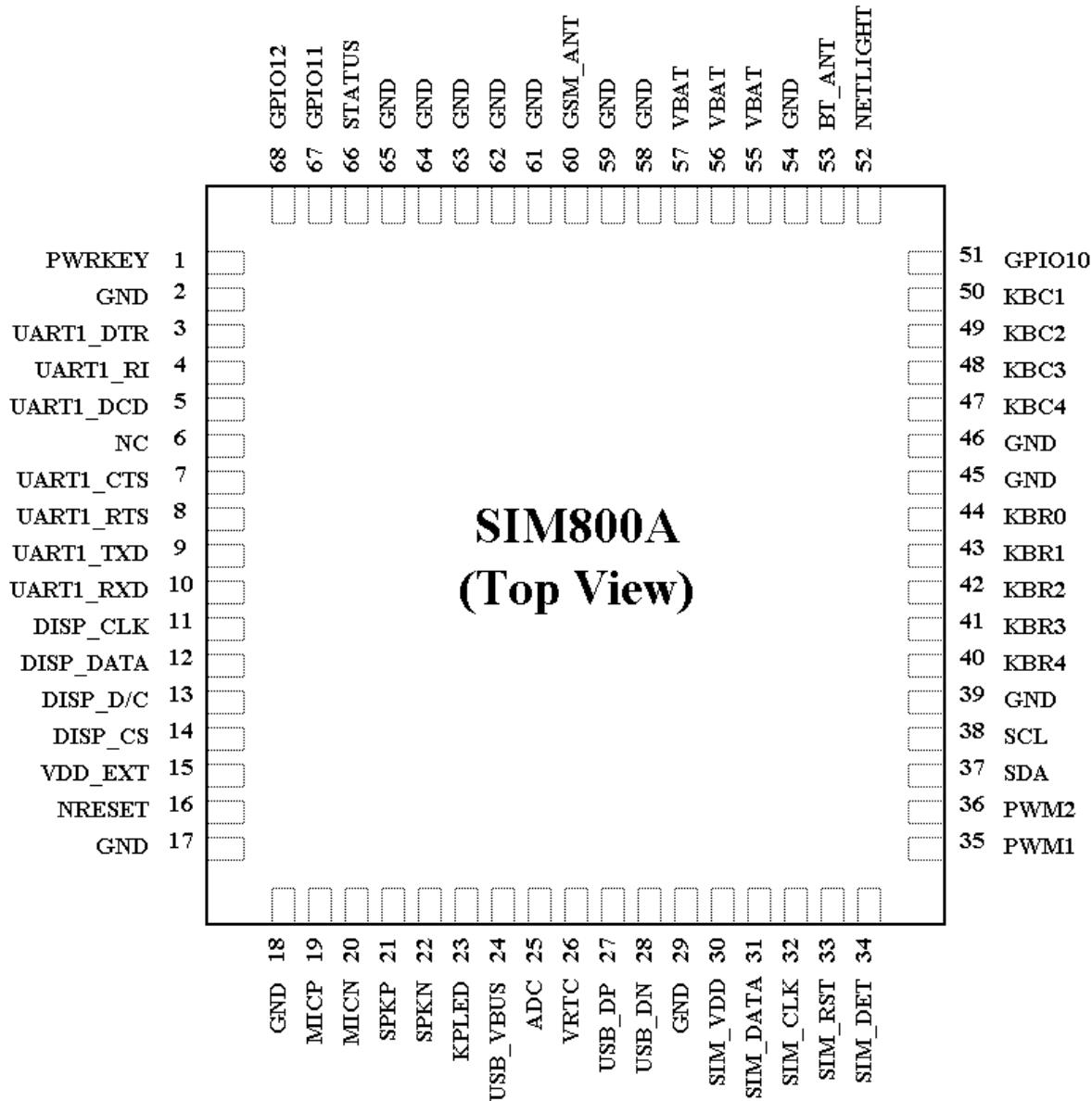


Figure 2: SIM800A pin out diagram (Top view)

3.2 Pin Description

Table 4: Pin description

Pin name	Pin number	I/O	Description	Comment
Power supply				
VBAT	55,56,57	I	Power supply	
VRTC	26	I/O	Power supply for RTC	It is recommended to connect with a battery or a capacitor (e.g. 4.7uF)
VDD_EXT	15	O	2.8V output power supply	Left floating if unused
GND	2,17,18,29, 39,45,46,54, 58,59,61,62, 63,64,65	-	Ground	
Power on/off				
PWRKEY	1	I	PWRKEY should be pulled low more than 1 second then released to power on/off the module.	Pulled up internally already
Audio interfaces				
MICP	19	I	Differential audio input	
MICN	20	I		
SPKP	21	O	Differential audio output	Left floating if unused
SPKN	22	O		
Status				
STATUS	66	O	Power on status indication	
NETLIGHT	52	O	Network status indication	Left floating if unused
LCD interface				
DISP_CLK	11	O		
DISP_DATA	12	I/O		
DISP_D/C	13	O	Display interface	Left floating if unused
DISP_CS	14	O		
I2C interface				
SDA	37	I/O	I2C bus data	
SCL	38	O	I2C bus clock	Left floating if unused
Keypad interface / GPIO				
KBR0	44	I/O	keypad row 0	
KBR1	43		keypad row 1	
KBR2	42		keypad row 2	
KBR3	41		keypad row 3	
KBR4	40		keypad row 4	
KBC1	50		keypad column 1	Left floating if unused; KBC1 can not be pulled down during power on procedure

KBC2	49		keypad column 2	
KBC3	48		keypad column 3	
KBC4	47		keypad column 4	
GPIO10	51		GPIO10	Left floating if unused
GPIO11	67		GPIO11	Do not pull up externally; Left floating if unused
GPIO12	68		GPIO12	Left floating if unused
Serial port				
UART1_RXD	10	I	Receive data	Left floating if unused
UART1_TXD	9	O	Transmit data	
UART1_RTS	8	I	Request to send	
UART1_CTS	7	O	Clear to send	
UART1_DCD	5	O	Data carrier detect	
UART1_RI	4	O	Ring indicator	
UART1_DTR	3	I	Data terminal ready	
USB interface				
USB_VBUS	24	I	For debugging & upgrading firmware	Left floating if unused
USB_DP	27	I/O		
USB_DN	28	I/O		
SIM interface				
SIM_VDD	30	O	Voltage supply for SIM card. Support 1.8V or 3V SIM card	Should be protected against ESD with TVS diode
SIM_DATA	31	I/O	SIM data input/output	
SIM_CLK	32	O	SIM card clock	
SIM_RST	33	O	SIM card reset	
SIM_DET	34	I	SIM card detection	
ADC				
ADC	25	I	Input voltage range: 0V ~ 2.8V	Left floating if unused
External reset				
NRESET	16	I	Reset input, active low	Left floating if unused
Pulse width modulation(PWM)				
PWM1	35	O	Pulse-Width Modulation	Left floating if unused
PWM2	36	O	Pulse-Width Modulation	
RF interface				
GSM_ANT	60	I/O	GSM antenna	Impedance must be controlled to 50Ω
BT_ANT	53	I/O	Bluetooth antenna	Impedance must be controlled to 50Ω
Not connect				
KPLED	23	I	Sink current for keypad LED	Left floating if unused
NC	6	-	No connection	Do not connect

3.3 Package Dimensions

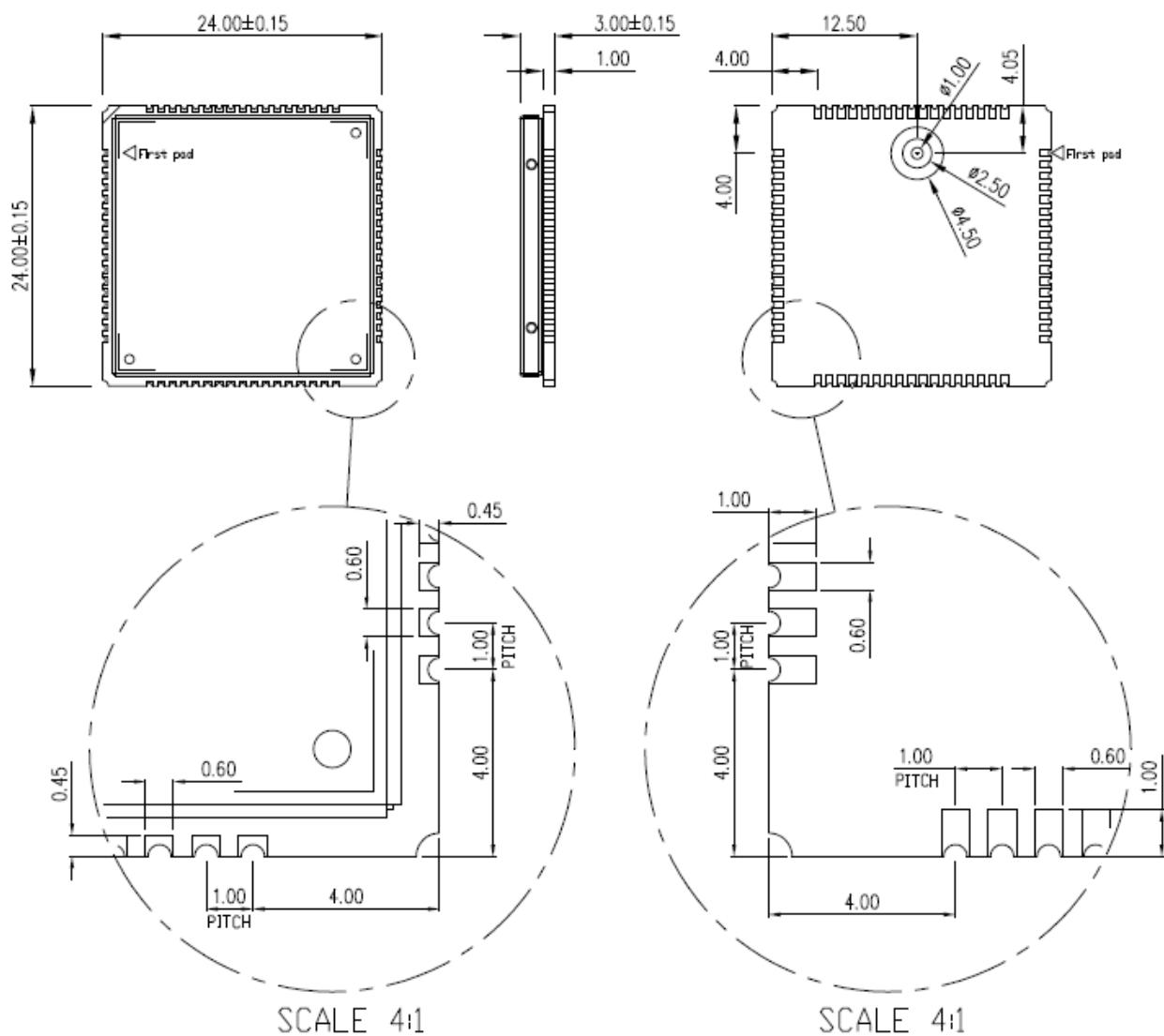


Figure 3: Dimensions of SIM800A (Unit: mm)

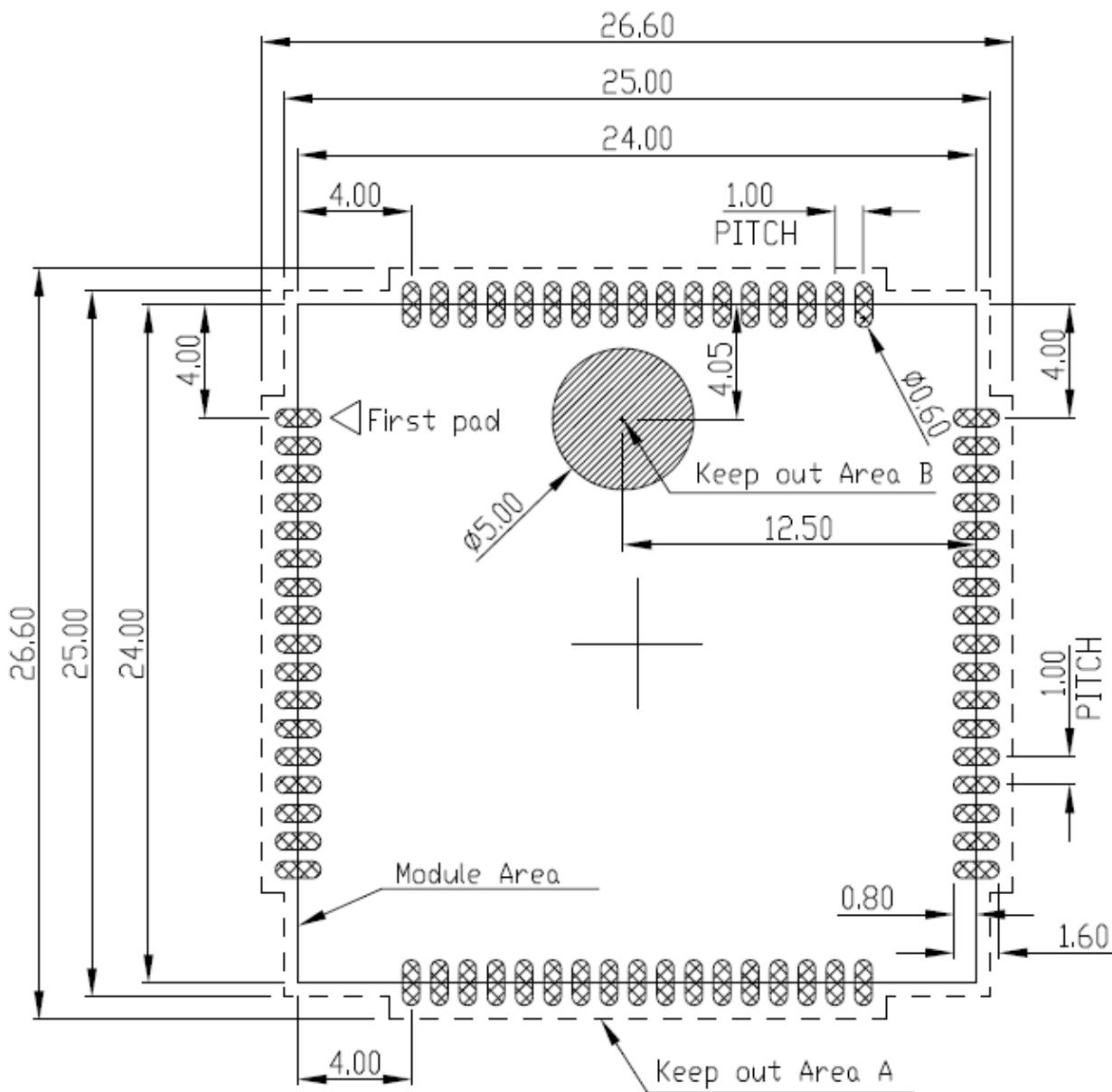


Figure 4: Recommended PCB footprint outline (Unit: mm)

Note: Keep copper out of area A. Do not place via in area B to avoid short circuit between the vias on customer board and the test points on the bottom side of the module.



MITEL[®]

ISO²-CMOS **MT8870D/MT8870D-1**

Integrated DTMF Receiver

Features

- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

ISSUE 3

May1995

Ordering Information

MT8870DE/DE-1	18 Pin Plastic DIP
MT8870DC/DC-1	18 Pin Ceramic DIP
MT8870DS/DS-1	18 Pin SOIC
MT8870DN/DN-1	20 Pin SSOP
MT8870DT/DT-1	20 Pin TSSOP

-40 °C to +85 °C

Applications

- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

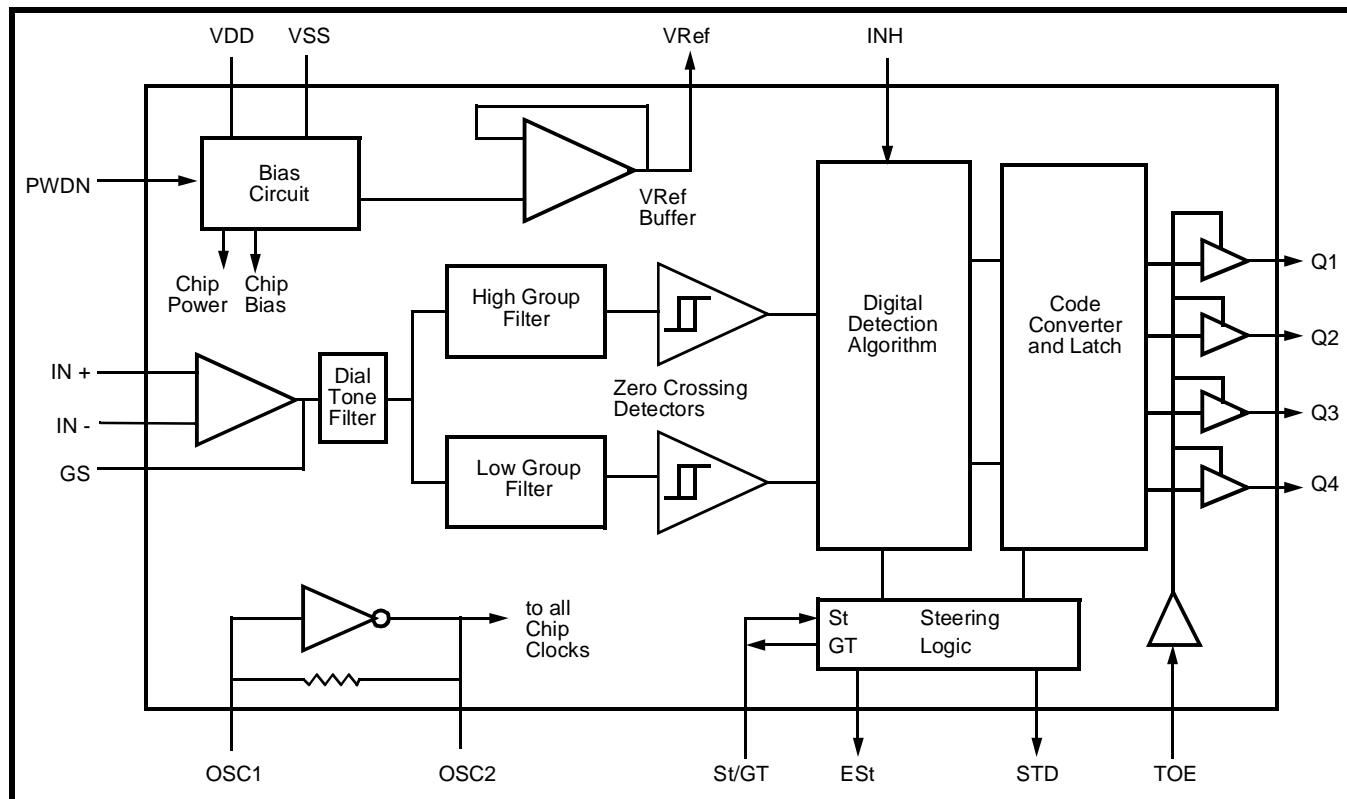


Figure 1 - Functional Block Diagram

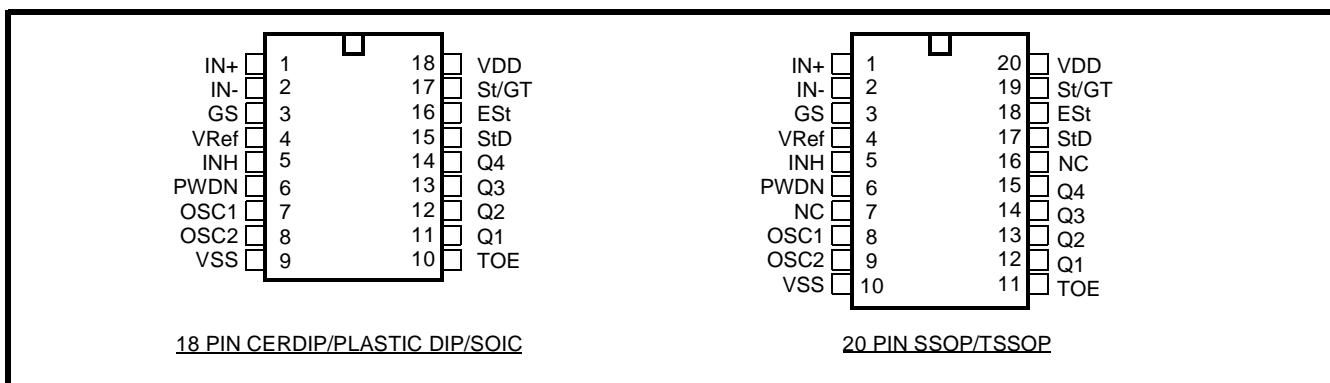


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
18	20		
1	1	IN+	Non-Inverting Op-Amp (Input).
2	2	IN-	Inverting Op-Amp (Input).
3	3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V _{Ref}	Reference Voltage (Output). Nominally V _{DD} /2 is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
5	5	INH	Inhibit (Input). Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	Power Down (Input). Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	Clock (Input).
8	9	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	V _{SS}	Ground (Input). 0V typical.
10	11	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	17	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V _{TSt} .
16	18	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	19	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V _{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V _{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	20	V _{DD}	Positive power supply (Input). +5V typical.
	7, 16	NC	No Connection.

Functional Description

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while

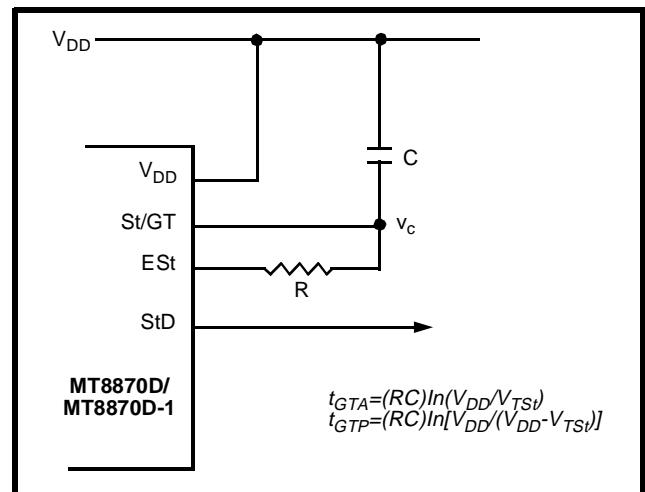


Figure 4 - Basic Steering Circuit

providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 4) to rise as the capacitor discharges. Provided signal

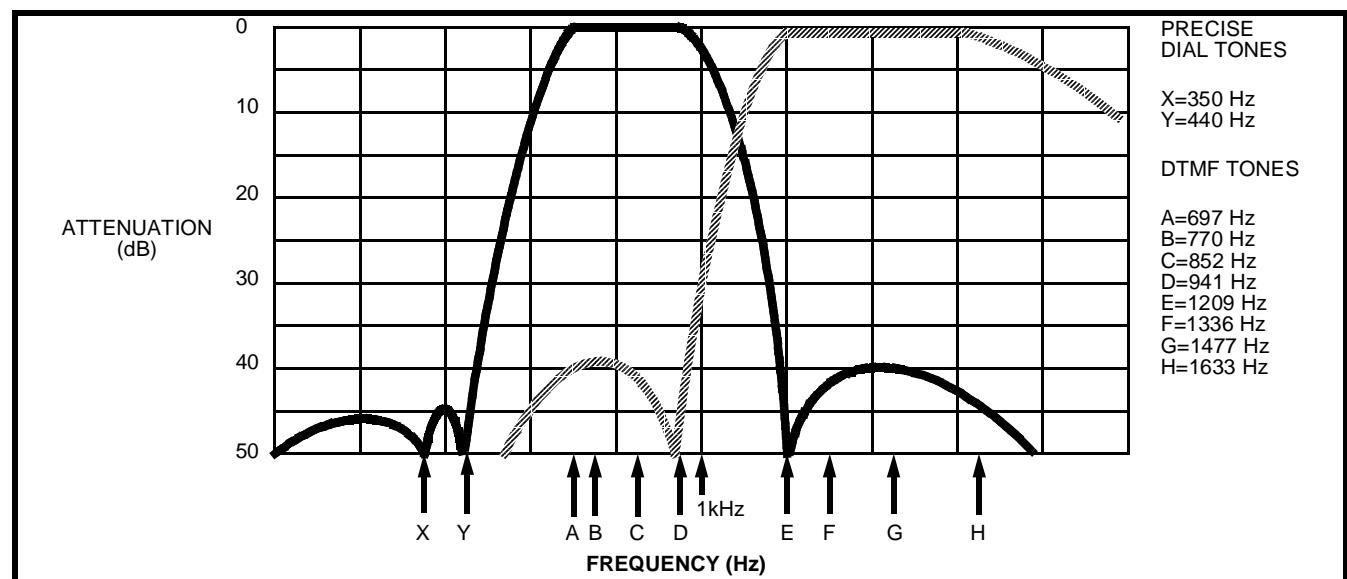


Figure 3 - Filter Response

condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSI}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives v_c to V_{DD} . GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 4 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see Figure 11) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μ F is

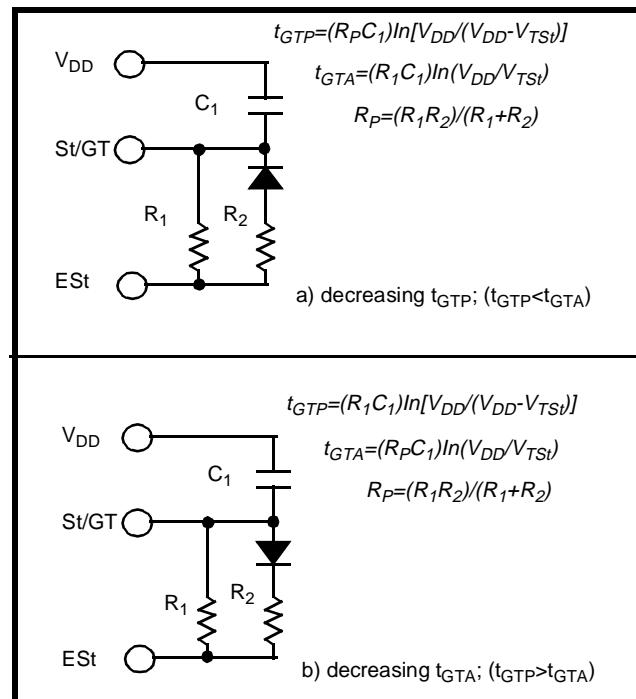


Figure 5 - Guard Time Adjustment

Digit	TOE	INH	ESt	Q ₄	Q ₃	Q ₂	Q ₁
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L				
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1. Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE

X = DON'T CARE

recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

Differential Input Configuration

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and V_{Ref} biasing the input at $\frac{1}{2}V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5 .

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several MT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

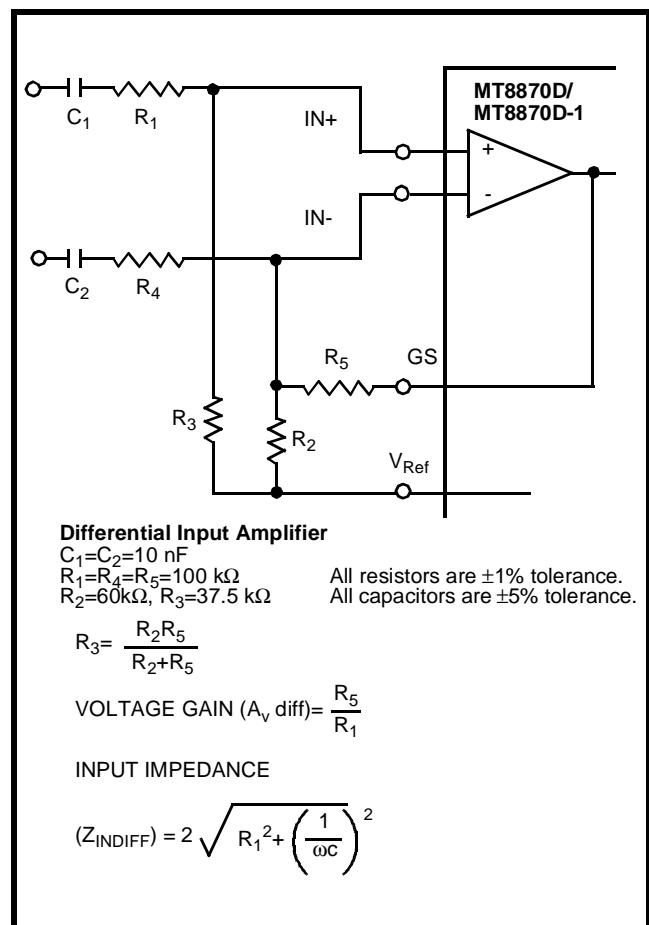


Figure 6 - Differential Input Configuration

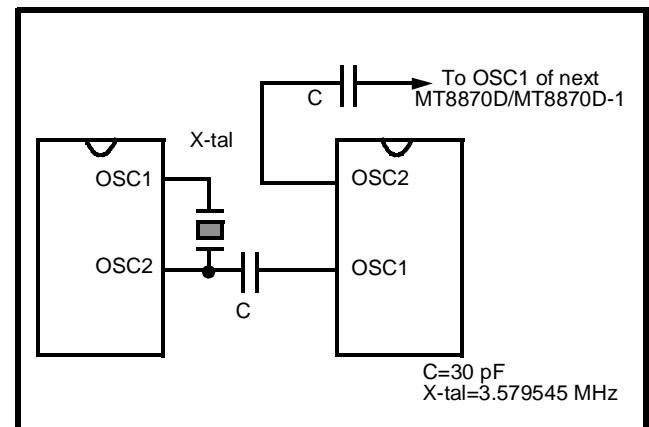


Figure 7 - Oscillator Connection

Parameter	Unit	Resonator
R1	Ohms	10.752
L1	mH	.432
C1	pF	4.984
C0	pF	37.915
Qm	-	896.37
Δf	%	$\pm 0.2\%$

Table 2. Recommended Resonator Specifications

Note: Qm=quality factor of RLC model, i.e., $1/2\pi f R_1 C_1$.

Applications

RECEIVER SYSTEM FOR BRITISH TELECOM SPEC POR 1151

The circuit shown in Fig. 9 illustrates the use of MT8870D-1 device in a typical receiver system. BT Spec defines the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing a suitable values of R_1 and R_2 to provide 3 dB attenuation, such that -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of MT8870D-1. As shown in the diagram, the component values of R_3 and C_2 are the guard time requirements when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 8.

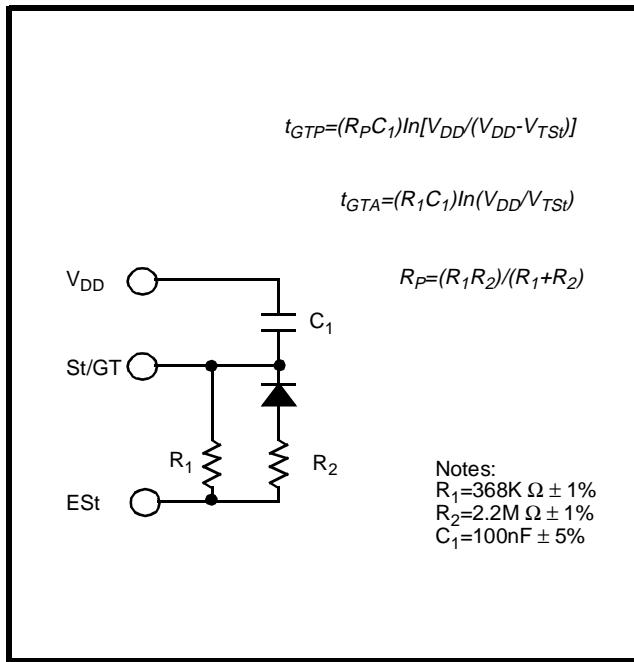


Figure 8 - Non-Symmetric Guard Time Circuit

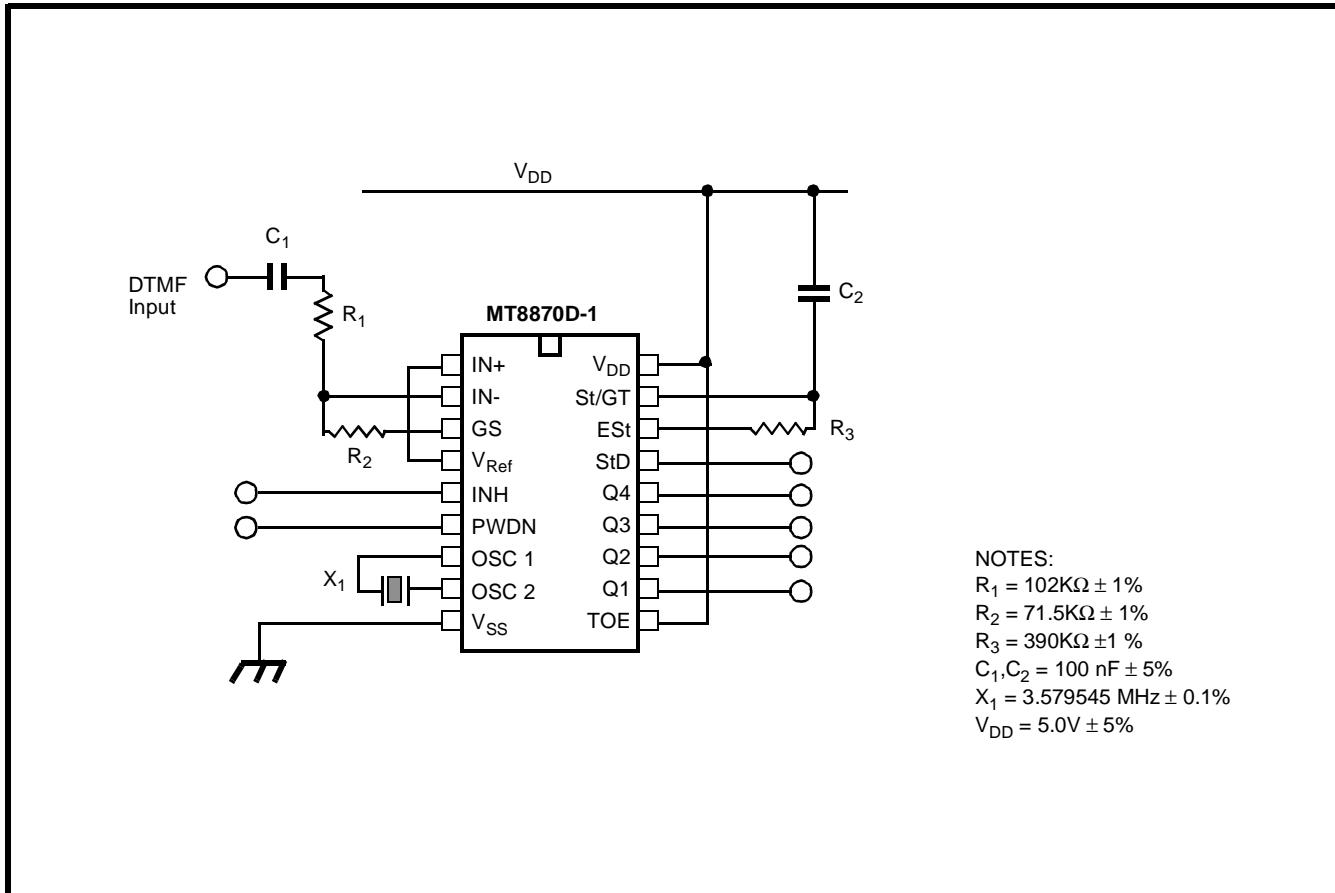


Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec

Absolute Maximum Ratings[†]

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V _{DD}		7	V
2	Voltage on any pin	V _I	V _{SS} -0.3	V _{DD} +0.3	V
3	Current at any pin (other than supply)	I _I		10	mA
4	Storage temperature	T _{STG}	-65	+150	°C
5	Package power dissipation	P _D		500	mW

[†] Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	DC Power Supply Voltage	V _{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T _O	-40		+85	°C	
3	Crystal/Clock Frequency	f _C		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δf _C		±0.1		%	

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	S U P P L Y	Standby supply current	I _{DDQ}		10	μA	PWDN=V _{DD}
2		Operating supply current	I _{DD}		3.0	mA	
3		Power consumption	P _O		15	mW	f _C =3.579545 MHz
4	I N P U T S	High level input	V _{IH}	3.5		V	V _{DD} =5.0V
5		Low level input voltage	V _{IL}		1.5	V	V _{DD} =5.0V
6		Input leakage current	I _{IH} /I _{IL}		0.1	μA	V _{IN} =V _{SS} or V _{DD}
7		Pull up (source) current	I _{SO}		7.5	μA	TOE (pin 10)=0, V _{DD} =5.0V
8		Pull down (sink) current	I _{SI}		15	μA	INH=5.0V, PWDN=5.0V, V _{DD} =5.0V
9		Input impedance (IN+, IN-)	R _{IN}		10	MΩ	@ 1 kHz
10		Steering threshold voltage	V _{TSt}	2.2	2.4	V	V _{DD} = 5.0V
11	O U T P U T S	Low level output voltage	V _{OL}		V _{SS} +0.03	V	No load
12		High level output voltage	V _{OH}	V _{DD} -0.03		V	No load
13		Output low (sink) current	I _{OL}	1.0	2.5	mA	V _{OUT} =0.4 V
14		Output high (source) current	I _{OH}	0.4	0.8	mA	V _{OUT} =4.6 V
15		V _{Ref} output voltage	V _{Ref}	2.3	2.5	V	No load, V _{DD} = 5.0V
16		V _{Ref} output resistance	R _{OR}		1	kΩ	

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Operating Characteristics - $V_{DD}=5.0V \pm 5\%$, $V_{SS}=0V$, $-40^{\circ}C \leq T_O \leq +85^{\circ}C$, unless otherwise stated.
Gain Setting Amplifier

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	$0.75 V \leq V_{IN} \leq 4.25 V$ biased at $V_{Ref} = 2.5 V$
6	DC open loop voltage gain	A_{VOL}	32			dB	
7	Unity gain bandwidth	f_C	0.30			MHz	
8	Output voltage swing	V_O	4.0			V _{pp}	Load $\geq 100 k\Omega$ to V_{SS} @ GS
9	Maximum capacitive load (GS)	C_L			100	pF	
10	Resistive load (GS)	R_L			50	kΩ	
11	Common mode range	V_{CM}	2.5			V _{pp}	No Load

MT8870D AC Electrical Characteristics - $V_{DD}=5.0V \pm 5\%$, $V_{SS}=0V$, $-40^{\circ}C \leq T_O \leq +85^{\circ}C$, using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6,9
			27.5		869	mV _{RMS}	1,2,3,5,6,9
2	Negative twist accept				8	dB	2,3,6,9,12
3	Positive twist accept				8	dB	2,3,6,9,12
4	Frequency deviation accept		$\pm 1.5\% \pm 2$ Hz				2,3,5,9
5	Frequency deviation reject		$\pm 3.5\%$				2,3,5,9
6	Third tone tolerance			-16		dB	2,3,4,5,9,10
7	Noise tolerance			-12		dB	2,3,4,5,7,9,10
8	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES**

1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by $\pm 1.5 \% \pm 2$ Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) $\pm 2\%$.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

MT8870D-1 AC Electrical Characteristics - $V_{DD}=5.0V \pm 5\%$, $V_{SS}=0V$, $-40^{\circ}C \leq T_O \leq +85^{\circ}C$, using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-31		+1	dBm	Tested at $V_{DD}=5.0V$ 1,2,3,5,6,9
			21.8		869	mV _{RMS}	
2	Input Signal Level Reject		-37			dBm	Tested at $V_{DD}=5.0V$ 1,2,3,5,6,9
			10.9			mV _{RMS}	
3	Negative twist accept				8	dB	2,3,6,9,13
4	Positive twist accept				8	dB	2,3,6,9,13
5	Frequency deviation accept		$\pm 1.5\% \pm 2$ Hz				2,3,5,9
6	Frequency deviation reject		$\pm 3.5\%$				2,3,5,9
7	Third zone tolerance			-18.5		dB	2,3,4,5,9,12
8	Noise tolerance			-12		dB	2,3,4,5,7,9,10
9	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES

1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by $\pm 1.5 \% \pm 2$ Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) $\pm 2 \%$.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
13. Guaranteed by design and characterization.

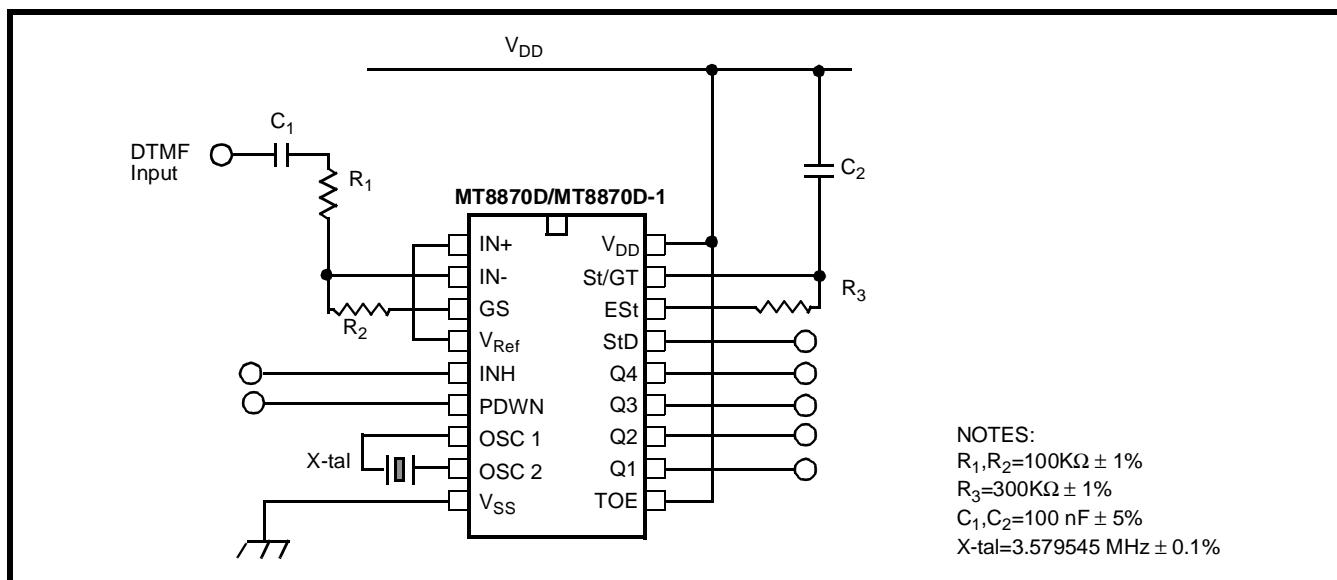
AC Electrical Characteristics - $V_{DD}=5.0V \pm 5\%$, $V_{SS}=0V$, $-40^\circ C \leq T_0 \leq +85^\circ C$, using Test Circuit shown in Figure 10.

		Characteristics	Sym	Min	Typ [‡]	Max	Units	Conditions
1	T I M I N G	Tone present detect time	t_{DP}	5	11	14	ms	Note 1
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 1
3		Tone duration accept	t_{REC}			40	ms	Note 2
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	Note 2
5		Interdigit pause accept	t_{ID}			40	ms	Note 2
6		Interdigit pause reject	t_{DO}	20			ms	Note 2
7	O U T P U T S	Propagation delay (St to Q)	t_{PQ}		8	11	μs	$TOE=V_{DD}$
8		Propagation delay (St to StD)	t_{PSID}		12	16	μs	$TOE=V_{DD}$
9		Output data set up (Q to StD)	t_{QSID}		3.4		μs	$TOE=V_{DD}$
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 k Ω , 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	load of 10 k Ω , 50 pF
12	P D	Power-up time	t_{PU}		30		ms	Note 3
13	W N	Power-down time	t_{PD}		20		ms	
14	C L O C K	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
15		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
16		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
17		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
18		Capacitive load (OSC2)	C_{LO}			30	pF	

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES:**

- Used for guard-time calculation purposes only.
- These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
- With valid tone present at input, t_{PU} equals time from PDWN going low until ESt going high.


Figure 10 - Single-Ended Input Configuration

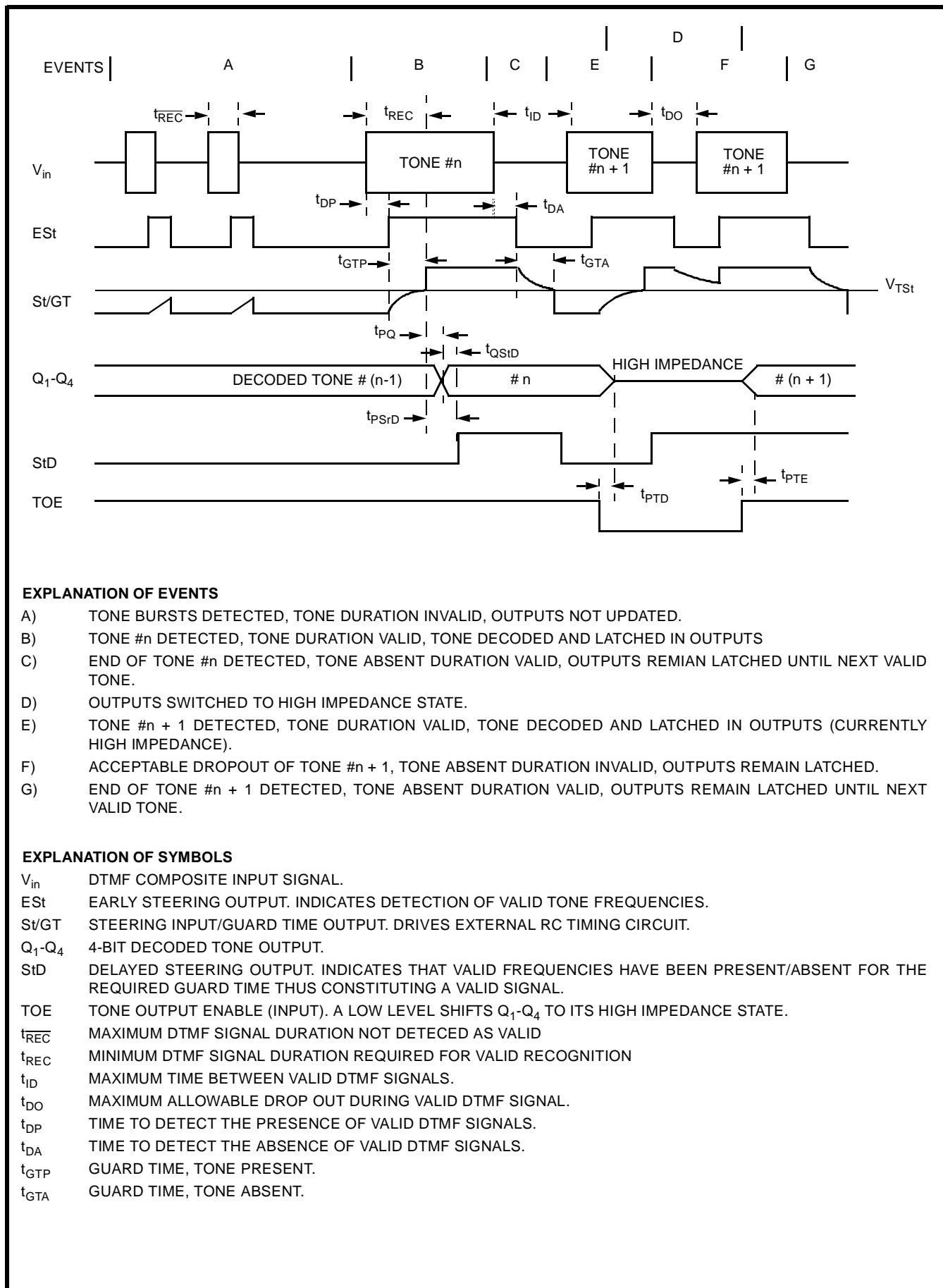


Figure 11 - Timing Diagram

NOTES:

1. Overview

1.1 General Introduction

JQ6500 MP3 is a hardware decoder providing serial MP3 chip, perfectly integrating MP3 and WMV. Meanwhile, the software supports TF card driver, spi flash update on the computer, and FAT16, FAT32 file system. Through simple serial commands, it can execute music playing. Easy-to-use without cumbersome underlying operations, stability and reliability are the most important features of this product. Also the chip is uniquely customized as a low-cost solution for specific voice playing field.

1.2 Features

1. Supports sampling rate (KHz): 8/11.025/12/16/22.05/24/32/44.1/48
2. 24-bit DAC output; dynamic range support 90dB; 85dB SNR support
3. Supports FAT16, FAT32 file system, TF card(maximum capacity 32G), USB 32G, NORFLASH(64M bytes)
4. A variety of control modes: serial mode, AD button control mode
5. Supports inter-cut announcement by pausing the ongoing background music
6. Sort the audio data by folder; supports up to 100 folders with every folder assigned to 1000 songs
7. 30 level volume adjustable, 10 EQ adjustable
8. External spi flash if connected to the computer, can display spi flash drive to update the content
9. Play the specific music through the Microcontroller serial
10. In the button mode, you can choose play modes: pulse repetition, pulse cannot be repeated, the level of non keep recycling, maintain levels of circulating

1.3 Application

1. Voice broadcasts in vehicle navigation;
2. Road transport inspectors, toll station voice prompts;
3. Railway station, bus station security check voice prompts;
4. Power, communications, financial business hall voice prompts;
5. Vehicles access voice prompts;
6. Frontier inspection voice prompts;
7. Multi-channel voice alarms or equipment operation guide voices;
8. Electric sightseeing cars voice notices for safe driving;
9. Electromechanical equipment error auto alarms;

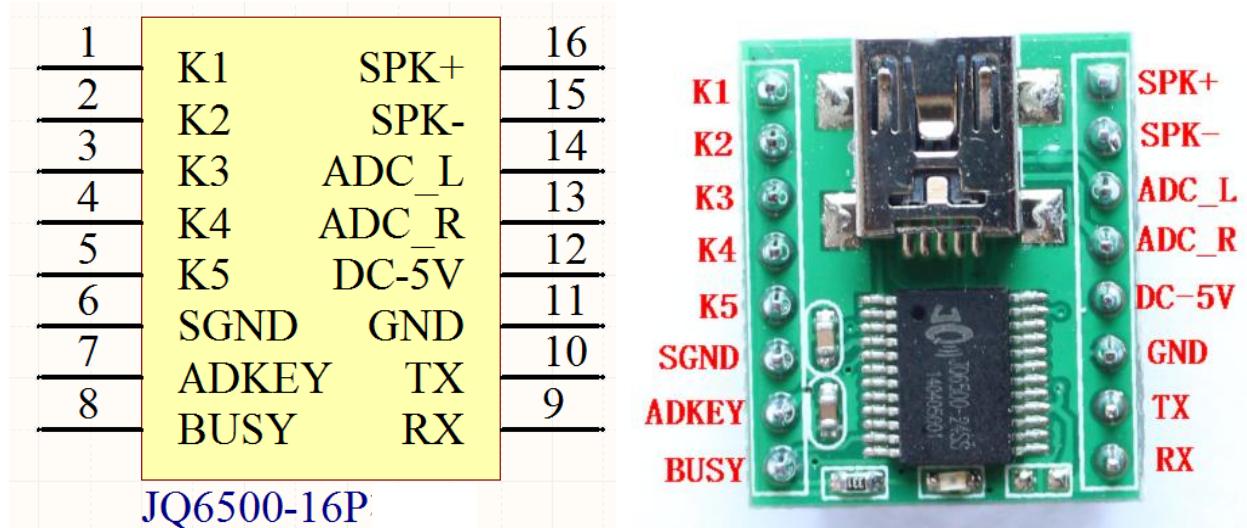
10. Fire alarms;
11. Regular broadcasts of automatic broadcast equipment.

2. Parameters

2.1 Hardware Parameters

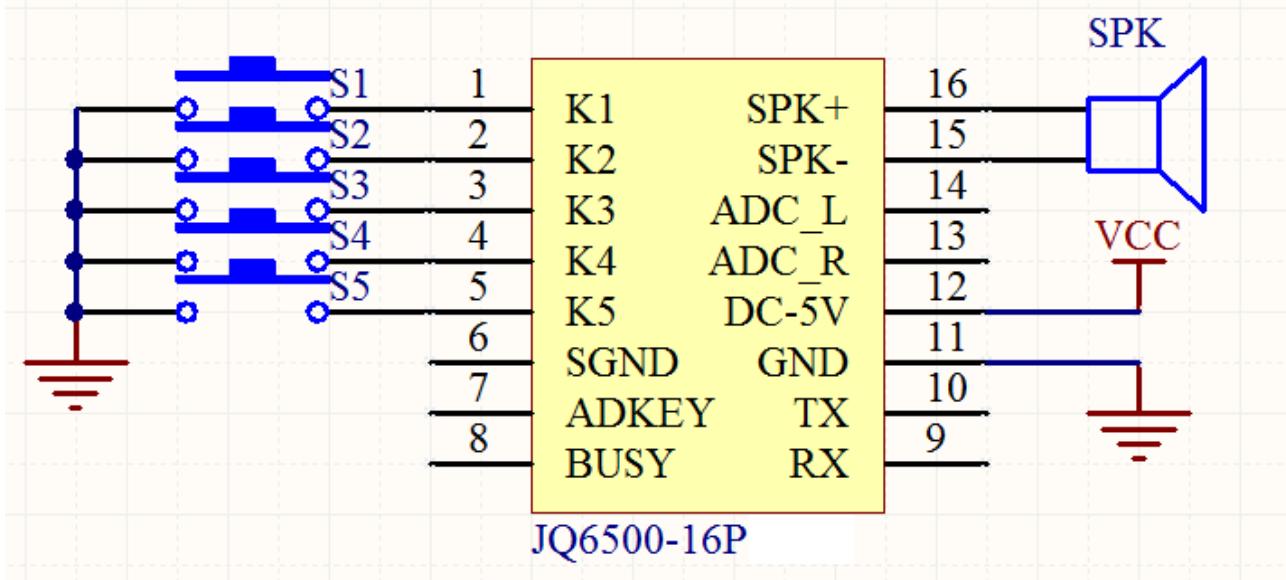
Item	Parameters
MP3 File Format	Support all bit rates 11172-3 and ISO13813-3 layer3 audio decoding
	The sampling rate support (KHZ): 8/11.025/12/16/22.05/24/32/44.1/48
	Support sound effect like Normal, Jazz, Classic, Pop, Rock,etc.
UART Interface	Standard serial port, TTL level, the baud rate can be set up
Input Voltage	power supply 3.5V-5V; optimum value 4.2V
Rated Current	20ma
Size	Standard DIP16 package
Speaker Power	8 ohm / 3 w
Operating Temperature	-40°C~80°C
Humidity	5% ~ 95%

2.2 Module Pin Description



Pin No.	Pin Name	Corresponding Function	Remark
1	K1	corresponding audio Paragraph 1	grounding trigger the playback of audio Paragraph 1
2	K2	corresponding audio Paragraph 2	grounding trigger the playback of audio Paragraph 2
3	K3	corresponding audio Paragraph 3	grounding trigger the playback of audio Paragraph 3
4	K4	corresponding audio Paragraph 4	grounding trigger the playback of audio Paragraph 4
5	K5	corresponding audio Paragraph 5	grounding trigger the playback of audio Paragraph 5
6	SGND	ground	power ground
7	ADKEY	AD port	
8	BUSY	play indicator	high when there's audio output; low when no audio output
9	RX	UART serial data input	
10	TX	UART serial data output	
11	GND	ground	power ground
12	DC-5V	module power input	cannot exceed 5.2V
13	ADC_R	right channel	headphones, amplifier
14	ADC_I	left channel	headphones, amplifier
15	SPK-	speaker +	direct drive speakers below 1W/8R
16	SPK+	speaker -	

2.3 Wiring Diagram



3. Operation

3.1 Communications Directive

1. Send commands directly no need return parameters

Detailed CMD (command)	Corresponding Function	Parameters (16 bits) and the Corresponding Instruction Format
0x01	next	【7E 02 01 EF】
0x02	pre	【7E 02 02 EF】
0x03	assigned song	0-65535、SPI(0-200) 【7E 04 03 00 01 EF】 Indicates the playback of the first paragraph of music. The red font is the number of paragraphs that they can change.
0x04	volume+	【7E 02 04 EF】
0x05	volume -	【7E 02 05 EF】
0x06	assigned volume	0-30 【7E 03 06 15 EF】 The red font is the volume range from 00 to 1E.
0x07	assigned EQ(0/1/2/3/4/5)	Normal/Pop/Rock/Jazz/Classic/Base 【7E 03 07 01 EF】 The red font can be changed from 00 to 05.
0x09	assigned devices(0/1/2/3/4)	U/TF/AUX/SLEEP/FLASH 【7E 03 09 01 EF】 The red font can be changed from 00 to 05.
0x0A	enter sleep mode - low power consumption	Pause 【7E 02 0A EF】

0x0C	chip reset	【7E 02 0C EF】
0x0D	play	【7E 02 0D EF】
0x0E	pause	【7E 02 0E EF】
0x0F	folders switching	1 the next folder; 0 the previous folder 【7E 03 0F 00 EF】 The red font can be described as 00 01.
0x10	preserve	
0x11	loop	0 1 2 3 4(ALL FOL ONE RAM ONE_STOP) 【7E 03 11 00 EF】 The red font is 0001 corresponding mode: 00 for All Cycle, 01 for Single Cycle. Eg: To repeat the second song, first send 7E 03 11 01 EF and then sent 7E 04 03 00 02 EF.
0x12	specified folder file playback	01 01 The former 01 refers to the folder while the latter refers to the file. Note 1: 【7E 04 12 01 01 EF】 play the file 01 in the folder 01

For example, for next, send: 7E 02 01 EF

For previous, send: 7E 02 02 EF

For play, send: 7E 02 0D EF

2. Parameter Query

Detailed CMD (command)	Corresponding Function	Description and Command Format
0x40	Return error, request resend	
0x42	Check the current status	Three states: Play Stop Pause 【7E 02 42 EF】
0x43	Inquire the current volume	【7E 02 43 EF】
0x44	Inquire the current EQ	The return value corresponds to 012345 (Normal/Pop/Rock/Jazz/Classic/Base) 【7E 02 44 EF】
0x45	Inquire the current play mode	The return value corresponds to 0 1 2 3 4(ALL FOL ONE RAM ONE_STOP) 【7E 02 45 EF】

0x46	Inquire the current software version	【7E 02 46 EF】
0x47	Check the total number of files of TF card	【7E 02 47 EF】
0x48	Inquire the total number of UDISK files	【7E 02 48 EF】
0x49	Inquire the total number of FLASH files	【7E 02 49 EF】
0x4B	Inquire the current track of TF card	【7E 02 4B EF】
0x4C	Inquire the current track of UDISK	【7E 02 4C EF】
0x4D	Inquire the current track of FLASH	【7E 02 4D EF】
0x50	Inquire the current play time	【7E 02 50 EF】
0x51	Inquire the total play time of the current track	【7E 02 51 EF】
0x52	Inquire the name of the playing song	The return value is the name of the song(SPIflsh not supported) 【7E 02 52 EF】
0x53	Inquire the total number of the current folders	【7E 02 53 EF】

Example: To read the volume, sent [7E 02 43 EF], it'll directly return to volume (16 bits)

ADKEY resistance function: OR PLAY 3.3K for Next, V + 6.2K for Pre, V-9.1K for mode switching.

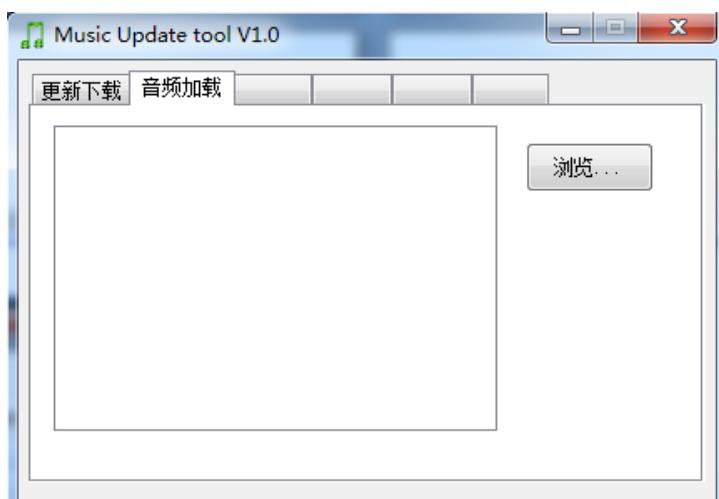
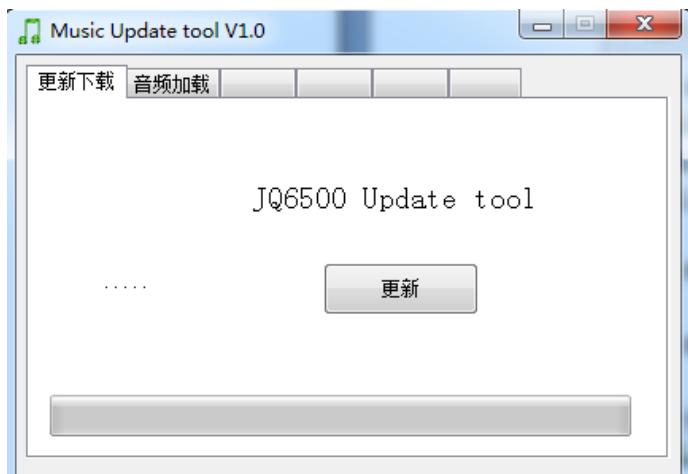
Note 1: The folders inside USB and TF card must be named 01 02...99; the files inside the folders must be named 001 002 003....

4. Instructions on Voice Update

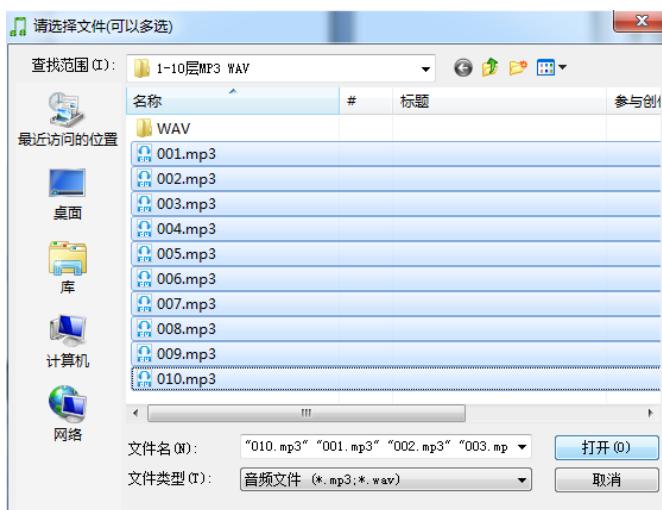
Connect the MINI USB of the module to the computer. Open “My Computer”, double-click the “CD

▲ 有可移动存储的设备 (1)

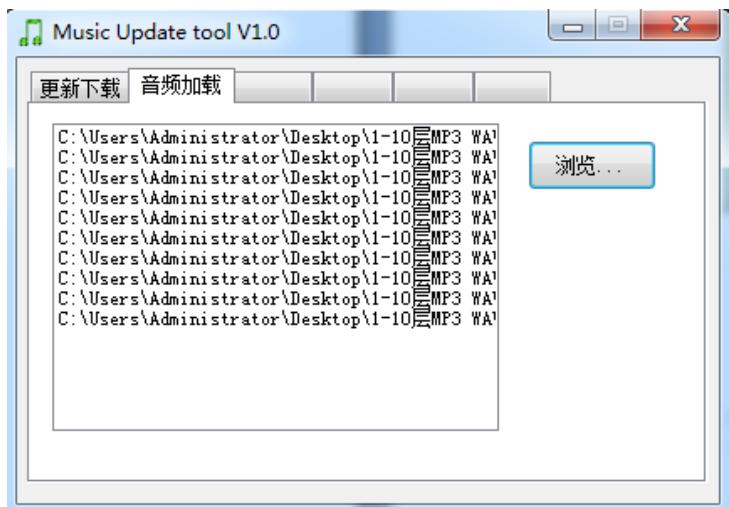
Drive”  CD 驱动器 (H:) JQ... CD 驱动器 , and you will see an update content of PC software, as shown below:



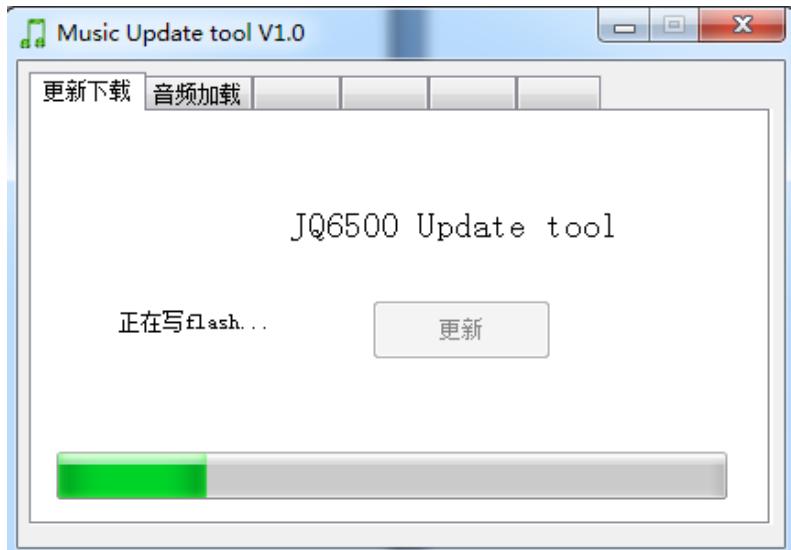
Select "Audio loading" - Click "Browse".



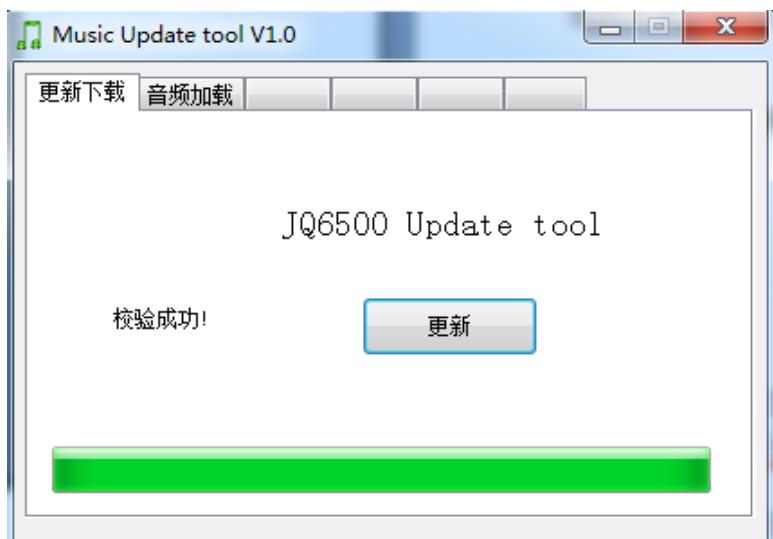
Choose the audio, click the "Open".



The audio is added to the PC software.

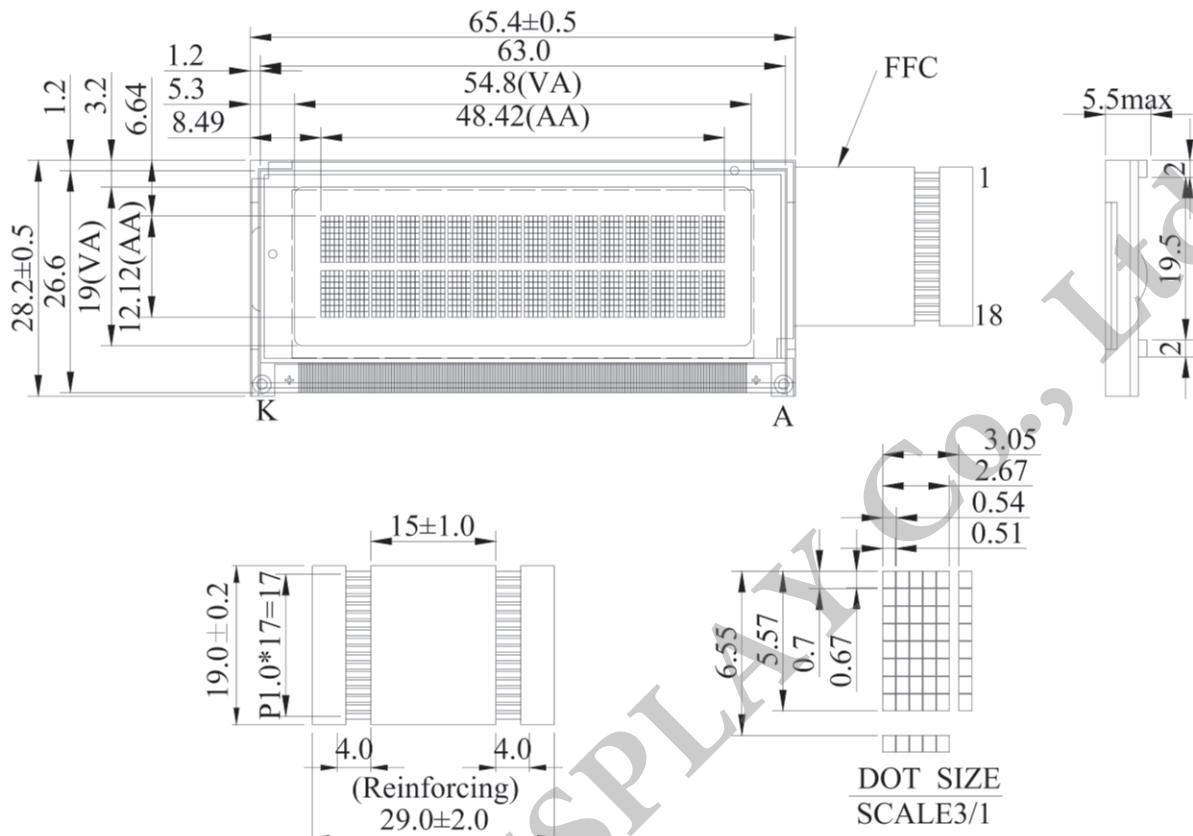


Select "update download" tab, click update;
Audio writing is shown in picture.



The picture means that the voice has been downloaded to the spi flash in the module.

WH1602T Character 16x2



Feature

- 1.5x8 dots includes cursor
- 2.Bult-in controller (ST7066 or Equivalent)
- 3.5V power supply only
- 4.N.V, optional for 3V power supply
- 5.1/16 duty cycle
- 6.White LED B/L not available
- 7.Interface : 6800, option SPI/I2C (RW1063 IC)

Pin No.	Symbol	Description
1	V _{DD}	Power supply for logic
2	V _{SS}	Ground
3	V _O	Contrast Adjustment
4	NC	No connection
5	NC	No connection
6	RS	Data/ Instruction select signal
7	R/W	Read/Write select signal
8	E	Enable signal
9	DB0	Data bus line
10	DB1	Data bus line
11	DB2	Data bus line
12	DB3	Data bus line
13	DB4	Data bus line
14	DB5	Data bus line
15	DB6	Data bus line
16	DB7	Data bus line
17	A	Power supply for B/L +
18	K	Power supply for B/L -

Mechanical Data

Item	Standard Value	Unit
Module Dimension	65.4 x 28.2	mm
Viewing Area	54.8 x 19.0	mm
Character Size	2.67 x 5.57	mm

Electrical Characteristics

Item	Symbol	Standard Value typ.	Unit
Input Voltage	VDD	5.0	V
Recommended LCD Driving Voltage for Normal Temp. Version module @25°C	VDD-VO	4.20	V

Display Character Address Code

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01	02												0E	0F
DD RAM Address	40	41	42												4E	4F

APPENDIX G: Rubrics for Project Phase-I and Phase-II

Review-I

Sr.No.	Criterion	Excellent	Good	Beginner
1	Problem Definition (5)	Problem Statement clearly defined. (5-4)	Problem Statement partially defined. (4-2)	Problem Statement not defined. (2-0)
2	Scope & Objectives (10)	Description of scope of project is clearly stated and objective of project is clear (10-8)	Description of scope of project is somewhat clearly stated and objective is somewhat clear (8-5)	Scope and Objective of project is not clear (5-0)
3	Literature Review (10)	Many and relevant IEEE paper refereed. Comprehensive review providing a good basis for the project. Entire Coverage with relevant and accurate support. (10-8)	Few and relevant Papers Referred but not IEEE. Systematic survey attempted but incomplete and inconsistent. Little coverage and less accurate support. (8-5)	Very few and no relevant papers referred. No evidence of research been conducted. (5-0)
4	Methodology (10)	Methodologies which will be used are clearly described. (10-8)	Methodology which will be used are partially described (8-5)	Methodology are not described (5-0)
5	Block Diagram / Architecture (10)	Block Diagram and Design is Correct. (10-8)	Block Diagram and Design is partially Correct (8-5)	Block Diagram and Design is incorrect (5-0)
6	Project Planning (5)	Highly effective use of available resources. Effective management of workload (5-4)	Moderate use of available resources. Less effective management of workload (4-2)	No use of available resources No management of workload. (2-0)

	Total (50)	(50-40)	(40-27)	(25-0)
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Review-II

Sr.No.	Criterion	Excellent	Good	Beginner
1	Requirement Specification (10)	Properly stated and correct Specification (10-8)	Not clearly stated and incorrect Specification (8-5)	Not Properly stated and incorrect Specification (5-0)
2	Literature Review (5)	Additional improvement in the Literature Review (5-4)	Less improvement in the Literature Review (4-2)	No improvement in the Literature Review (2-0)
3	Detailed Design (10)	Designing is stated correctly (10-8)	Design is partially correct (8-5)	Designing is not correct (5-0)
4	Experimental Setup / Simulation (10)	Proper simulation and correct Experimental Setup (10-8)	Simulation and Experimental Setup is partially correct (8-5)	Simulation and Experimental Setup is not done. (5-0)
5	Performance Parameters (10)	Performance Parameters are stated clearly. (10-8)	Performance Parameters partially stated. (8-5)	Performance Parameters not stated. (5-0)
6	Efficiency Issues (5)	Efficiency Issues addressed. (5-4)	Efficiency Issues partially addressed. (4-2)	Efficiency Issues not addressed. (2-0)
	Total (50)	(50-40)	(40-27)	(25-0)

Stage-I Documentation

Sr.No.	Criterion for (Project Stage-I)	Excellent	Good	Beginner
1	Documentation (50)	All Contents are covered with the given format and well organized report. (50-40)	Content are covered but the format is not proper and somewhat organized report. (40-20)	Content are not covered, format is not proper and report not organized. (<20)

Sr.No.	Criterion
1	Project Review 1 (50)
2	Project Review 2 (50)
3	Documentation (Project Stage-I Report) (50)
	Average of Review-1, Review-2 and Documentation stage is taken for 50 marks Evaluation

Review –III

Sr.No.	Criterion	Excellent	Good	Beginner
1	Revised Final Design (10)	Final Design is correct (10-8)	Final Design is somewhat correct (8-5)	Design is incorrect, to be revised again (5-0)
2	Tools and Techniques Used (10)	Appropriate tools and techniques used(10-8)	Tools and techniques to some extent only used (8-5)	Tools and techniques not used(5-0)
3	Partial Implementation (15)	Project is partially implemented (15-12)	Project implementation is just started. (12-7)	Project implementation is not yet started. (7-0)
4	Partial Results (15)	Partial Results are correct. (15-12)	Partial results are somewhat correct. (12-8)	Results not obtained. (8-0)
	Total (50)	(50-40)	(40-25)	(25-0)

Review –IV

Sr.No.	Criterion	Excellent	Good	Beginner
1	Implementation Status (10)	Project implementation is complete. (10-8)	Project implementation is partially completed. (8-5)	Project implementation is incomplete. (5-0)
2	Modular Testing (10)	Modular testing is correct (10-8)	Modular testing is somewhat correct(8-5)	Modular testing is incorrect. (5-0)
3	Intermediate Results (15)	Desired results are shown (15-12)	Results are partially shown. (12-8)	Results are not obtained. (8-0)
4	Conclusion and Future Scope (10)	Conclusion and future scope are clearly stated (10-8)	Conclusion and future scope are somewhat clearly stated (8-5)	Conclusion and future scope are not clear. (5-0)

5	Cost Analysis (5)	Cost analysis is correct. (5-4)	Cost analysis is somewhat done (4-2)	Cost analysis not done.(2-0)
	Total (50)	(50-40)	(40-25)	(25-0)

Stage-II Documentation

Sr.No.	Criterion for (Project Stage-II)	Excellent	Good	Poor
1	Documentation (50)	All Contents are covered with the given format and well organized report. (50- 40)	Content are covered but the format is not proper and somewhat organized report. (40-20)	Content are not covered, format is not proper and report not organized. (<20)

Sr.No.	Criterion
1	Project Review 3 (50)
2	Project Review 4 (50)
3	Documentation (Project Stage-II Report) (50)
	Total of Review-3, Review-4 and Documentation stage is taken for 150 marks Evaluation