

KARMAVEER KAKASAHEB WAGH INSTITUTE OF ENGINEERING EDUCATION AND RESEARCH



EMPLOYABILITY SKILLS & MINI PROJECT REPORT ON

“Third Eye for Blind”

Submitted by

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**DEPARTMENT OF
ELECTRONICS AND TELECOMMUNICATION
ENGINEERING**

YEAR 2020-2021

KARMAVEER KAKASAHEB WAGH INSTITUTE OF ENGINEERING EDUCATION AND RESEARCH



CERTIFICATE

This is to certify that the project work titled "**Third Eye for Blind**", has been successfully completed during the academic year of 2020-2021 by the following students:

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This project conforms to the standards laid down by SPPU and has been completed in satisfactory manner as a partial fulfillment for the bachelor's degree in Electronics & Telecommunication Engineering, SPPU.

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ACKNOWLEDGMENT

With all respect and gratitude, we would like to thank all the people who have helped us directly or indirectly for the project work.

We would like to thank **Prof. Dr. K. N. Nandurkar** Principal, K. K. Wagh Institute of Engineering Education and research, Nashik and **Prof. Dr. D. M. Chandwadkar** HOD, of Electronics and Telecommunication. We express our humble gratitude for being with us and for all the help needed.

We would extend deep gratitude towards **Prof. Dr. S. A. Patil (Ugale)** for guidance and selection of our project. Madam has given us very important guide lines that helped us for strengthening the objective of our project.

Finally, we would like to express our sincere gratitude towards **Prof. S. V. Shelke** for helping us to complete this project work on “**Third Eye for Blind**” Their ideas and direction gave us moral boost up to complete this project.

We are ending this acknowledgement with deep indebtedness to our friends and each and every person who help us to complete the manuscript.

Thank you!!!

ABSTRACT

People with visual disabilities are often dependent on external assistance which can be provided by humans, trained dogs, or special electronic devices as support systems for decision making. The main problem with blind people is how to navigate their way to wherever they want to go. Such people need assistance from others with good eyesight. As described by WHO, 10% of the visually impaired have no functional eyesight at all to help them move around without assistance and safely.

This project is designed to help the blind to overcome the lack of visual sense, by using other senses like sound and touch. The system uses *80C51 microcontroller, which is 8-bit RISC-based microcontroller*. For sensing the distance, the system uses *an Infrared sensor*. The sensor module is designed to sense characteristics in its surroundings by emitting and/or detecting infrared radiation. Infrared sensors are also used to measure distance or proximity. The reflected light is detected and then an estimate of presence of an object is made. The system also consists of a buzzer to generate an alarm sound and a motor to generate vibration signals. The system uses audio and vibration signals to notify the user about upcoming hurdle. As the distance between glove and obstacle decreases, frequency of both audio and vibration signals increases. Thus, the system helps to ease the navigation process for the needy. This system offers a low-cost, reliable, portable, low power consumption and robust solution for navigation with obvious short response time.

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1. Introduction

Third eye for blind is a wearable device that can help the visually impaired people to move by themselves in an indoor environment. This reduces the work on people who are assisting the blind. Furthermore, it also provides an opportunity for visually impaired persons to move from one place to another independently. Technology has been developing a lot these days and people are showing interest in them. This device is helpful especially when the person wants to move around a house or some indoor places by themselves.

In this device, the obstacle is detected by using *an Infrared sensors module and a Microcontroller*. The sensor module is designed to sense characteristics in its surroundings by emitting and/or detecting infrared radiation. Infrared sensors are also used to measure distance or proximity. The reflected light is detected and then an estimate of presence of an object is made. The system also consists of a buzzer to generate an alarm sound and a motor to generate vibration signals. The system uses audio and vibration signals to notify the user about upcoming hurdle. The obstacle distance is measured and informed to the visually impaired person in the form of a buzzer and vibrations. The person can move in other directions and avoid collisions using this. This project used only the microcontroller instead of using a whole Arduino board, so the size of the device is reduced to a large extent and the cost is also minimized. End results of the work would be a glove with a wearable band attached to the gloves to which all the components are connected on a PCB, which works with high degree of accuracy and reliability. Thus, the system helps to ease the navigation process for the needy. This system offers a low-cost, reliable, portable, low power consumption and robust solution for navigation with obvious short response time.

2. Literature Survey

1] Third eye for the visually impaired utilizing arduino and ultrasonic sensor by k. Maheswari, Dr. D. Subitha (2020).

The goal of this venture The Third Eye for the Visually impaired is to plan an item which is especially helpful to those individuals who are outwardly disabled and the individuals who frequently need to depend on others. This is the wearable innovation for the blinds which helps settle every one of the issues of the current advancements. When the ultrasonic sensor recognizes snag the gadget will inform the client through vibrations and sound blares

2] Third Eye for Blind Using Ultrasonic Sensor GVNSK Sravya, N Harini Department of Electronics and Communication Engineering, G. Narayananamma Institute of Technology and Science for Women, Hyderabad, India (2020).

Third eye for blind is a wearable device that can help the visually impaired people to move by themselves in an indoor environment. In this device, the distance of the obstacle is determined by using an Ultrasonic module and a Microcontroller. The obstacle distance is measured and informed to the visually impaired person in the form of a buzzer and vibrations. The person can move in other directions and avoid collisions using this. This project used only the microcontroller instead of using a whole Arduino board, so the size of the device is reduced to a large extent and the cost is also minimized. End results of the work would be a glove with a wearable band attached to the gloves to which all the components are connected on a PCB, which works with high degree of accuracy and reliability.

3] Navigation System for Blind -Third Eye Samartha Koharwal, Samer Bani Awwad, Aparna Vyakaranam (2019).

This project proposes the design of portable AI based —guidance system for blind –Third Eye, which benefits the visually impaired community and also helps in their day to day mobility. Third eye provides the visually impaired community a new way to visualize the world by explaining them about their surroundings. The whole system is controlled by Raspberry Pi microcontroller. Third eye harnesses the maximum capabilities of Raspberry Pi microcontroller which has enough potential to uphold the system with one advantage being the inbuilt graphic card. The prototype uses various sensors such as IR Sensors, Sonar Sensors and a Camera module which helps the system to gather the required data. Additionally, text to speech module is used to talk to the user.

4] Third Eye for the Blind Person Nikhil Manwani¹Sajal Gupta²Piyush Agrawal³Mandeep Singh Saini.

This proposed system consists the equipment like Arduino mini pro, ultrasonic sensor, pref board, vibrating motor, buzzers for detecting the obstacles and letting the user know about the obstacle, Red LEDs, Switches, Jumper cable, power bank, Male and female header pins, 3.3 volt old mobile battery which is unused or discarded, some elastic and stickers to make the device wearable as a band for wearing for the users. The transmitter emits the US waves and if obstacles are present in the path, the US waves hits the obstacles and gets reflected back, the reflected wave is received by the receiver. The US sensor is a combination of one transmitter and receiver. In this way, along these lines Third Eye for Blind will be intended for the outwardly weakened individuals and will make it simple and advantageous as it will be a wearable gadget and therefore will help the client in voyaging and identifying the impediments while strolling effortlessly

5] Third eye for blind people using ultrasonic vibrating gloves with image processing. Suprabha Potphode¹, Sneha Kumbhar², Prashant Mhargude³, Parvin Kinikar

The existing system consists of the devices used for helping blind peoples to detect the obstacles and travel to places; It is a smart device like a torch for blinds. When an ultrasonic sensor detects the obstacle then vibrating motor vibrates and also there is audio to turn left or right-side blind people move in a safe place. VGA camera captures the image and sends it towards the controller for the identification.

3. System Details

3.1 Project Specifications:

1. 80C51 microcontroller:

80C51 is a high-performance static 80C51 design fabricated with high-density CMOS technology with operation from 2.7 V to 5.5 V. The 80C51 contain a 128×8 RAM and 256×8 RAM respectively, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits. in addition, the device is a low power static design which offers a wide range of operating frequencies down to zero. Two software selectable modes of power reduction-idle mode and power-down mode are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.

Features:

- 8051 Central Processing Unit- $4k \times 8$ ROM (80C51)
- Memory addressing capability-64k ROM and 64k RAM
- Power control modes: Clock can be stopped and resumed-Idle mode-Power-down mode
- CMOS and TTL compatible
- TWO speed ranges at $V_{CC} = 5$ V-0 to 16 MHz-0 to 33 MHz
- Extended temperature ranges
- Dual Data Pointers
- 4 level priority interrupts (6 interrupt sources)
- Four 8-bit I/O ports
- Full-duplex enhanced UART-Framing error detection-Automatic address recognition.

2. Infrared Sensor:

Infrared Sensor, it works on 5Vdc operating voltage and supply current is 20mA, its ranging module that provides up to 20 cm. It provides adjustable sensing range, and has built-in ambient light sensor. IR LED emits light, in the range of Infrared frequency. IR light is invisible to us as its wavelength (700nm – 1mm) is much higher than the visible light range. IR LEDs have light

emitting angle of approx. 20-60 degree and range of approx. few centimeters to several feet, it depends upon the type of IR transmitter and the manufacturer. Some transmitters have the range in kilometers. IR LED white or transparent in colour, so it can give out amount of maximum light.

Features:

- 5VDC Operating voltage
- I/O pins are 5V and 3.3V compliant
- Range: Up to 20cm.
- Adjustable Sensing range
- Built-in Ambient Light Sensor
- 20mA supply current

3. DC Motor:

Motor1 is a 12V DC geared motor with a .25" motor output shaft and a 2mm rear encoder shaft. The 2mm shaft works with our ENC300 quadrature encoder to allow the motor to be used in position control applications. Motor controllers that are rated for 12V@2A are ideal for controlling this motor. However, motor controllers with lower current ratings can also be used if they have over-current and overtemperature protection.

Features:

- 12V – 200RPM –
- 3.6KG CM torque DC gearhead motor
- 30:1 Gear Ratio
- 2mm rear encoder shaft
- Good compromise between speed and torque for small robotic designs.

4. Buzzer:

The Buzzer specification rated voltage is 6V DC, operating voltage is 4-8V DC, rated current is <30mA, the sound type is continuous beep, with the resonant frequency 2300hz.

Features:

- Rated Voltage: 6V DC
- Operating Voltage: 4 to 8V DC
- Rated Current*: $\leq 30\text{mA}$
- Sound Output at 10cm*: $\geq 85\text{dB}$
- Resonant Frequency: $2300 \pm 300\text{Hz}$
- Temperature: -25°C to $+80^\circ\text{C}$

5. LED (Light Emitting Diode):

LEDs can last over 100,000 hours (10+ years) if used at rated specifications there is no annoying flicker like from fluorescent lamps. LEDs are impervious to heat, cold, shock and vibration. LEDs do not contain breakable glass, this LEDs are Solid-State, shock and vibration resistant, there is low power consumption that puts less load on the electrical systems increasing battery life.

Features:

- For DC and pulse operation
- Luminous intensity categorized
- Standard T-1 $\frac{3}{4}$ package
- Package: 5 mm
- Product series: standard
- Angle of half intensity: $\pm 30^\circ$

6. Voltage Regulator 7805:

LM7805 Family monolithic3-terminal positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heatsinking is provided, they can deliver over 1.5-A output current. They are intended as fixed voltage regulators in a wide range of applications including local(on-card) regulation for elimination of noise and distribution problems associate with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents. The voltage regulator is 5V positive regulator with minimum input voltage is 7V and maximum input voltage is 25V.

Features:

- Output Current up to 1.5 A
- Available in Fixed 5-V, 12-V, and 15-V Options
- Output Voltage Tolerances of $\pm 2\%$ at $T_J = 25^\circ\text{C}$ (LM340A)
- Line Regulation of 0.01%/ V of at 1-A Load (LM340A)
- Load Regulation of 0.3%/ A (LM340A)
- Internal Thermal Overload, Short-Circuit and SOA Protection
- Available in Space-Saving SOT-223 Package
- Output Capacitance Not Required for Stability

3.2 Block Diagram:

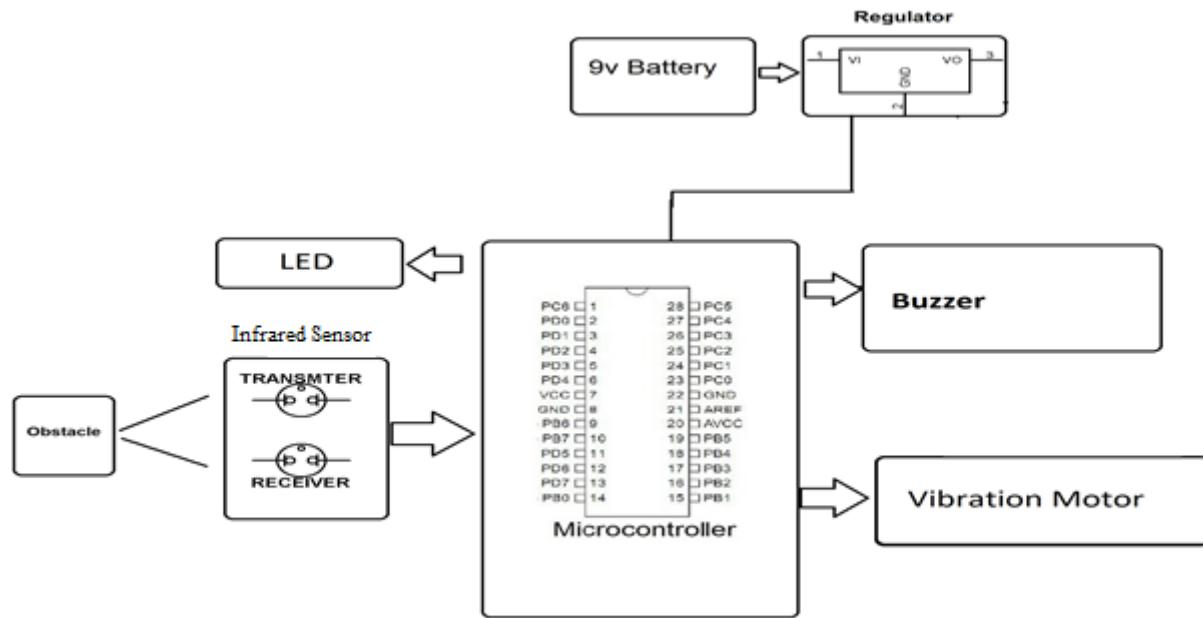


Figure 3.2.1: Block Diagram

3.3 Description of blocks:

1. 80C51 microcontroller:

In this project microcontroller acts, as a main controlling element or as a brain of the system.

In the proposed system the IR sensor, act as input device which senses the obstacle and when the obstacle is detected, it will provide the input to the microcontroller. The Microcontroller then takes the decision depending on the presence of the object, it will run the motor with higher speed and it will also give the indication to user by audio signal i.e. by turning on buzzer and it will also glow the LED. In case of absence of an object, it will simply run the motor with lower speed. The Microcontroller device is a low power static design which offers a wide range of operating frequencies down to zero. There are two software selectable modes of power reduction, idle mode and power down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.



Figure 3.3.1: 80C51 microcontroller

2. Infrared Sensor:

An Infrared (IR) sensor is an electronic device that measures and detects infrared radiation in its surrounding environment. In this project an IR sensor is used to sense the presence of an object/obstacle in front of a blind person. An IR sensor, acts as an input element. If the obstacle is detected it will provide the input to the microcontroller and accordingly the microcontroller will perform necessary actions. IR is invisible to the human eye, as its wavelength is longer than that of visible light anything that emits heat gives off infrared radiation. There are two types of infrared sensors: active and passive. Active infrared sensors both emit and detect infrared radiation. Active IR sensors have two parts: a light emitting diode (LED) and a receiver. When an object comes close to the sensor, the infrared light from the LED reflects off of the object and is detected by the receiver. Active IR sensors act as proximity sensors, and they are commonly used in obstacle detection systems (such as in robots). Passive infrared (PIR) sensors only detect infrared radiation and do not emit it from an LED.

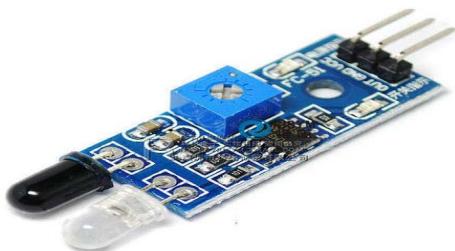


Figure 3.3.2: Infrared sensor

3. DC Motor:

In the proposed system the DC motor is simply used to generate the vibrations. In the absence of the obstacle, it will rotate at lower speed as soon as obstacle is detected microcontroller will

increase its speed of rotation. By sensing increase in vibrations, the user will come to know about upcoming hurdle. The DC motor is the motor which converts the direct current into the mechanical work. It works on the principle of Lorentz Law, which states that “the current carrying conductor placed in a magnetic and electric field experience a force”. And that force is the Lorentz force.



Figure 3.3.3: DC motor

4. Buzzer:

Buzzer acts as an output device which is used to give sound indication to user about upcoming hurdle. IR sensor senses the presence of an object/obstacle in front of a blind person. An IR sensor, acts as an input element. If the obstacle is detected it will provide the input to the microcontroller and accordingly the microcontroller will give indications to user by turning on buzzer. The buzzer consists of an outside case with two pins to attach it to power and ground.

Inside is a piezo element, which consists of a central ceramic disc surrounded by a metal (often bronze) vibration disc. When current is applied to the buzzer it causes the ceramic disk to contract or expand. Changing this then causes the surrounding disc to vibrate. That's the sound that you hear. By changing the frequency of the buzzer, the speed of the vibrations changes, which changes the pitch of the resulting sound.

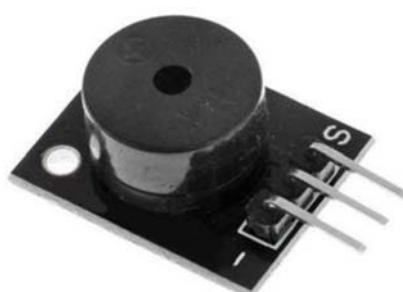


Figure 3.3.4: Buzzer

5. LED (Light Emitting Diode):

A light releasing diode is an electric component that emits light when the electric current flows through it. It is simply use for indication purpose when obstacle is detected then microcontroller

will turn on the LED otherwise it will remain off. It is a light source based on semiconductors. When current passes through the LED, the electrons recombine with holes emitting light in the process. It is a specific type of diode having similar characteristics as the p-n junction diode.



Figure 3.3.5: LED

6. Voltage Regulator 7805:

The LM78XX/LM78XXA series of three-terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a Wide range of applications. Each type employs internal current limiting, thermal shutdown and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output Current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

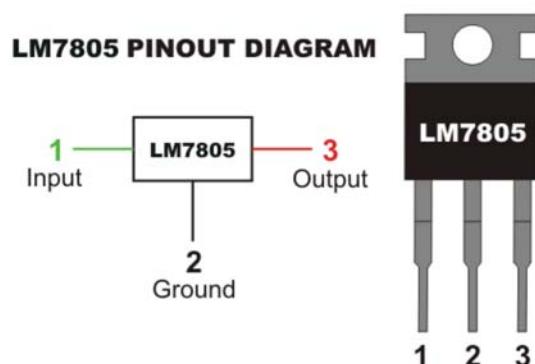


Figure 3.3.6: Voltage regulator 7805

4. Design

4.1 Circuit Diagram:

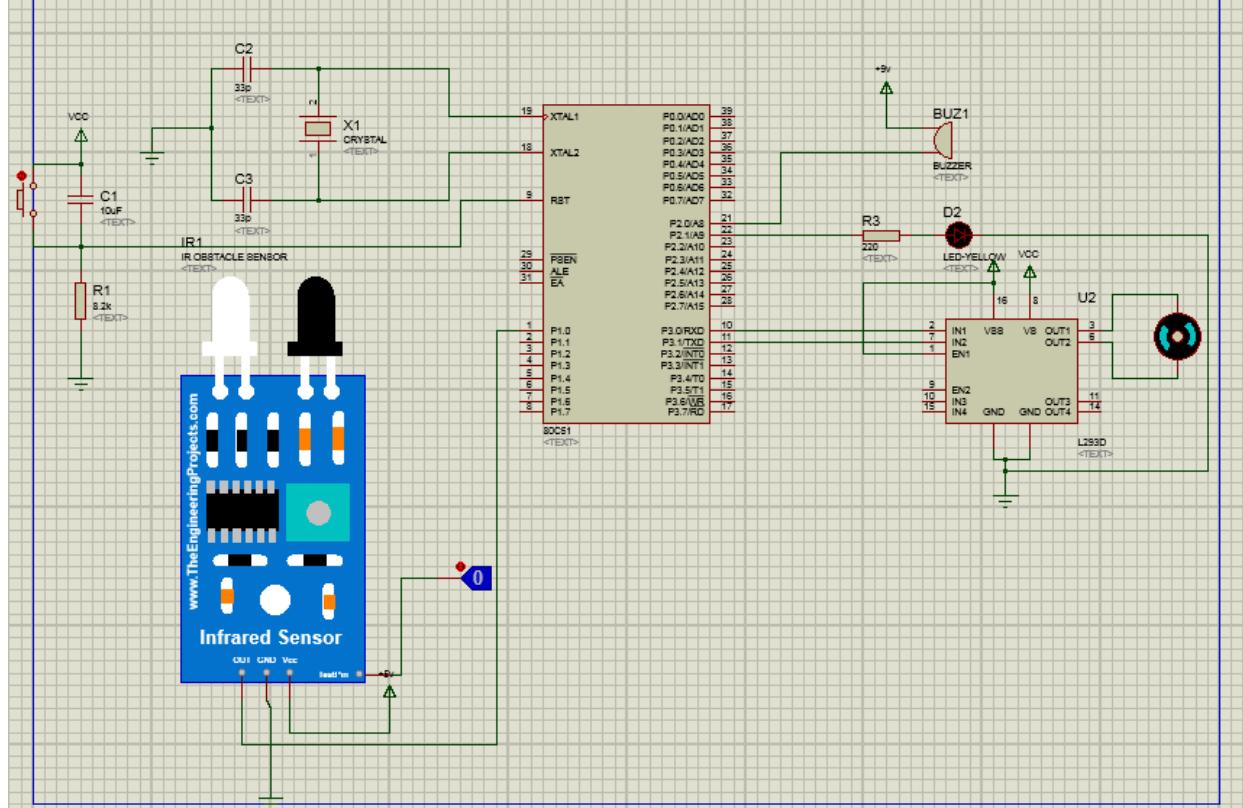


Figure 4.1(a): Circuit Diagram

In the circuit diagram an IR sensor acts as an input device and motor, LED, buzzer acts as an output device. IR sensor will sense the presence of an obstacle in front of a blind person and provide an input to the microcontroller. In this project microcontroller acts, as a main controlling element or as a brain of the system. The Microcontroller then takes the decision depending on the presence of the object, it will run the motor with higher speed and it will also give the indication to user by audio signal i.e. by turning on buzzer and it will also glow the LED. In case of absence of an object, it will simply run the motor with lower speed.

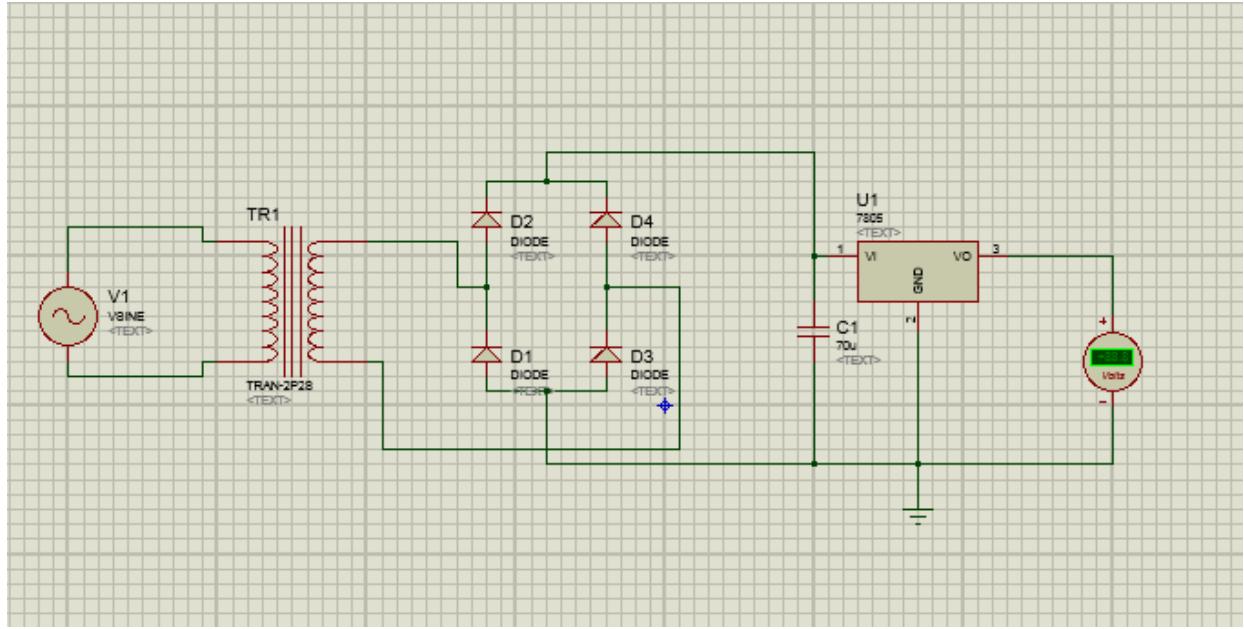


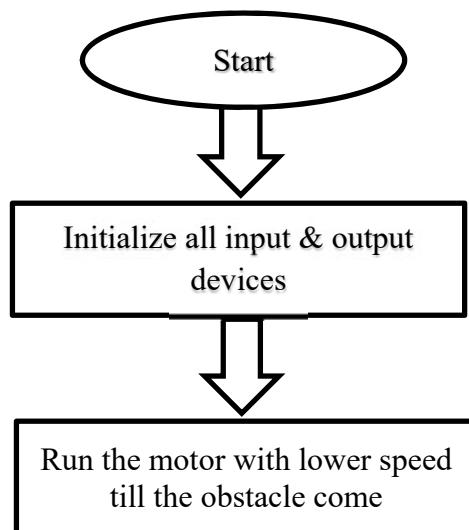
Figure 4.1(b): Circuit Diagram of power supply

4.2 Software:

- **Algorithm:**

1. Start
2. Initialize all input and output devices.
3. Run the motor with lower speed till the obstacle come.
4. Monitor the output of the IR sensor if it is high (i.e. obstacle is detected) increase the speed of the rotation of the motor, also turn on the buzzer and glow the LED for indication purpose.
5. stop

- **Flowchart:**



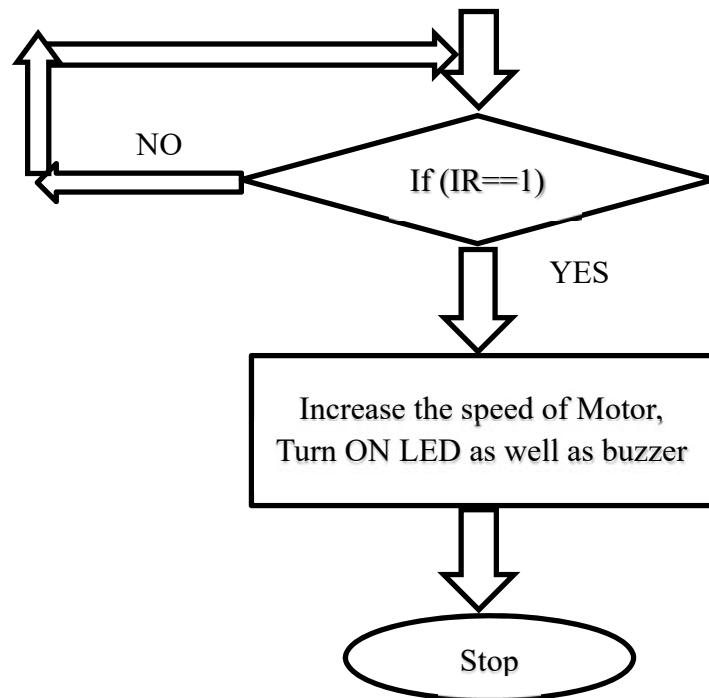


Figure 4.2: Flowchart

4.3 PCB design:

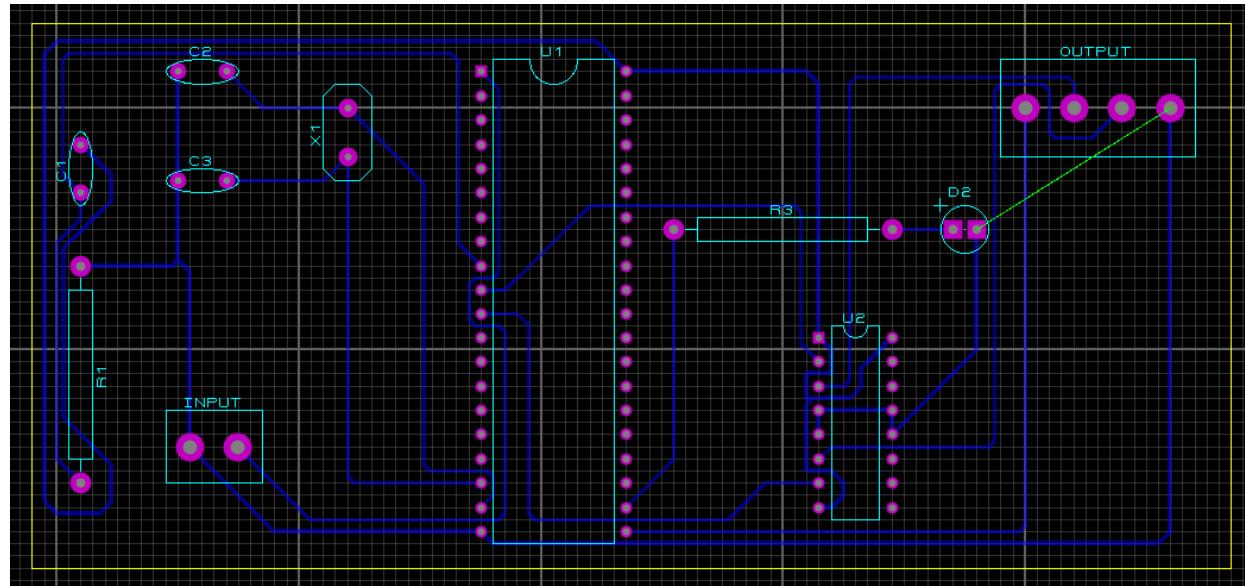


Figure 4.3.1(a): PCB Layout

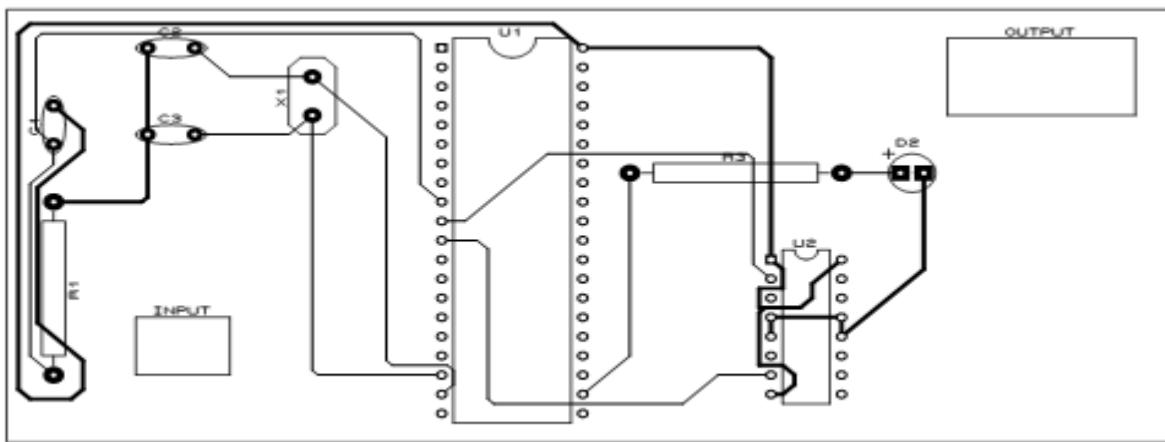


Figure 4.3.1(b): Actual PCB Layout

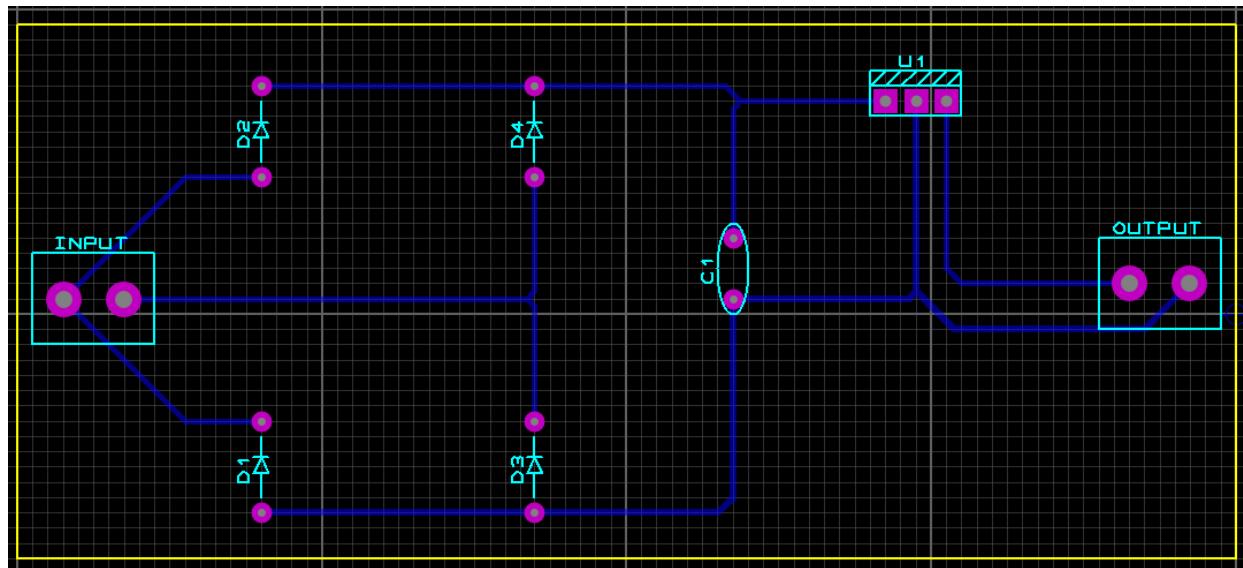


Figure 4.3.1(c): PCB Layout of a power supply

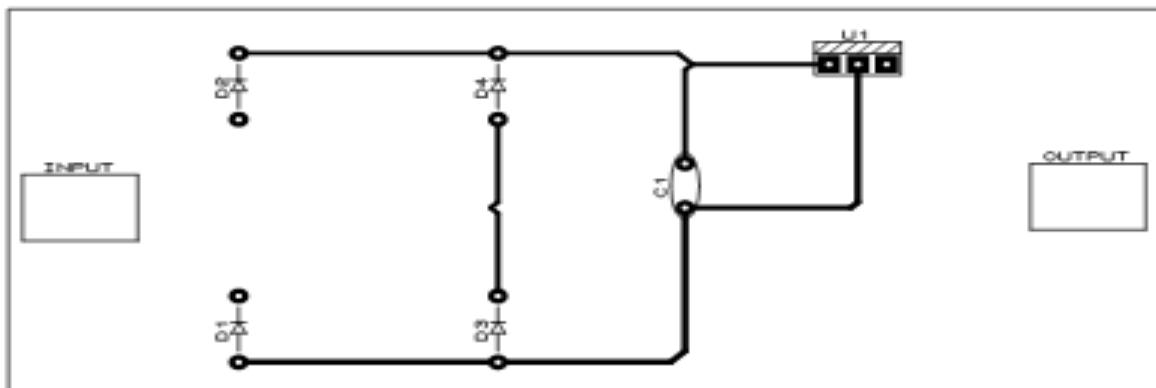


Figure 4.3.1(d): Actual PCB Layout of a power supply

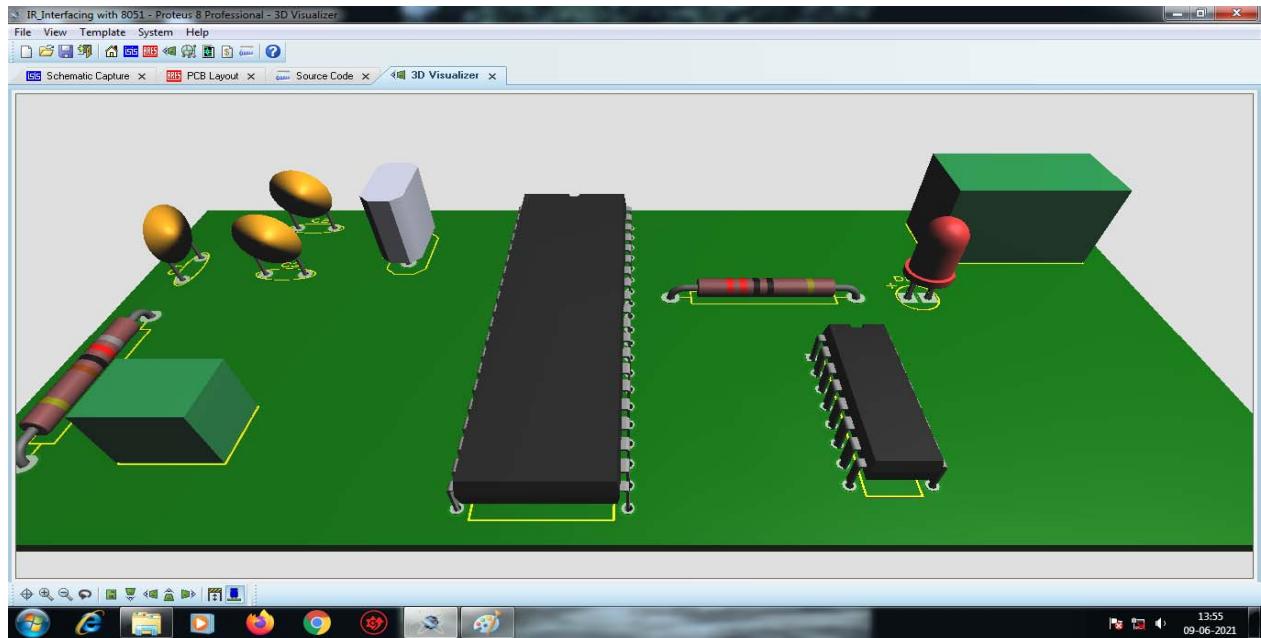


Figure 4.3.1(e): 3D View of PCB

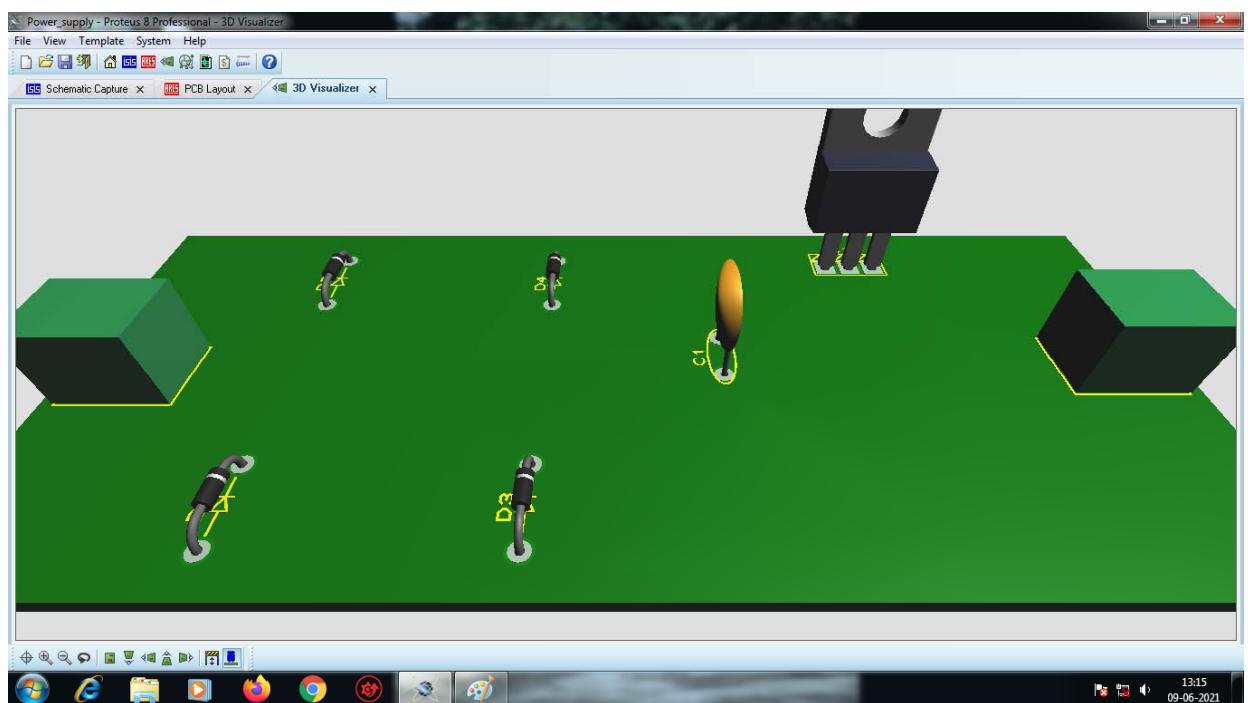


Figure 4.3.1(f): 3D View of PCB of a power supply

5. Testing

We have carried out testing in following steps:

Step-1: Firstly, we have checked only the interfacing of Buzzer and LED with 80C51 microcontroller and monitored whether they are functioning properly or not. In order to test whether LED is glowing or not we have simply interface it with push button and same procedure is followed for buzzer as well.

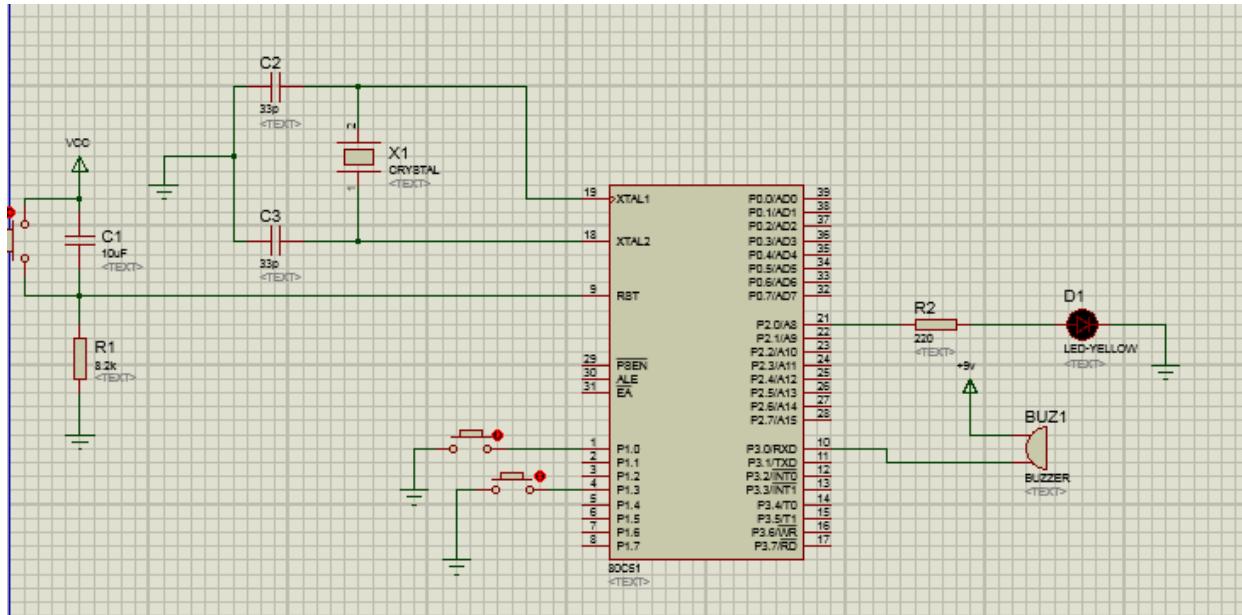


Figure 5.1: Interfacing of LED and Buzzer

Step-2: In this step we have checked the speed of rotation of motor by the interfacing motor with 80C51 microcontroller. In order to change the speed of motor we have used three push buttons for lower, medium and higher speeds. We cannot interface motor directly with microcontroller as output current sinking capability of microcontroller is less, hence a driver IC called L293D is used in between microcontroller and the motor. By pressing each and every switch we have verified the speed of rotation of the motor.

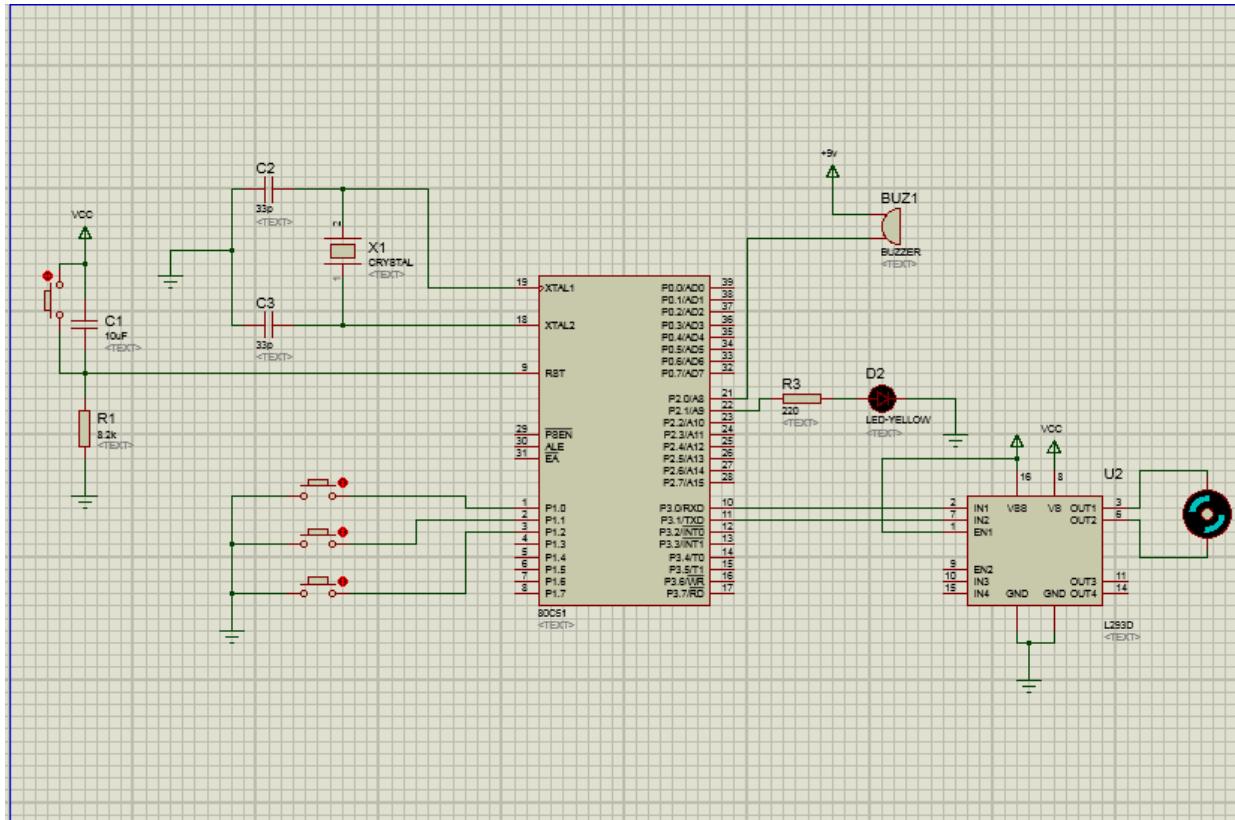


Figure 5.2: Interfacing of DC motor

6. Results

After testing each and every module individually we have integrated them into the final project which consists of an IR sensor at its input side and LED, buzzer and motor at its output side.

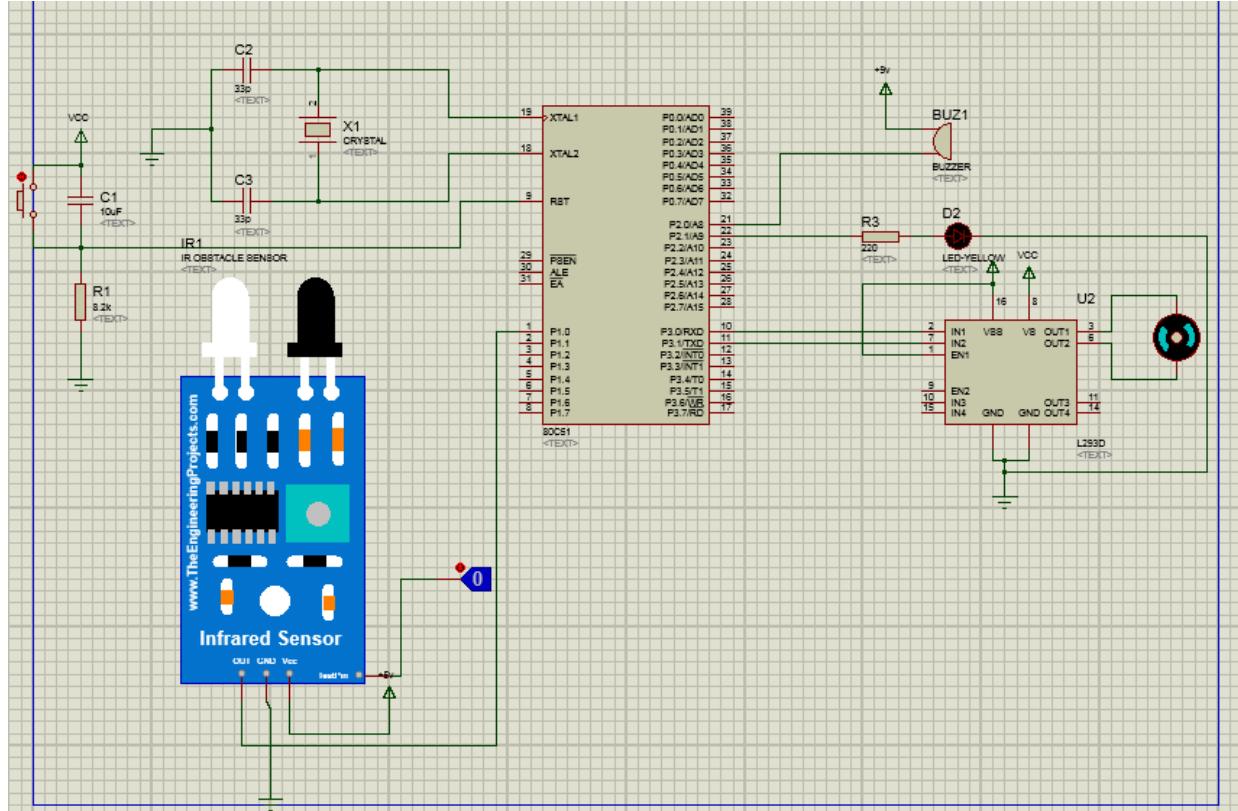


Figure 6.1: Final view of a project

6.1 Advantages and Applications:

Advantages:

1. Low cost.
2. Simple to use.
3. No Special training is required for user in order to use this product.
4. Easy to handle and portable.

Applications:

1. Robotics sensing arm.
2. Counting people / people detection.
3. Obstacle detection.

6.2 Conclusion:

Blind people need constant assistance to do their daily chores. The Third Eye for Blind is a device helpful for the blind to do their work independently in an indoor environment. It is developed to help the blind to overcome the lack of visual sense by using other senses like sound and touch. A combination of a microcontroller 80C51 and an Infrared (IR) sensor are used as inputs to calculate the distance of the obstacle from the blind person and another combination of vibrator motor and buzzer are used to indicate the person about the obstacle. Thus, an IR Sensor is used to detect the obstacle which is very efficient and accurate. The removable microcontroller 80C51 is used for processing the information obtained from the IR sensor and finally, output is received through three devices LED, Buzzer and Vibrator motor in the form of sound and touch. Thus, a simple, cheap, efficient, easy to carry, configurable, easy to handle electronic guidance system is developed to provide constructive assistance for the blind. With this system, if constructed with at-most accuracy, the blind people will be able to move without others help.

6.3 Future Scope:

In today ‘s world, disability of any kind for any person can be hard and it is the same case with blindness. Blind people are generally left underprivileged. It is very difficult to give a vision to a blind person. So, our Future work will be focused on enhancing the performance of the system and reducing the load on the user by adding the camera to guide the blind exactly. Images acquired by using web camera and NI-smart cameras helps in identification of objects as well as scans the entire instances for the presence of number of objects in the path of the blind person. It can also detect the material and shape of the object. Matching percentage has to be nearly all the time correct as there no chance for correction for a blind person if it is to be trusted and reliable one. The principles of mono pulse radar can be utilized for determining long range target objects. The other scope may include a new concept of optimum and safe path detection based on neural networks for a blind person.

6.4 References:

[1] V. Diana Earshia, S.M Kalaivanan, K. Bala Subramanian “A Wearable Ultrasonic Obstacle Sensor for Aiding Visually Impaired and Blind Individuals.” International Journal of Computer Applications, National Conference on Growth of Technologies in Electronics January 2016

[2] G Dhiraj, S Pankhuri, et al. Design and development of a low-cost Electronic Hand Glove for deaf and blind, International Conference on Computing for Sustainable Global Development

2015

[3] Proceedings of International Conference on Circuits, Communication, Control and Computing (I4C 2014) Voice Assisted Navigation System for the Blind by Ananth Noorithaya1, Kishore Kumar M.3 and Dr. Sreedevi A

[4] Shraga Shovel, Iwan Ulrich, Johann Borenstien, Nav Belt and the Guide Cane, IEEE Transactions on Robotics & Automation. 2003; 10(1):9-20.

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[6] Hugo Fernandesc, João Barroso "Blind Guide: an ultrasound sensor-based body area network for guiding blind people ",6th International Conference on Software Development and Technologies for Enhancing Accessibility and Fighting Infoexclusion (DSAI 2015)

[7] Sabarish S. Navigation Tool for Visually Challenged using Microcontroller, International Journal of Engineering and Advanced Technology (IJEAT), 2013; 2(4):139-143.

[8] Espinosa MA, Ungar S, Ochaíta E. Blades comparing methods for Introducing Blind and Visually Impaired People to unfamiliar urban environments., Journal of Environmental psychology. 1998; 18:277-287.

[9] Pooja Sharma, Shimi SL, Chatterji S. A Review on Obstacle Detection and Vision, International Journal of Science and Research Technology. 2015; 4(1):1-11.

7. Appendix

7.1 Bill of materials:

Sr. No	COMPONENT	QUANTITY	PRICE
1.	80C51 MICROCONTROLLER	1	₹165.00
2.	INFRARED SENSOR	1	₹58.00
3.	DC MOTOR	1	₹45.00
4.	BUZZER	1	₹15.00
5.	VOLTAGE REGULATOR 7805	1	₹09.00
6.	LED	1	₹08.00
7.	WIRE	1	₹35.00
8.	IC SOCKETS	1	₹11.00
9.	PCB	1	₹175.00
10.	GLOVES	1	₹299.00
		TOTAL	₹820.00

7.2 Datasheets:

DATA SHEET

80C51/87C51/80C52/87C52

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V), low power, high speed (33 MHz), 128/256 B RAM

Product specification

2000 Aug 07

Replaces datasheet 80C51/87C51/80C31 of 2000 Jan 20

80C51 8-bit microcontroller family 4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V), low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

DESCRIPTION

The Philips 80C51/87C51/80C52/87C52 is a high-performance static 80C51 design fabricated with Philips high-density CMOS technology with operation from 2.7 V to 5.5 V.

The 8xC51 and 8xC52 contain a 128×8 RAM and 256×8 RAM respectively, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device is a low power static design which offers a wide range of operating frequencies down to zero. Two software selectable modes of power reduction—idle mode and power-down mode are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.

SELECTION TABLE

For applications requiring more ROM and RAM, see the 8XC54/58 and 8XC51RA+/RB+/RC+/80C51RA+ data sheet.

Note: 80C31/80C32 is specified in separate data sheet.

ROM/EPROM Memory Size (X by 8)	RAM Size (X by 8)	Programmable Timer Counter (PCA)	Hardware Watch Dog Timer
80C31*/80C51/87C51			
0K/4K	128	No	No
80C32*/80C52/87C52			
0K/8K/16K/32K	256	No	No
80C51RA+/8XC51RA+/RB+/RC+			
0K/8K/16K/32K	512	Yes	Yes
8XC51RD+			
64K	1024	Yes	Yes

FEATURES

- 8051 Central Processing Unit
 - $4k \times 8$ ROM (80C51)
 - $8k \times 8$ ROM (80C52)
 - 128×8 RAM (80C51)
 - 256×8 RAM (80C52)
 - Three 16-bit counter/timers
 - Boolean processor
 - Full static operation
 - Low voltage (2.7 V to 5.5 V@ 16 MHz) operation
- Memory addressing capability
 - 64k ROM and 64k RAM
- Power control modes:
 - Clock can be stopped and resumed
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- TWO speed ranges at $V_{CC} = 5$ V
 - 0 to 16 MHz
 - 0 to 33 MHz
- Three package styles
- Extended temperature ranges
- Dual Data Pointers
- Security bits:
 - ROM (2 bits)
 - OTP/EPROM (3 bits)
- Encryption array – 64 bytes
- 4 level priority interrupt
- 6 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Programmable clock out
- Asynchronous port reset
- Low EMI (inhibit ALE and slew rate controlled outputs)
- Wake-up from Power Down by an external interrupt

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52**80C51/87C51 ORDERING INFORMATION**

	MEMORY SIZE 4K × 8	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DWG. #
ROM	P80C51SBPN	0 to +70, Plastic Dual In-line Package	2.7 V to 5.5 V	0 to 16	SOT129-1
OTP	P87C51SBPN				
ROM	P80C51SBAA	0 to +70, Plastic Leaded Chip Carrier	2.7 V to 5.5 V	0 to 16	SOT187-2
OTP	P87C51SBAA				
ROM	P80C51SBBB	0 to +70, Plastic Quad Flat Pack	2.7 V to 5.5 V	0 to 16	SOT307-2
OTP	P87C51SBBB				
ROM	P80C51SFPN	−40 to +85, Plastic Dual In-line Package	2.7 V to 5.5 V	0 to 16	SOT129-1
OTP	P87C51SFPN				
ROM	P80C51SFA A	−40 to +85, Plastic Leaded Chip Carrier	2.7 V to 5.5 V	0 to 16	SOT187-2
OTP	P87C51SFA A				
ROM	P80C51SFBB	−40 to +85, Plastic Quad Flat Pack	2.7 V to 5.5 V	0 to 16	SOT307-2
OTP	P87C51SFBB				
ROM	P80C51UBAA	0 to +70, Plastic Leaded Chip Carrier	5 V	0 to 33	SOT187-2
OTP	P87C51UBAA				
ROM	P80C51UBPN	0 to +70, Plastic Dual In-line Package	5 V	0 to 33	SOT129-1
OTP	P87C51UBPN				
ROM	P80C51UFAA	−40 to +85, Plastic Leaded Chip Carrier	5 V	0 to 33	SOT187-2
OTP	P87C51UFAA				

PART NUMBER DERIVATION

DEVICE NUMBER	DEVICE NUMBER	OPERATING FREQUENCY, MAX (S)	TEMPERATURE RANGE (B)	PACKAGE (AA)
ROM	P80C51	S = 16 MHz	B = 0° to +70°C	AA = PLCC
ROM	P80C52	S = 16 MHz	B = 0° to +70°C	AA = PLCC
OTP	P87C51	U = 33 MHz	F = −40°C to +85°C	BB = PQFP
OTP	P87C52	U = 33 MHz	F = −40°C to +85°C	BB = PQFP

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52**80C52/87C52 ORDERING INFORMATION**

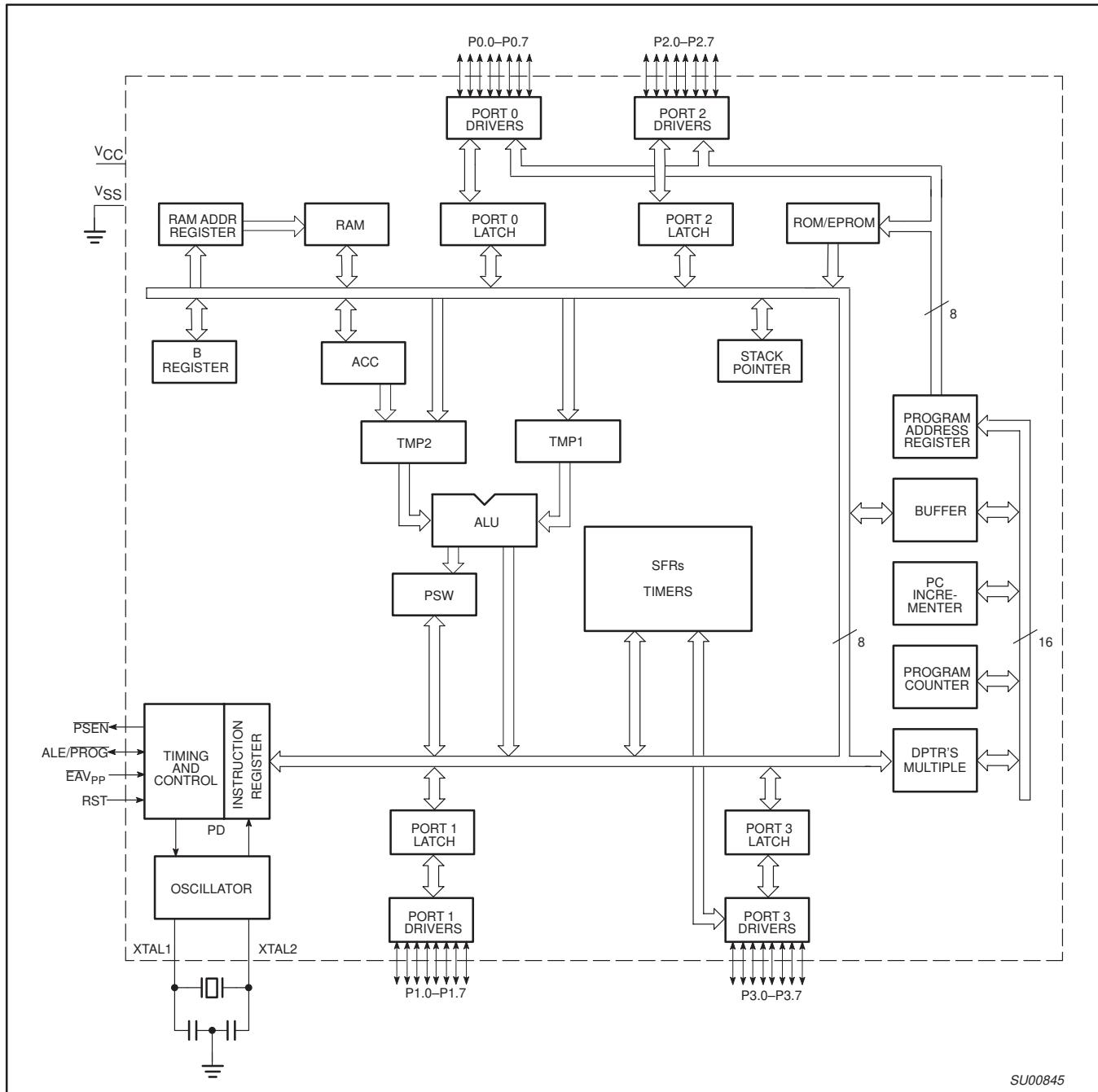
	MEMORY SIZE 8K × 8	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DWG. #
ROM	P80C52SBPN	0 to +70, Plastic Dual In-line Package	2.7 V to 5.5 V	0 to 16	SOT129-1
OTP	P87C52SBPN				
ROM	P80C52SBAA	0 to +70, Plastic Leaded Chip Carrier	2.7 V to 5.5 V	0 to 16	SOT187-2
OTP	P87C52SBAA				
ROM	P80C52SBBB	0 to +70, Plastic Quad Flat Pack	2.7 V to 5.5 V	0 to 16	SOT307-2
OTP	P87C52SBBB				
ROM	P80C52SF PN	–40 to +85, Plastic Dual In-line Package	2.7 V to 5.5 V	0 to 16	SOT129-1
OTP	P87C52SF PN				
ROM	P80C52SFA A	–40 to +85, Plastic Leaded Chip Carrier	2.7 V to 5.5 V	0 to 16	SOT187-2
OTP	P87C52SFA A				
ROM	P80C52SF BB	–40 to +85, Plastic Quad Flat Pack	2.7 V to 5.5 V	0 to 16	SOT307-2
OTP	P87C52SF BB				
ROM	P80C52UBAA	0 to +70, Plastic Leaded Chip Carrier	5 V	0 to 33	SOT187-2
OTP	P87C52UBAA				
ROM	P80C52UB PN	0 to +70, Plastic Dual In-line Package	5 V	0 to 33	SOT129-1
OTP	P87C52UB PN				
ROM	P80C52UFA A	–40 to +85, Plastic Leaded Chip Carrier	5 V	0 to 33	SOT187-2
OTP	P87C52UFA A				

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

BLOCK DIAGRAM

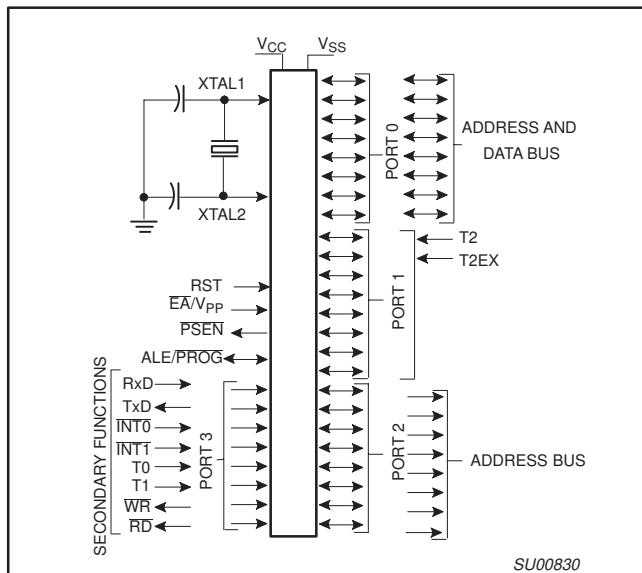


80C51 8-bit microcontroller family

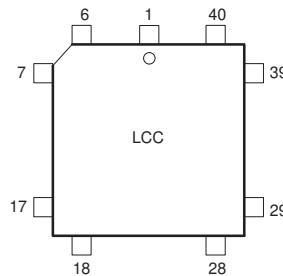
4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

LOGIC SYMBOL



PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

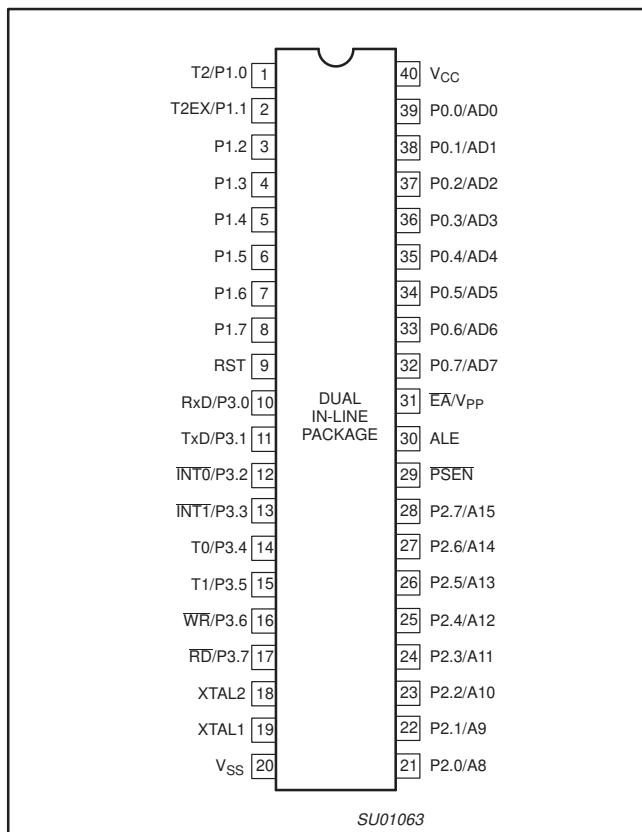


Pin	Function	Pin	Function	Pin	Function
1	NIC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	PSEN
3	P1.1/T2EX	18	P3.6/WR	33	ALE
4	P1.2	19	P3.7/RD	34	NIC*
5	P1.3	20	XTAL2	35	EA/V _{PP}
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	V _{SS}	37	P0.6/AD6
8	P1.6	23	NIC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/INT0	29	P2.5/A13	44	V _{CC}
15	P3.3/INT1	30	P2.6/A14		

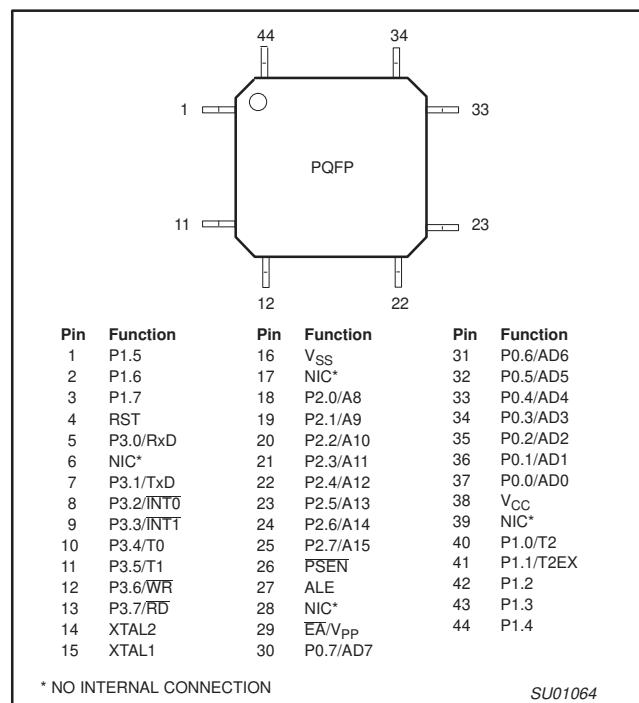
* NO INTERNAL CONNECTION

SU01062

PIN CONFIGURATIONS



PLASTIC QUAD FLAT PACK PIN FUNCTIONS



80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
V _{SS}	20	22	16	I	Ground: 0 V reference.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port with Schmitt trigger inputs. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups and Schmitt trigger inputs. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include: T2 (P1.0): Timer/Counter 2 external count input/clockout (see Programmable Clock-Out) T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	21–28	24–31	18–25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups and Schmitt trigger inputs. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @R _i), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups and Schmitt trigger inputs. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below: 10 11 5 I RxD (P3.0): Serial input port 11 13 7 O TxD (P3.1): Serial output port 12 14 8 I INT0 (P3.2): External interrupt 13 15 9 I INT1 (P3.3): External interrupt 14 16 10 I T0 (P3.4): Timer 0 external input 15 17 11 I T1 (P3.5): Timer 1 external input 16 18 12 O WR (P3.6): External data memory write strobe 17 19 13 O RD (P3.7): External data memory read strobe
RST	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE/PROG	30	33	27	O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR auxiliary 0. With this bit set, ALE will be active only during a MOVX instruction.
PSEN	29	32	26	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/V _{PP}	31	35	29	I	External Access Enable/Programming Supply Voltage: EA must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than the on-chip ROM/OTP. This pin also receives the 12.75 V programming supply voltage (V _{PP}) during EPROM programming. If security bit 1 is programmed, EA will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5 V or V_{SS} – 0.5 V, respectively.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

Table 1. 80C51/87C51/80C52/87C52 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB								LSB
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	—	—	—	—	—	—	—	AO	xxxxxx0B
AUXR1#	Auxiliary 1	A2H	—	—	—	LPEP ²	WUPD	0	—	DPS	xx000x0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes)	83H									00H
DPH	Data Pointer High	82H									00H
DPL	Data Pointer Low										
IE*	Interrupt Enable	A8H	AF	AE	AD	AC	AB	AA	A9	A8	0x000000B
IP*	Interrupt Priority	B8H	EA	—	ET2	ES	ET1	EX1	ET0	EX0	xx000000B
IPH#	Interrupt Priority High	B7H	BF	BE	BD	BC	BB	BA	B9	B8	xx000000B
P0*	Port 0	80H	—	—	PT2	PS	PT1	PX1	PT0	PX0	
P1*	Port 1	90H	B7	B6	B5	B4	B3	B2	B1	B0	
P2*	Port 2	A0H	—	—	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	
P3*	Port 3	B0H	87	86	85	84	83	82	81	80	
PCON# ¹	Power Control	87H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
PSW*	Program Status Word	D0H	97	96	95	94	93	92	91	90	
RACAP2H#	Timer 2 Capture High	CBH	—	—	—	—	—	—	T2EX	T2	FFH
RACAP2L#	Timer 2 Capture Low	CAH	A7	A6	A5	A4	A3	A2	A1	A0	
SADDR#	Slave Address	A9H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
SADEN#	Slave Address Mask	B9H	B7	B6	B5	B4	B3	B2	B1	B0	
SBUF	Serial Data Buffer	99H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
SCON*	Serial Control	87H	SMOD1	SMOD0	—	POF	GF1	GF0	PD	IDL	00xx000B
SP	Stack Pointer	81H	D7	D6	D5	D4	D3	D2	D1	D0	00000x0B
TCON*	Timer Control	88H	CY	AC	F0	RS1	RS0	OV	—	P	00H
T2CON*	Timer 2 Control	C8H	8F	8E	8D	8C	8B	8A	89	88	00H
T2MOD#	Timer 2 Mode Control	C9H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	xxxxxx0B
TH0	Timer High 0	8CH	CF	CE	CD	CC	CB	CA	C9	C8	00H
TH1	Timer High 1	8DH	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
TH2#	Timer High 2	CDH	—	—	—	—	—	—	T2OE	DCEN	00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

NOTE:

Unused register bits that are not defined should not be set by the user's program. If violated, the device could function incorrectly.

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

— Reserved bits.

1. Reset value depends on reset source.

2. LPEP – Low Power EPROM operation (OTP/EPROM only)

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52**OSCILLATOR CHARACTERISTICS**

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

For the 87C51 and 80C51 either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all

the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values. WUPD (AUXR1.3—Wakeup from Power Down) enables or disables the wakeup from power down with external interrupt.

Where:

WUPD = 0 Disable
WUPD = 1 Enable

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

LPEP

The eprom array contains some analog circuits that are not required when V_{CC} is less than 4 V, but are required for a V_{CC} greater than 4 V. The LPEP bit (AUXR.4), when set, will powerdown these analog circuits resulting in a reduced supply current. This bit should be set ONLY for applications that operate at a V_{CC} less than 4 V.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and PSEN is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and PSEN are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\text{Oscillator Frequency} = \frac{4 \times (65536 - \text{RCAP2H}, \text{RCAP2L})}{\text{Oscillator Frequency}}$$

Where:

$(\text{RCAP2H}, \text{RCAP2L})$ = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2* in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2=1, Timer 2 operates as described above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and

TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt. The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter (C/T2* in T2CON)) then programmed to count up or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0xFFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0xFFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0xFFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

Table 3. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

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(MSB)				(LSB)			
Symbol	Position	Name and Significance					
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.					
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).					
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.					
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.					
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.					
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.					
C/T2	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).					
CP/RL2	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.					

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Figure 1. Timer/Counter 2 (T2CON) Control Register

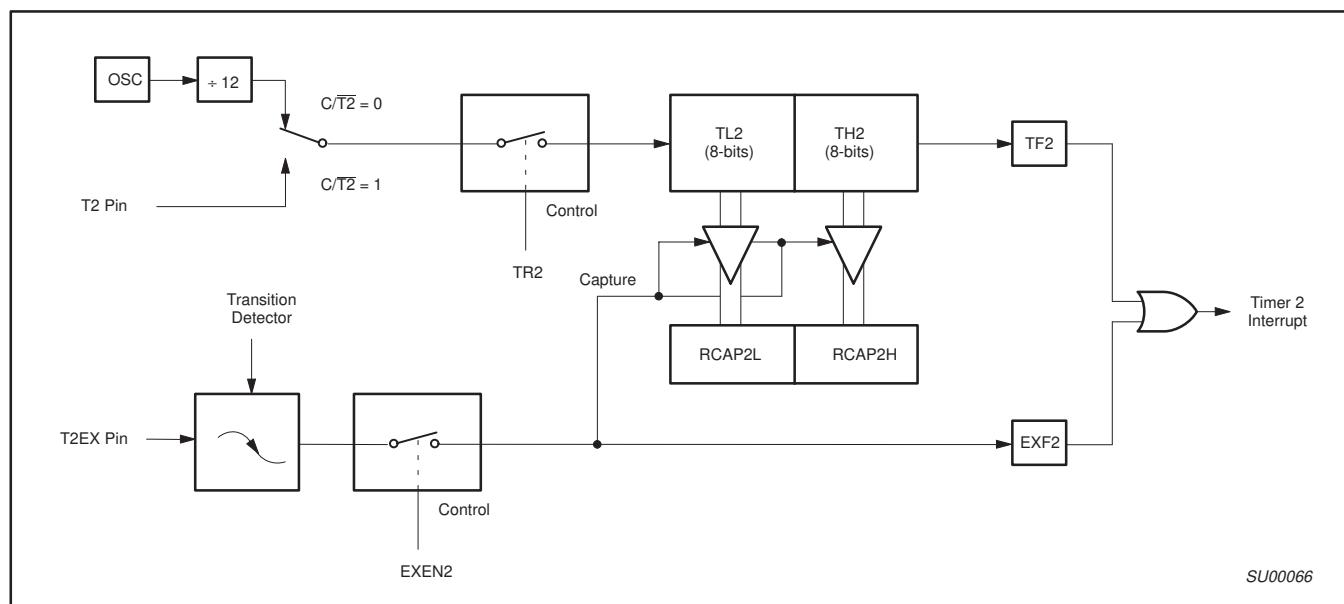


Figure 2. Timer 2 in Capture Mode

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T2MOD	Address = 0C9H	Reset Value = XXXX XX00B						
Not Bit Addressable								
Bit	7	6	5	4	3	2	1	0
Symbol			Function					
—								Not implemented, reserved for future use.*
T2OE								Timer 2 Output Enable bit.
DCEN								Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.								
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Figure 3. Timer 2 Mode (T2MOD) Control Register

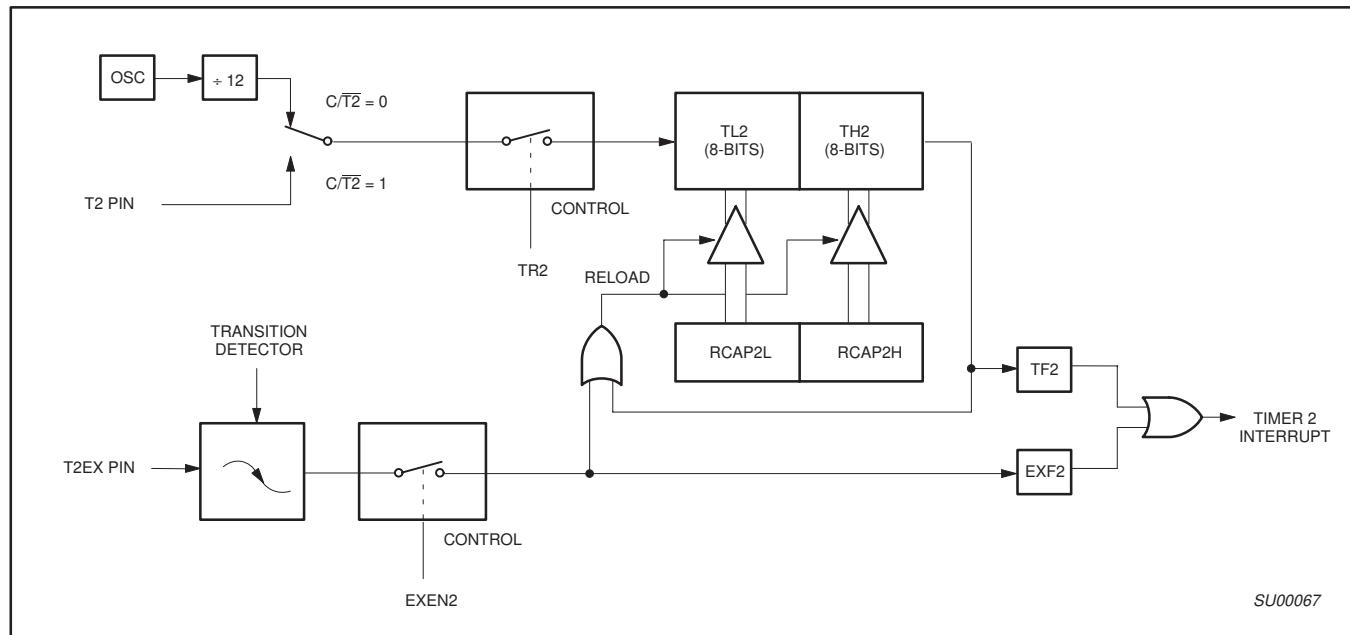


Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)

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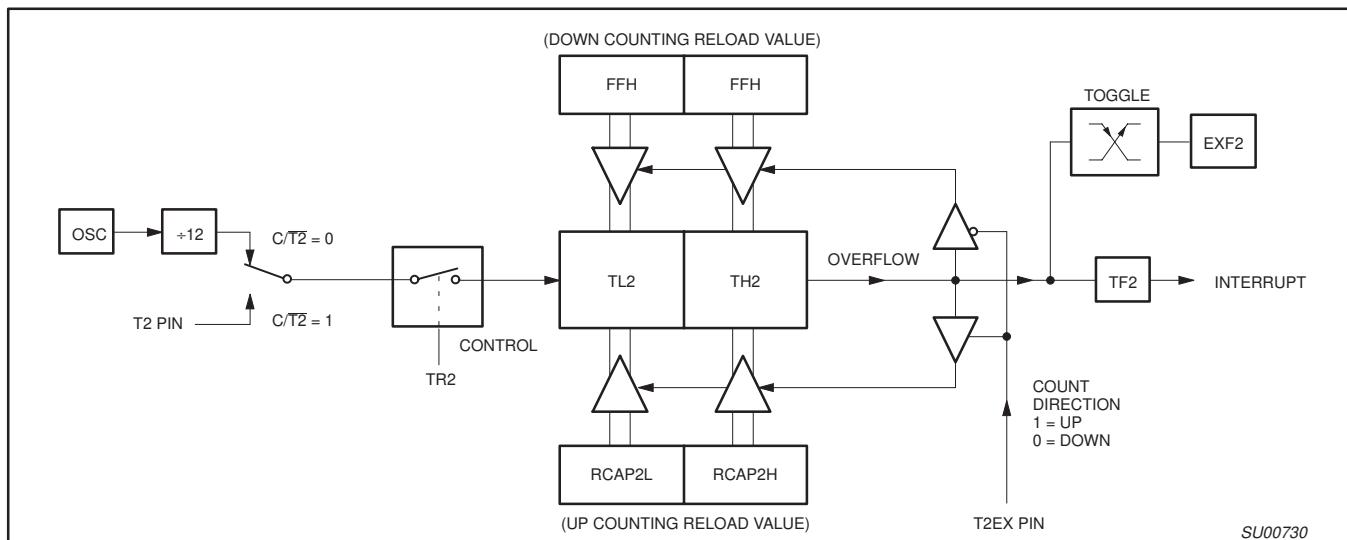


Figure 5. Timer 2 Auto Reload Mode (DCEN = 1)

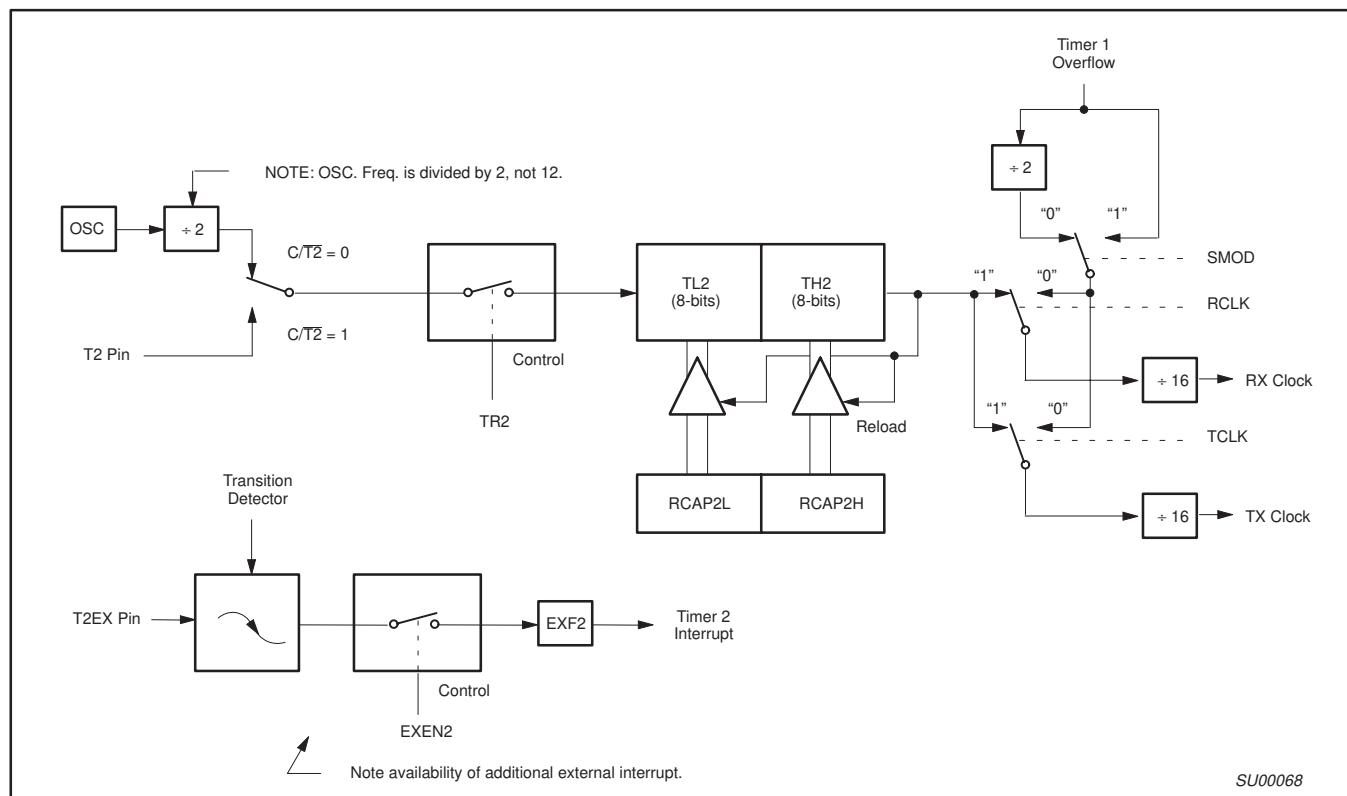


Figure 6. Timer 2 in Baud Rate Generator Mode

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80C51/87C51/80C52/87C52**Baud Rate Generator Mode**

Bits TCLK and/or RCLK in T2CON (Table 3) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 6 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/T2*=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where: ($\text{RCAP2H}, \text{RCAP2L}$)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 6, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2,TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time ($\text{osc}/2$) or asynchronously from pin T2;

under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Table 4. Timer 2 Generated Commonly Used Baud Rates

Baud Rate	Osc Freq	Timer 2	
		RCAP2H	RCAP2L
375 K	12 MHz	FF	FF
9.6 K	12 MHz	FF	D9
2.8 K	12 MHz	FF	B2
2.4 K	12 MHz	FF	64
1.2 K	12 MHz	FE	C8
300	12 MHz	FB	1E
110	12 MHz	F2	AF
300	6 MHz	FD	8F
110	6 MHz	F9	57

Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{\text{OSC}}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where f_{OSC} = Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 - \left(\frac{f_{\text{osc}}}{32 \times \text{Baud Rate}} \right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

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Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 8.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 9.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the

SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111</u> <u>1101</u>
	Given =	1100 00X0

Slave 1	SADDR =	1100 0000
	SADEN =	<u>1111</u> <u>1110</u>
	Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111</u> <u>1001</u>
	Given =	1100 0XX0

Slave 1	SADDR =	1110 0000
	SADEN =	<u>1111</u> <u>1010</u>
	Given =	1110 0X0X

Slave 2	SADDR =	1110 0000
	SADEN =	<u>1111</u> <u>1100</u>
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0

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and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are leaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

SCON Address = 98H								Reset Value = 0000 0000B						
Bit Addressable														
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI						
Bit:	7	6	5	4	3	2	1	0						
(SMOD0 = 0/1)*														
Symbol	Function													
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.													
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)													
SM1	Serial Port Mode Bit 1													
	SM0	SM1	Mode	Description	Baud Rate**									
	0	0	0	shift register	fosc/12									
	0	1	1	8-bit UART	variable									
	1	0	2	9-bit UART	fosc/64 or fosc/32									
	1	1	3	9-bit UART	variable									
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.													
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.													
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.													
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.													
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.													
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.													
NOTE:														
*SMOD0 is located at PCON6.														
**fosc = oscillator frequency														

Figure 7. SCON: Serial Port Control Register

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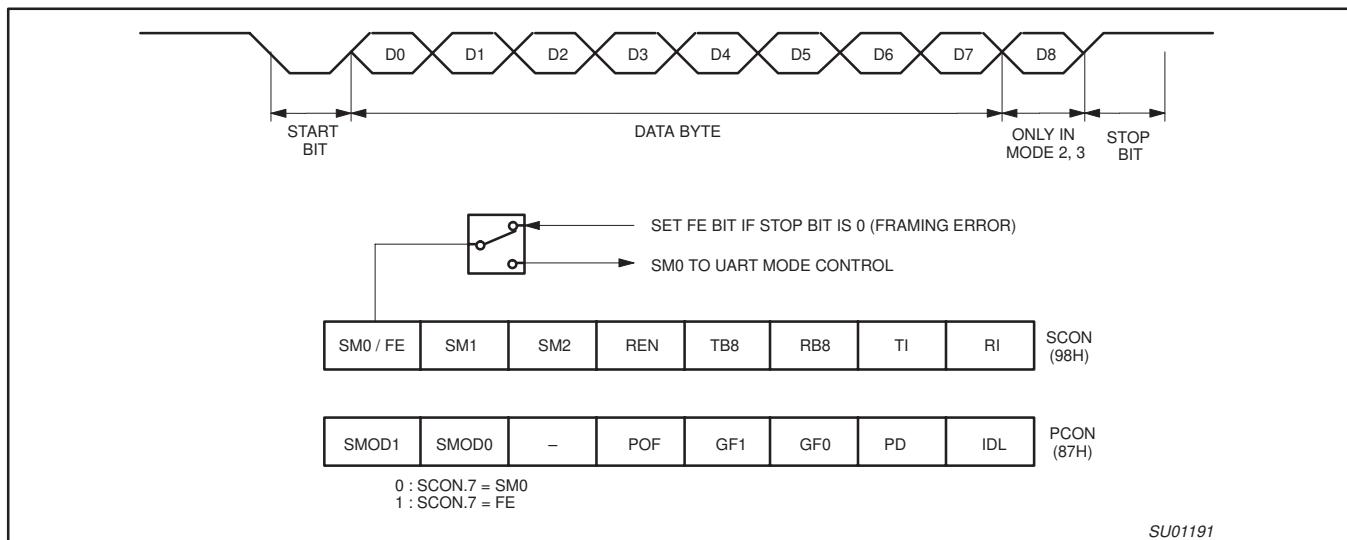


Figure 8. UART Framing Error Detection

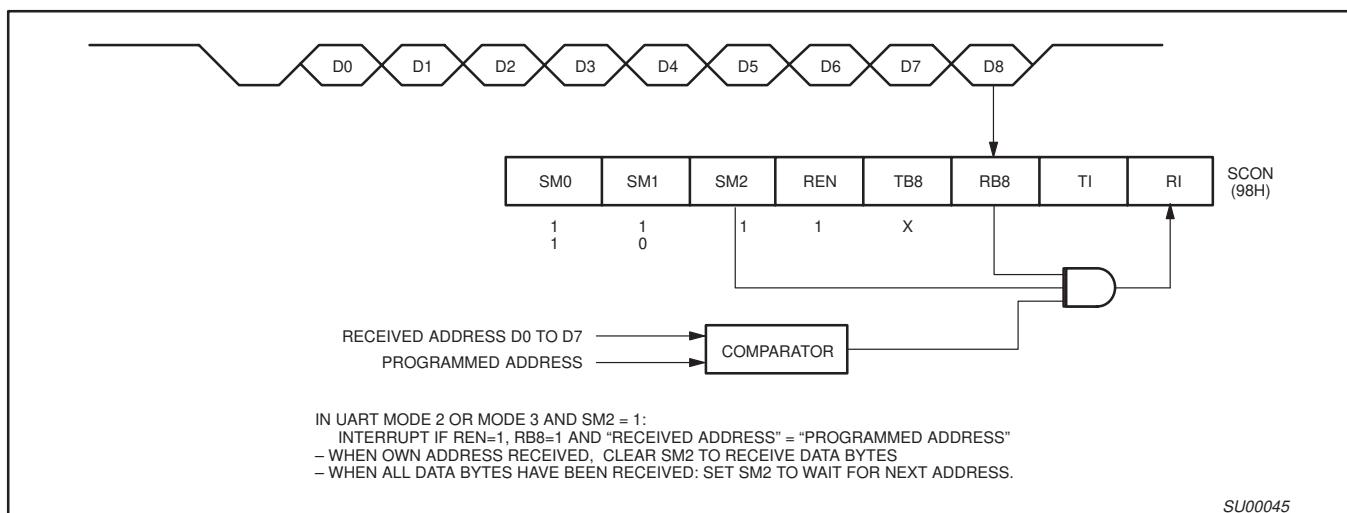


Figure 9. UART Multiprocessor Communication, Automatic Address Recognition

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80C51/87C51/80C52/87C52**Interrupt Priority Structure**

The 80C51/87C51 and 80C52/87C52 have a 6-source four-level interrupt structure. They are the IE, IP and IPH. (See Figures 10, 11, and 12.) The IPH (Interrupt Priority High) register that makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 12.

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L) ¹ Y (T) ²	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
SP	5	RI, TI	N	23H
T2	6	TF2, EXF2	N	2BH

NOTES:

1. L = Level activated
2. T = Transition activated

IE (0A8H)	7	6	5	4	3	2	1	0
	EA	—	ET2	ES	ET1	EX1	ET0	EX0
Enable Bit = 1 enables the interrupt. Enable Bit = 0 disables it.								
BIT	SYMBOL	FUNCTION						
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.						
IE.6	—	Not implemented. Reserved for future use.						
IE.5	ET2	Timer 2 interrupt enable bit.						
IE.4	ES	Serial Port interrupt enable bit.						
IE.3	ET1	Timer 1 interrupt enable bit.						
IE.2	EX1	External interrupt 1 enable bit.						
IE.1	ET0	Timer 0 interrupt enable bit.						
IE.0	EX0	External interrupt 0 enable bit.						

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Figure 10. IE Registers

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		7	6	5	4	3	2	1	0		
IP (0B8H)		—	—	PT2	PS	PT1	PX1	PT0	PX0		
Priority Bit = 1 assigns higher priority											
Priority Bit = 0 assigns lower priority											
BIT	SYMBOL	FUNCTION									
IP.7	—	Not implemented, reserved for future use.									
IP.6	—	Not implemented, reserved for future use.									
IP.5	PT2	Timer 2 interrupt priority bit.									
IP.4	PS	Serial Port interrupt priority bit.									
IP.3	PT1	Timer 1 interrupt priority bit.									
IP.2	PX1	External interrupt 1 priority bit.									
IP.1	PT0	Timer 0 interrupt priority bit.									
IP.0	PX0	External interrupt 0 priority bit.									

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Figure 11. IP Registers

		7	6	5	4	3	2	1	0		
IPH (B7H)		—	—	PT2H	PSH	PT1H	PX1H	PT0H	PX0H		
Priority Bit = 1 assigns higher priority											
Priority Bit = 0 assigns lower priority											
BIT	SYMBOL	FUNCTION									
IPH.7	—	Not implemented, reserved for future use.									
IPH.6	—	Not implemented, reserved for future use.									
IPH.5	PT2H	Timer 2 interrupt priority bit high.									
IPH.4	PSH	Serial Port interrupt priority bit high.									
IPH.3	PT1H	Timer 1 interrupt priority bit high.									
IPH.2	PX1H	External interrupt 1 priority bit high.									
IPH.1	PT0H	Timer 0 interrupt priority bit high.									
IPH.0	PX0H	External interrupt 0 priority bit high.									

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Figure 12. IPH Registers

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80C51/87C51/80C52/87C52**Reduced EMI**

All port pins of the 8xC51 and 8xC52 have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

AUXR (8EH)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	AO

AUXR.0 AO Turns off ALE output.

Dual DPTR

The dual DPTR structure (see Figure 13) enables a way to specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxx000x0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
—	—	—	LPEP	WUPD	0	—	DPS

Where:

DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC DPTR instruction without affecting the WOPD or LPEP bits.

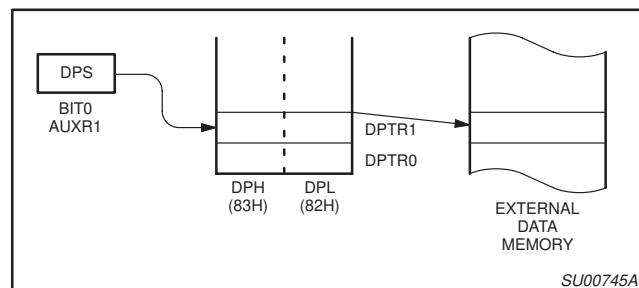


Figure 13.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR , A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See application note AN458 for more details.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on EA/V _{PP} pin to V _{SS}	0 to +13.0	V
Voltage on any other pin to V _{SS}	-0.5 to +6.5	V
Maximum I _{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or -40°C to +85°C

SYMBOL	FIGURE	PARAMETER	CLOCK FREQUENCY RANGE -f		UNIT
			MIN	MAX	
1/t _{CLCL}	29	Oscillator frequency Speed versions : S (16 MHz) U (33 MHz)	0 0	16 33	MHz MHz

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
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80C51/87C51/80C52/87C52

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -40°C to $+85^\circ\text{C}$, $V_{CC} = 2.7 \text{ V}$ to 5.5 V , $V_{SS} = 0 \text{ V}$ (16 MHz devices)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage ¹¹	$4.0 \text{ V} < V_{CC} < 5.5 \text{ V}$	-0.5		$0.2 V_{CC} - 0.1$	V
		$2.7 \text{ V} < V_{CC} < 4.0 \text{ V}$	-0.5		0.7	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, \overline{EA})			$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$
V_{IH1}	Input high voltage, XTAL1, RST ¹¹			$0.7 V_{CC}$		$V_{CC} + 0.5$
V_{OL}	Output low voltage, ports 1, 2, 8	$V_{CC} = 2.7 \text{ V}$ $I_{OL} = 1.6 \text{ mA}^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{8, 7}	$V_{CC} = 2.7 \text{ V}$ $I_{OL} = 3.2 \text{ mA}^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 2.7 \text{ V}$ $I_{OH} = -20 \mu\text{A}$		$V_{CC} - 0.7$		V
		$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -80 \mu\text{A}$		$V_{CC} - 0.7$		V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 2.7 \text{ V}$ $I_{OH} = -3.2 \text{ mA}$		$V_{CC} - 0.7$		V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4 \text{ V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0 \text{ V}$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 21): Active mode @ 16 MHz Idle mode @ 16 MHz Power-down mode or clock stopped (see Figure 25 for conditions)	See note 5				μA
		$T_{amb} = 0^\circ\text{C}$ to 70°C $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		3	50 75	μA
R_{RST}	Internal reset pull-down resistor		40		225	$\text{k}\Omega$
C_{IO}	Pin capacitance ¹⁰ (except \overline{EA})				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100 \text{ pF}$), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $V_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 22 through 25 for I_{CC} test conditions.
Active mode: $I_{CC} = 0.9 \times \text{FREQ.} + 1.1 \text{ mA}$
Idle mode: $I_{CC} = 0.18 \times \text{FREQ.} + 1.01 \text{ mA}$; See Figure 21.
- This value applies to $T_{amb} = 0^\circ\text{C}$ to $+70^\circ\text{C}$. For $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $I_{TL} = -750 \mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85°C specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except \overline{EA} is 25 pF).
- To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the INT0 and INT1 pins. Previous devices provided only an inherent 5 ns of glitch rejection.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -40°C to $+85^\circ\text{C}$, 33 MHz devices; $5 \text{ V} \pm 10\%$; $V_{SS} = 0 \text{ V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage ¹¹	$4.5 \text{ V} < V_{CC} < 5.5 \text{ V}$	-0.5		$0.2 \text{ V}_{CC} - 0.1$	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{\text{EA}}$)			$0.2 \text{ V}_{CC} + 0.9$	$\text{V}_{CC} + 0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST ¹¹			0.7 V_{CC}	$\text{V}_{CC} + 0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3 ⁸	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 1.6 \text{ mA}^2$			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN ^{7, 8}	$V_{CC} = 4.5 \text{ V}$ $I_{OL} = 3.2 \text{ mA}^2$			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 ³	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -30 \mu\text{A}$	$\text{V}_{CC} - 0.7$			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE ⁹ , PSEN ³	$V_{CC} = 4.5 \text{ V}$ $I_{OH} = -3.2 \text{ mA}$	$\text{V}_{CC} - 0.7$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.4 \text{ V}$	-1		-50	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3 ⁶	$V_{IN} = 2.0 \text{ V}$ See note 4			-650	μA
I_{LI}	Input leakage current, port 0	$0.45 < V_{IN} < V_{CC} - 0.3$			± 10	μA
I_{CC}	Power supply current (see Figure 21): Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 25 for conditions)	See note 5 $T_{amb} = 0^\circ\text{C}$ to 70°C $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		3	50 75	μA μA
R_{RST}	Internal reset pull-down resistor		40		225	k Ω
C_{IO}	Pin capacitance ¹⁰ (except $\overline{\text{EA}}$)				15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading $> 100 \text{ pF}$), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $\text{V}_{CC} - 0.7$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
- See Figures 22 through 25 for I_{CC} test conditions.
Active mode: $I_{CC(\text{MAX})} = 0.9 \times \text{FREQ.} + 1.1 \text{ mA}$
Idle mode: $I_{CC(\text{MAX})} = 0.18 \times \text{FREQ.} + 1.0 \text{ mA}$; See Figure 21.
- This value applies to $T_{amb} = 0^\circ\text{C}$ to $+70^\circ\text{C}$. For $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $I_{TL} = -750 \mu\text{A}$.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85°C specification.)
Maximum I_{OL} per 8-bit port: 26 mA
Maximum total I_{OL} for all outputs: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to V_{OH1} , except when ALE is off then V_{OH} is the voltage specification.
- Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\overline{\text{EA}}$ is 25 pF).
- To improve noise rejection a nominal 100 ns glitch rejection circuitry has been added to the RST pin, and a nominal 15 ns glitch rejection circuitry has been added to the INT0 and INT1 pins. Previous devices provided only an inherent 5 ns of glitch rejection.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or -40°C to +85°C, $V_{CC} = +2.7$ V to +5.5 V, $V_{SS} = 0$ V^{1, 2, 3}

SYMBOL	FIGURE	PARAMETER	16 MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
1/t _{CLCL}	14	Oscillator frequency ⁵ Speed versions :S			3.5	16	MHz
t _{LHLL}	14	ALE pulse width	85		2t _{CLCL} -40		ns
t _{AVLL}	14	Address valid to ALE low	22		t _{CLCL} -40		ns
t _{LLAX}	14	Address hold after ALE low	32		t _{CLCL} -30		ns
t _{LLIV}	14	ALE low to valid instruction in		150		4t _{CLCL} -100	ns
t _{LLPL}	14	ALE low to PSEN low	32		t _{CLCL} -30		ns
t _{PLPH}	14	PSEN pulse width	142		3t _{CLCL} -45		ns
t _{PLIV}	14	PSEN low to valid instruction in		82		3t _{CLCL} -105	ns
t _{PXIX}	14	Input instruction hold after PSEN	0		0		ns
t _{PXIZ}	14	Input instruction float after PSEN		37		t _{CLCL} -25	ns
t _{AVIV} ⁴	14	Address to valid instruction in		207		5t _{CLCL} -105	ns
t _{PLAZ}	14	PSEN low to address float		10		10	ns
Data Memory							
t _{RLRH}	15, 16	RD pulse width	275		6t _{CLCL} -100		ns
t _{WLWH}	15, 16	WR pulse width	275		6t _{CLCL} -100		ns
t _{RLDV}	15, 16	RD low to valid data in		147		5t _{CLCL} -165	ns
t _{RHDX}	15, 16	Data hold after RD	0		0		ns
t _{RHDZ}	15, 16	Data float after RD		65		2t _{CLCL} -60	ns
t _{LLDV}	15, 16	ALE low to valid data in		350		8t _{CLCL} -150	ns
t _{AVDV}	15, 16	Address to valid data in		397		9t _{CLCL} -165	ns
t _{LLWL}	15, 16	ALE low to RD or WR low	137	239	3t _{CLCL} -50	3t _{CLCL} +50	ns
t _{AVWL}	15, 16	Address valid to WR low or RD low	122		4t _{CLCL} -130		ns
t _{QVWX}	15, 16	Data valid to WR transition	13		t _{CLCL} -50		ns
t _{WHQX}	15, 16	Data hold after WR	13		t _{CLCL} -50		ns
t _{QVWH}	16	Data valid to WR high	287		7t _{CLCL} -150		ns
t _{RLAZ}	15, 16	RD low to address float		0		0	ns
t _{WHLH}	15, 16	RD or WR high to ALE high	23	103	t _{CLCL} -40	t _{CLCL} +40	ns
External Clock							
t _{CHCX}	18	High time	20		20	t _{CLCL} -t _{CLCX}	ns
t _{CLCX}	18	Low time	20		20	t _{CLCL} -t _{CHCX}	ns
t _{CLCH}	18	Rise time		20		20	ns
t _{CHCL}	18	Fall time		20		20	ns
Shift Register							
t _{XLXL}	17	Serial port clock cycle time	750		12t _{CLCL}		ns
t _{QVXH}	17	Output data setup to clock rising edge	492		10t _{CLCL} -133		ns
t _{XHQX}	17	Output data hold after clock rising edge	8		2t _{CLCL} -117		ns
t _{XHDX}	17	Input data hold after clock rising edge	0		0		ns
t _{XHDV}	17	Clock rising edge to input data valid		492		10t _{CLCL} -133	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Interfacing the 87C51, 80C51, 87C52, or 80C52 to devices with float times up to 45 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- See application note AN457 for external memory interface.
- Parts are guaranteed to operate down to 0 Hz. When an external clock source is used, the RST pin should be held high for a minimum of 20 µs for power-on or wakeup from power down.

80C51 8-bit microcontroller family

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80C51/87C51/80C52/87C52

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or -40°C to +85°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V^{1, 2, 3}

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK ⁴ 16 MHz to f_{max}		33 MHz ζ CLOCK		UNIT
			MIN	MAX	MIN	MAX	
t_{LHLL}	14	ALE pulse width	$2t_{CLCL}-40$		21		ns
t_{AVLL}	14	Address valid to ALE low	$t_{CLCL}-25$		5		ns
t_{LLAX}	14	Address hold after ALE low	$t_{CLCL}-25$				ns
t_{LLIV}	14	ALE low to valid instruction in		$4t_{CLCL}-65$		55	ns
t_{LLPL}	14	ALE low to PSEN low	$t_{CLCL}-25$		5		ns
t_{PLPH}	14	PSEN pulse width	$3t_{CLCL}-45$		45		ns
t_{PLIV}	14	PSEN low to valid instruction in		$3t_{CLCL}-60$		30	ns
t_{PXIX}	14	Input instruction hold after PSEN	0		0		ns
t_{PXIZ}	14	Input instruction float after PSEN		$t_{CLCL}-25$		5	ns
t_{AVIV}	14	Address to valid instruction in		$5t_{CLCL}-80$		70	ns
t_{PLAZ}	14	PSEN low to address float		10		10	ns
Data Memory							
t_{RLRH}	15, 16	RD pulse width	$6t_{CLCL}-100$		82		ns
t_{WLWH}	15, 16	WR pulse width	$6t_{CLCL}-100$		82		ns
t_{RLDV}	15, 16	RD low to valid data in		$5t_{CLCL}-90$		60	ns
t_{RHDX}	15, 16	Data hold after RD	0		0		ns
t_{RHDZ}	15, 16	Data float after RD		$2t_{CLCL}-28$		32	ns
t_{LLDV}	15, 16	ALE low to valid data in		$8t_{CLCL}-150$		90	ns
t_{AVDV}	15, 16	Address to valid data in		$9t_{CLCL}-165$		105	ns
t_{LLWL}	15, 16	ALE low to RD or WR low	$3t_{CLCL}-50$	$3t_{CLCL}+50$	40	140	ns
t_{AVWL}	15, 16	Address valid to WR low or RD low	$4t_{CLCL}-75$		45		ns
t_{QVWX}	15, 16	Data valid to WR transition	$t_{CLCL}-30$		0		ns
t_{WHQX}	15, 16	Data hold after WR	$t_{CLCL}-25$		5		ns
t_{QVWH}	16	Data valid to WR high	$7t_{CLCL}-130$		80		ns
t_{RLAZ}	15, 16	RD low to address float		0		0	ns
t_{WHLH}	15, 16	RD or WR high to ALE high	$t_{CLCL}-25$	$t_{CLCL}+25$	5	55	ns
External Clock							
t_{CHCX}	18	High time	$0.38t_{CLCL}$	$t_{CLCL}-t_{CLCX}$			ns
t_{CLCX}	18	Low time	$0.38t_{CLCL}$	$t_{CLCL}-t_{CHCX}$			ns
t_{CLCH}	18	Rise time		5			ns
t_{CHCL}	18	Fall time		5			ns
Shift Register							
t_{XLXL}	17	Serial port clock cycle time	$12t_{CLCL}$		360		ns
t_{QVXH}	17	Output data setup to clock rising edge	$10t_{CLCL}-133$		167		ns
t_{HQX}	17	Output data hold after clock rising edge	$2t_{CLCL}-80$				ns
t_{XHDX}	17	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	17	Clock rising edge to input data valid		$10t_{CLCL}-133$		167	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100 pF, load capacitance for all other outputs = 80 pF.
- Interfacing the 87C51, 80C51, 87C52 or 80C52 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
- Variable clock is specified for oscillator frequencies greater than 16 MHz to 33 MHz. For frequencies equal or less than 16 MHz, see 16 MHz "AC Electrical Characteristics", page 24.
- Parts are guaranteed to operate down to 0 Hz. When an external clock source is used, the RST pin should be held high for a minimum of 20 µs for power-on or wakeup from power down.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52**EXPLANATION OF THE AC SYMBOLS**

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A – Address
- C – Clock
- D – Input data
- H – Logic level high
- I – Instruction (program memory contents)
- L – Logic level low, or ALE

P – $\overline{\text{PSEN}}$

Q – Output data

R – $\overline{\text{RD}}$ signal

t – Time

V – Valid

W – $\overline{\text{WR}}$ signal

X – No longer a valid logic level

Z – Float

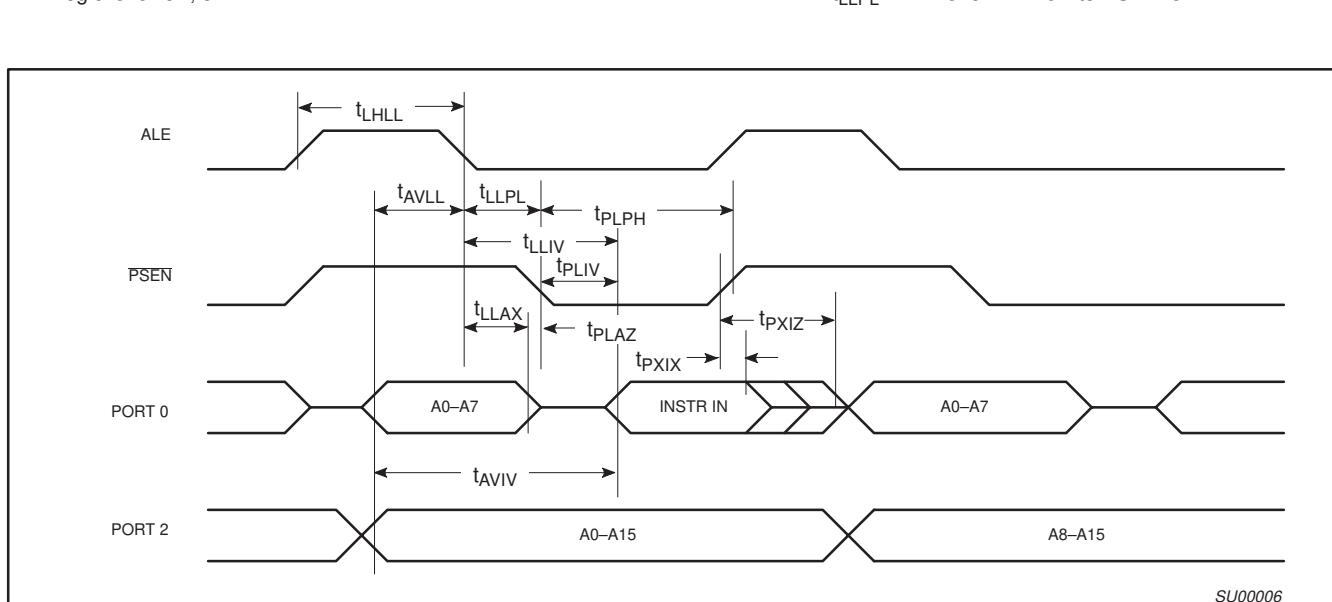
Examples: t_{AVLL} = Time for address valid to ALE low. t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

Figure 14. External Program Memory Read Cycle

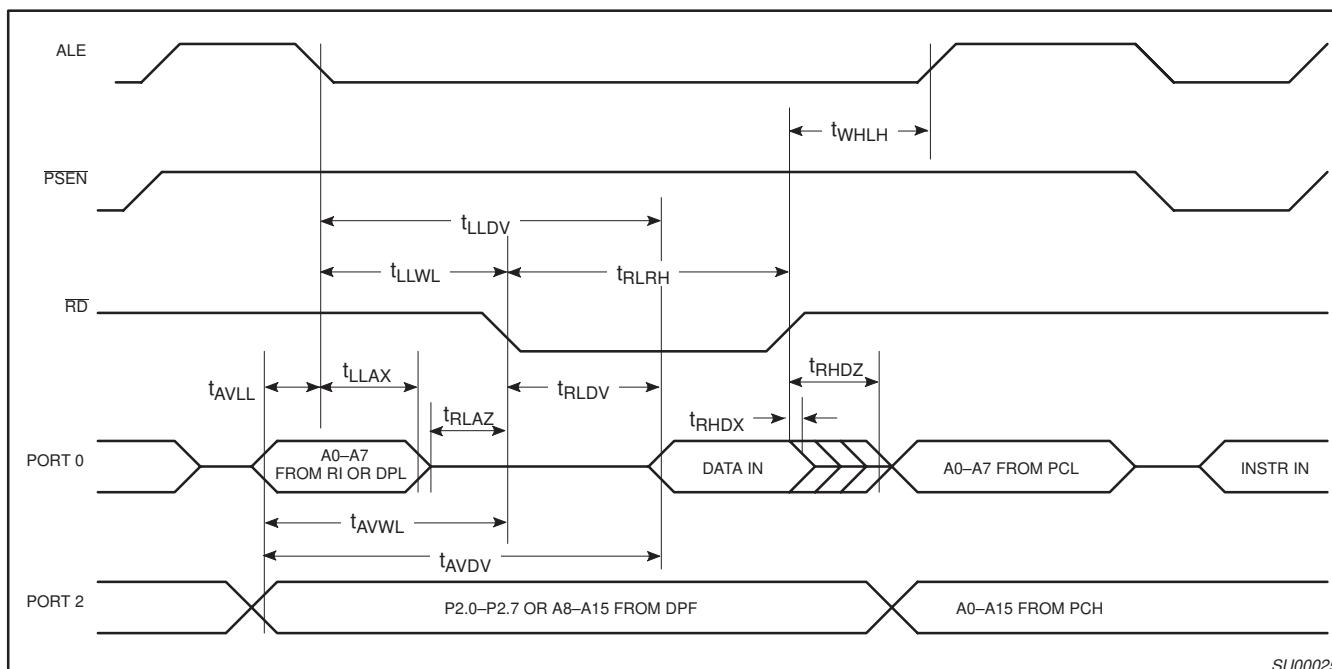


Figure 15. External Data Memory Read Cycle

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

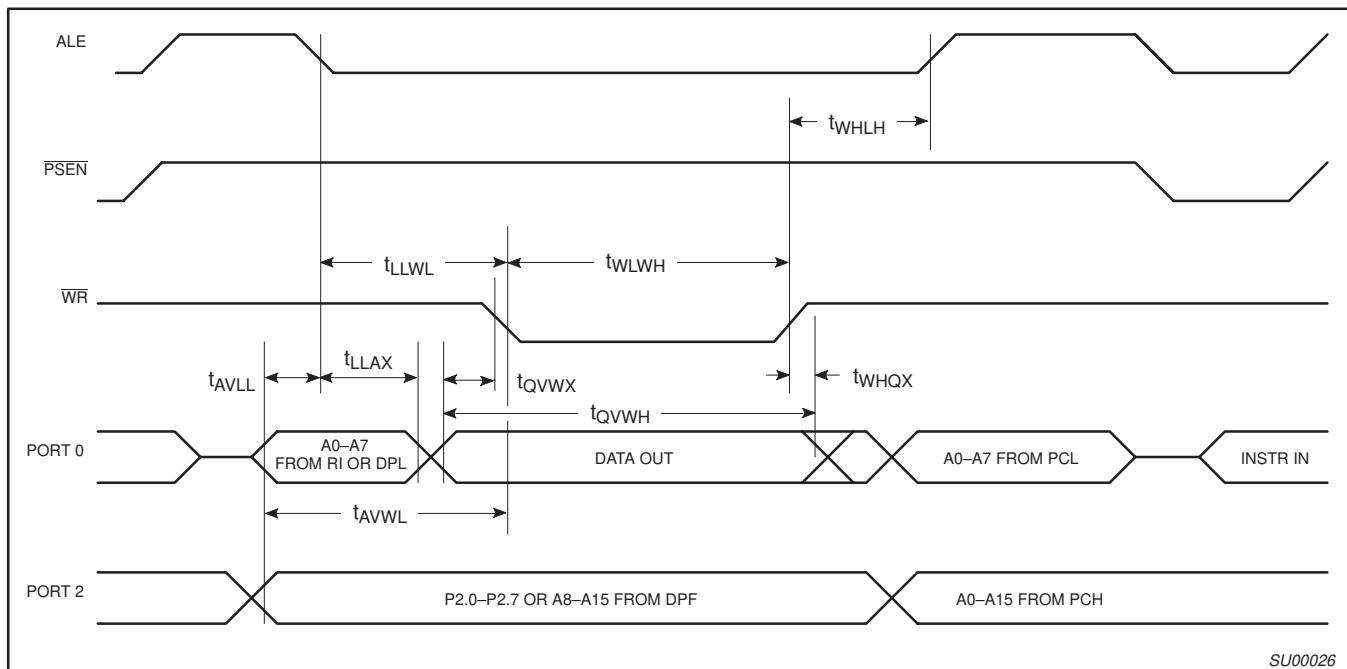


Figure 16. External Data Memory Write Cycle

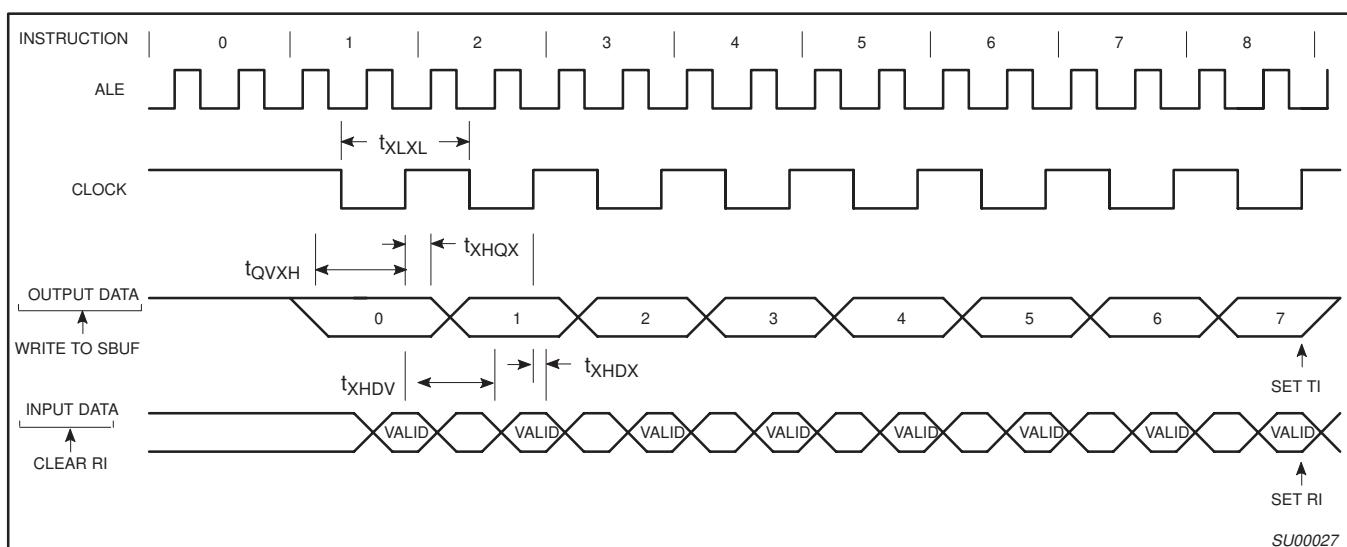


Figure 17. Shift Register Mode Timing

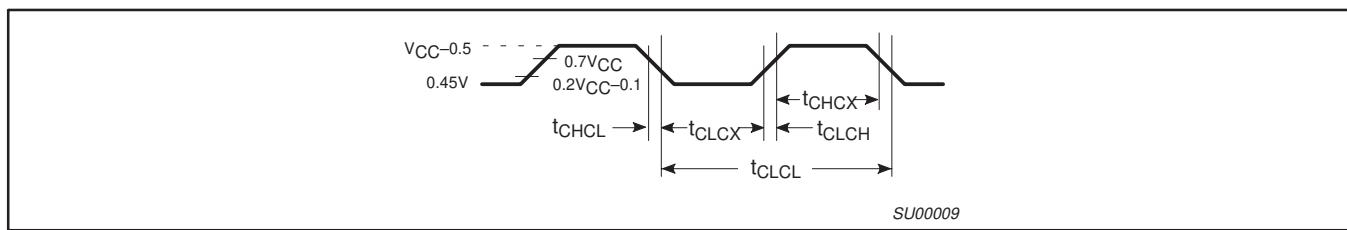


Figure 18. External Clock Drive

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

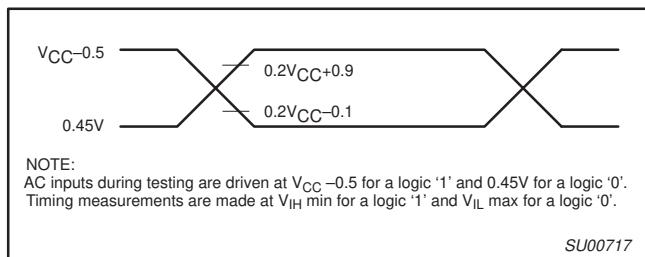
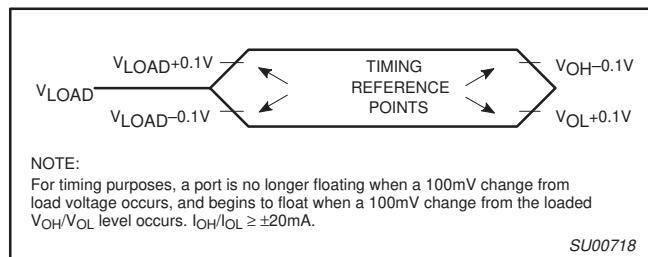
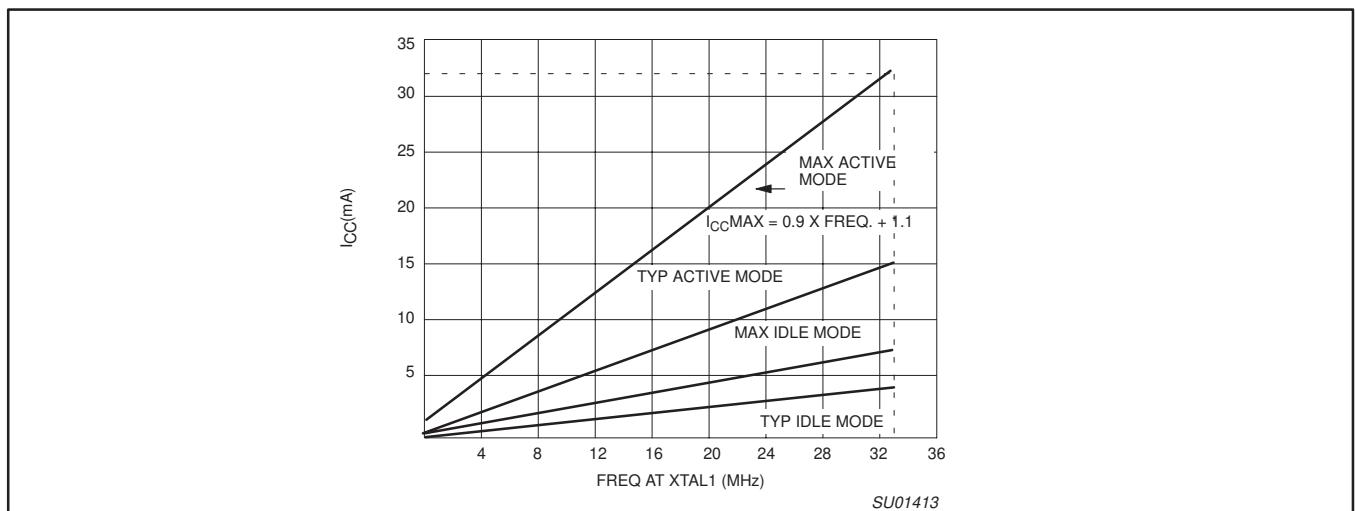
80C51/87C51/80C52/87C52**Figure 19. AC Testing Input/Output****Figure 20. Float Waveform**

Figure 21. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

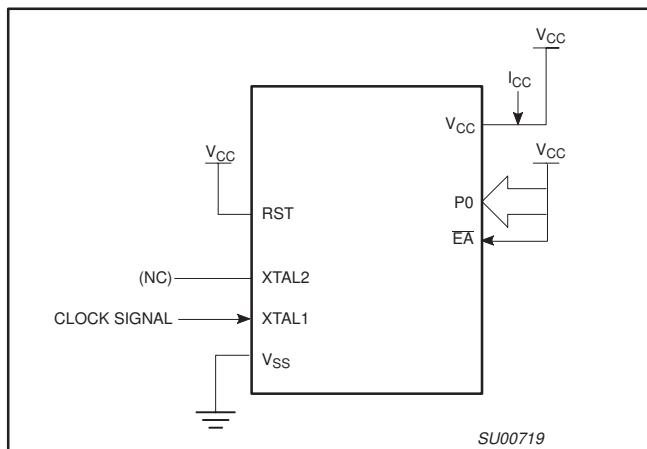


Figure 22. I_{CC} Test Condition, Active Mode
All other pins are disconnected

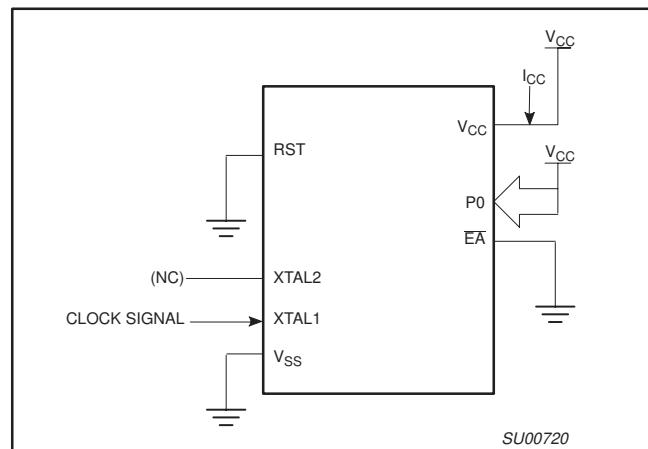


Figure 23. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

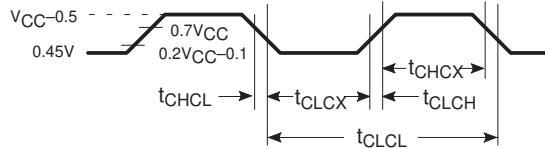


Figure 24. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$

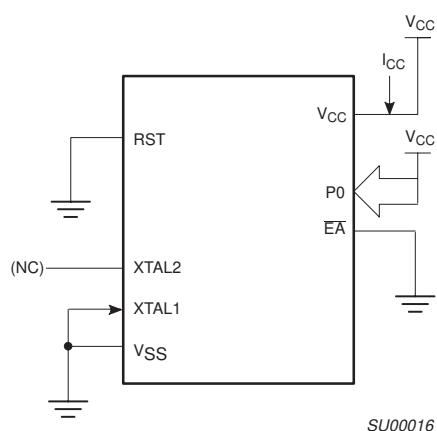


Figure 25. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. $V_{CC} = 2\text{ V to }5.5\text{ V}$

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52**EPROM CHARACTERISTICS**

These devices can be programmed by using a modified Improved Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The family contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as being manufactured by Philips.

Table 8 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 26 and 27. Figure 28 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 26. Note that the device is running with a 4 to 6 MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 26. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 8 are held at the 'Program Code Data' levels indicated in Table 8. The ALE/PROG is pulsed low 5 times as shown in Figure 27.

To program the encryption table, repeat the 5 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 5 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bits can still be programmed.

Note that the EA/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the

device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 28. The other pins are held at the 'Verify Code Data' levels indicated in Table 8. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 64 byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:
(030H) = 15H indicates manufactured by Philips
(031H) = 92H indicates 87C51

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 8, and which satisfies the timing specifications, is suitable.

Security Bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 9) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory, EA is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

Table 8. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V _{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V _{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V _{PP}	1	0	1	0
Pgm security bit 1	1	0	0*	V _{PP}	1	1	1	1
Pgm security bit 2	1	0	0*	V _{PP}	1	1	0	0
Pgm security bit 3	1	0	0*	V _{PP}	0	1	0	1

NOTES:

1. '0' = Valid low for that pin, '1' = valid high for that pin.
 2. V_{PP} = 12.75 V ±0.25 V.
 3. V_{CC} = 5 V ±10% during programming and verification.
- * ALE/PROG receives 5 programming pulses for code data (also for user array; 5 pulses for encryption or security bits) while V_{PP} is held at 12.75 V. Each programming pulse is low for 100 µs (±10 µs) and high for a minimum of 10 µs.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

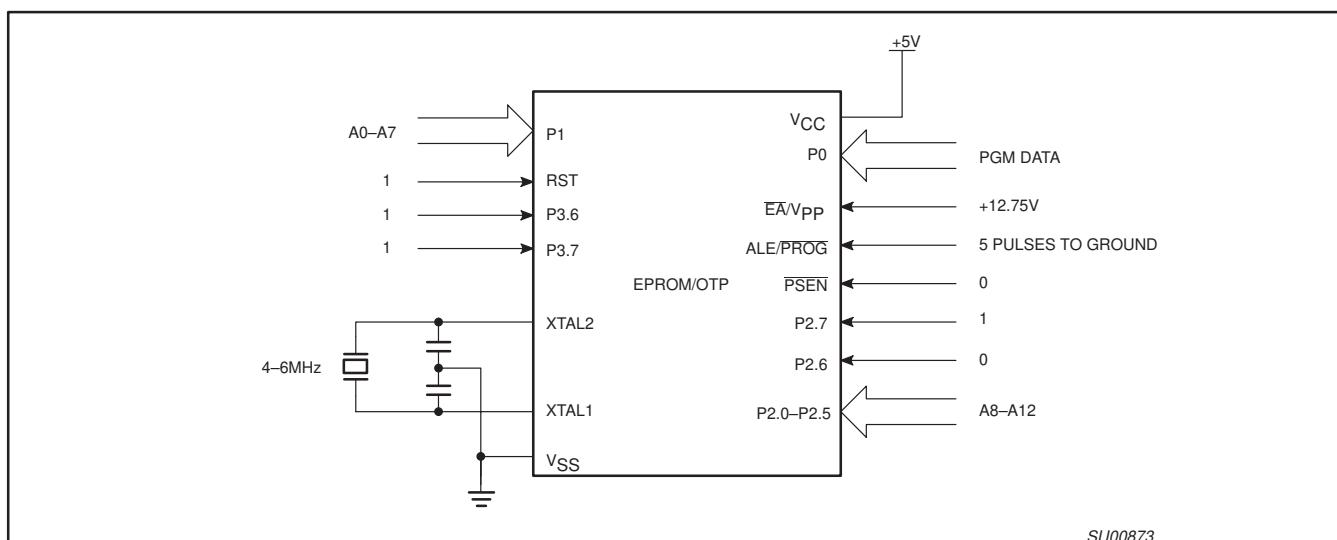
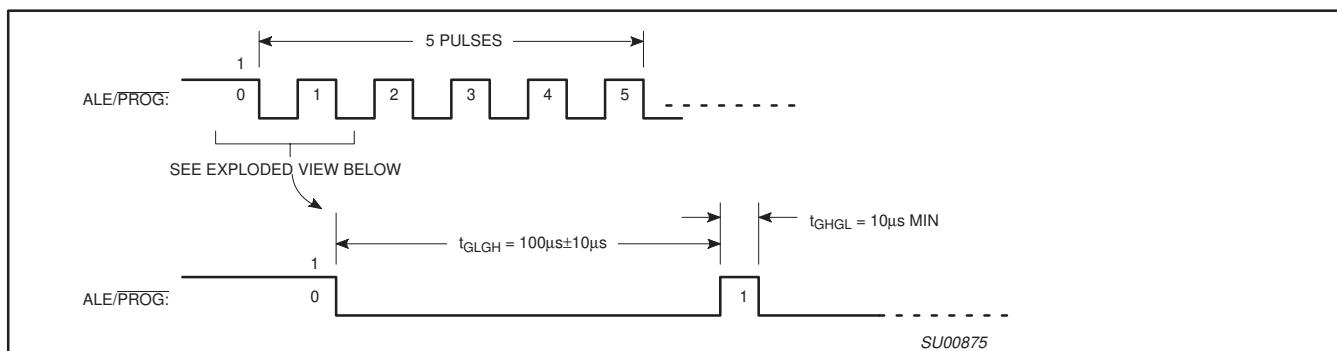
80C51/87C51/80C52/87C52

Table 9. Program Security Bits for EPROM Devices

PROGRAM LOCK BITS ^{1, 2}				PROTECTION DESCRIPTION
	SB1	SB2	SB3	
1	U	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, external execution is disabled. Internal data RAM is not accessible.

NOTES:

1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

**Figure 26. Programming Configuration****Figure 27. PROG Waveform**

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

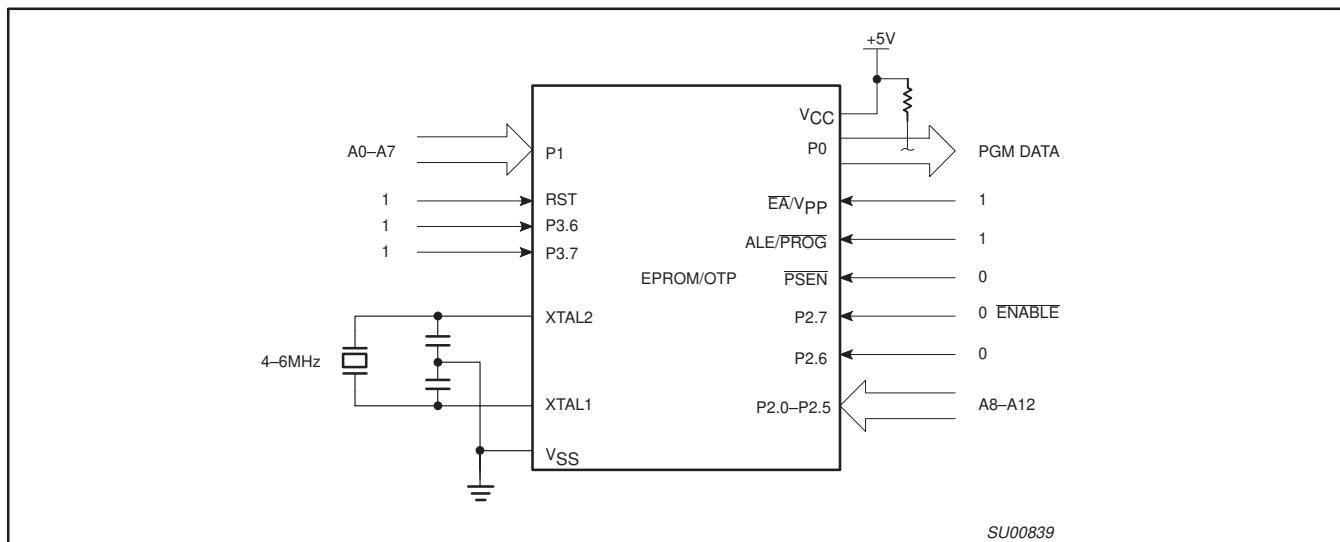


Figure 28. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5 V±10%, V_{SS} = 0 V (See Figure 29)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50 ¹	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to PROG low	48 t_{CLCL}		
t_{GHAX}	Address hold after PROG	48 t_{CLCL}		
t_{DVGL}	Data setup to PROG low	48 t_{CLCL}		
t_{GHDX}	Data hold after PROG	48 t_{CLCL}		
t_{EHSH}	P2.7 (ENABLE) high to V_{PP}	48 t_{CLCL}		
t_{SHGL}	V_{PP} setup to PROG low	10		μs
t_{GHSL}	V_{PP} hold after PROG	10		μs
t_{GLGH}	PROG width	90	110	μs
t_{AVQV}	Address to data valid		48 t_{CLCL}	
t_{ELQZ}	ENABLE low to data valid		48 t_{CLCL}	
t_{EHQZ}	Data float after ENABLE	0	48 t_{CLCL}	
t_{GHGL}	PROG high to PROG low	10		μs

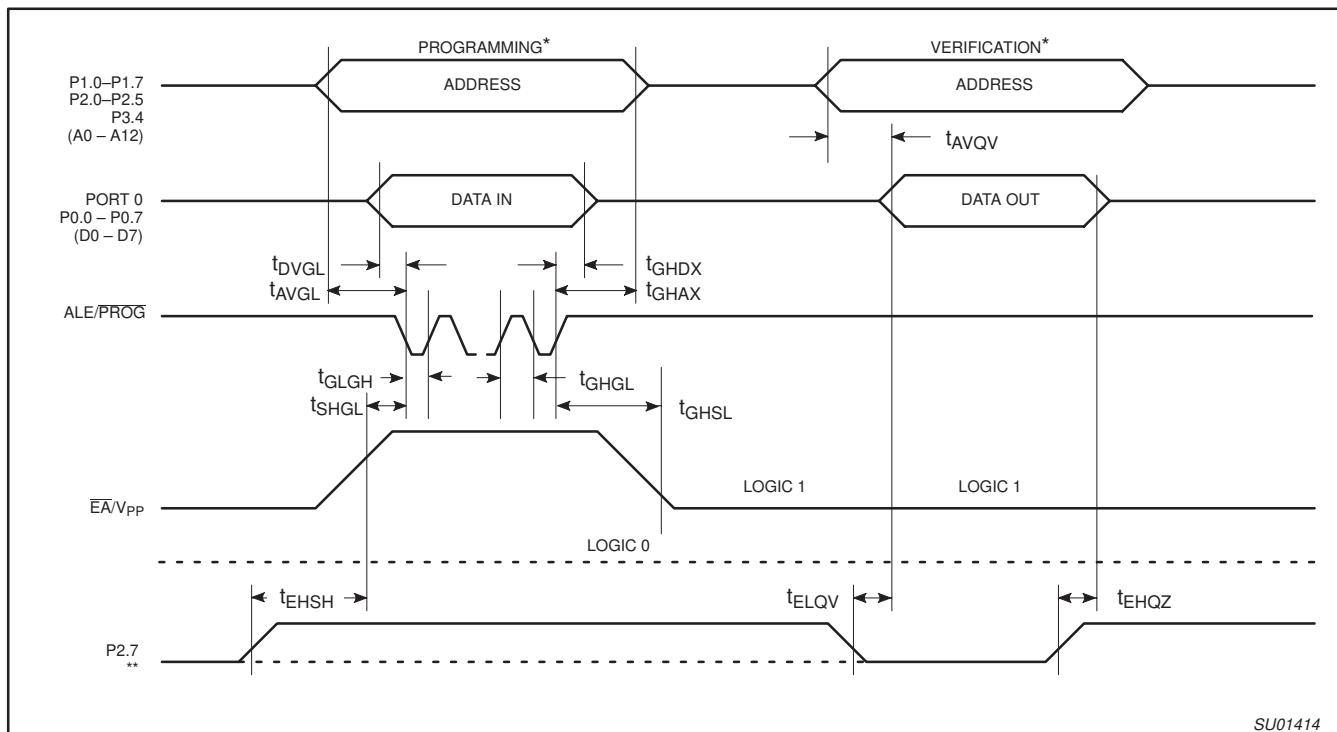
NOTE:

- Not tested.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52



SU01414

NOTES:

- * FOR PROGRAMMING CONFIGURATION SEE FIGURE 26.
- FOR VERIFICATION CONDITIONS SEE FIGURE 28.

- ** SEE TABLE 8.

Figure 29. EPROM Programming and Verification

MASK ROM DEVICES**Security Bits**

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 (see Table 10) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes

from the internal memory, EA is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled.

Encryption Array

64 bytes of encryption array are initially unprogrammed (all 1s).

Table 10. Program Security Bits

PROGRAM LOCK BITS ^{1,2}			PROTECTION DESCRIPTION
	SB1	SB2	
1	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
2	P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on Reset, and further programming of the EPROM is disabled.

NOTES:

- 1. P – programmed. U – unprogrammed.
- 2. Any other combination of the security bits is not defined.

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

80C51 ROM CODE SUBMISSION

When submitting ROM code for the 80C51, the following must be specified:

1. 4k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 0FFFH	DATA	7:0	User ROM Data
1000H to 103FH	KEY	7:0	ROM Encryption Key
1040H	SEC	0	ROM Security Bit 1
1040H	SEC	1	ROM Security Bit 2

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. EA is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

- Security Bit #1: Enabled Disabled
- Security Bit #2: Enabled Disabled
- Encryption: No Yes If Yes, must send key file.

80C52 ROM CODE SUBMISSION

When submitting ROM code for the 80C52, the following must be specified:

1. 8k byte user ROM data
2. 64 byte ROM encryption key
3. ROM security bits.

ADDRESS	CONTENT	BIT(S)	COMMENT
0000H to 1FFFH	DATA	7:0	User ROM Data
2000H to 203FH	KEY	7:0	ROM Encryption Key
2040H	SEC	0	ROM Security Bit 1
2040H	SEC	1	ROM Security Bit 2

Security Bit 1: When programmed, this bit has two effects on masked ROM parts:

1. External MOVC is disabled, and
2. EA is latched on Reset.

Security Bit 2: When programmed, this bit inhibits Verify User ROM.

NOTE: Security Bit 2 cannot be enabled unless Security Bit 1 is enabled.

If the ROM Code file does not include the options, the following information must be included with the ROM code.

For each of the following, check the appropriate box, and send to Philips along with the code:

- Security Bit #1: Enabled Disabled
- Security Bit #2: Enabled Disabled
- Encryption: No Yes If Yes, must send key file.

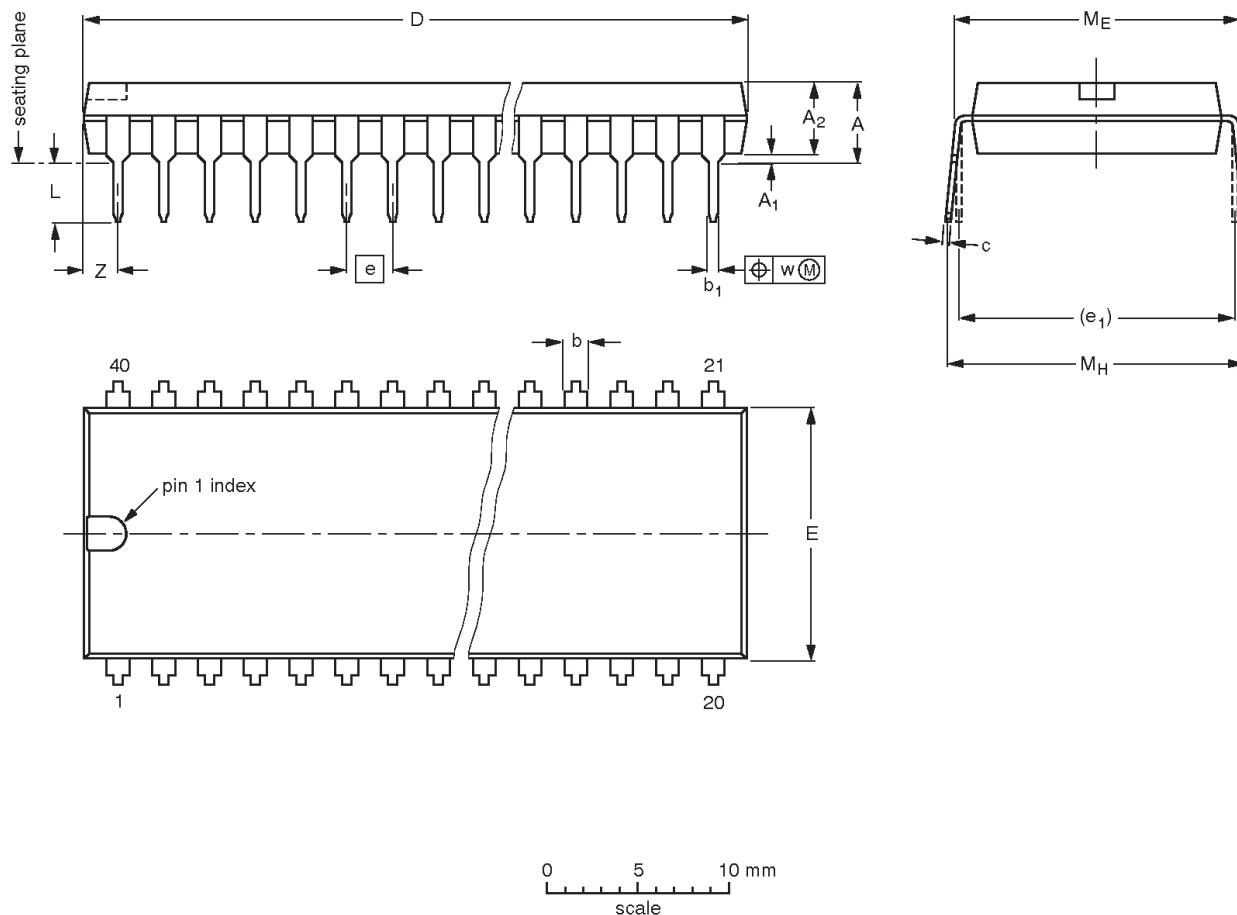
80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015	SC-511-40			-95-01-14 99-12-27

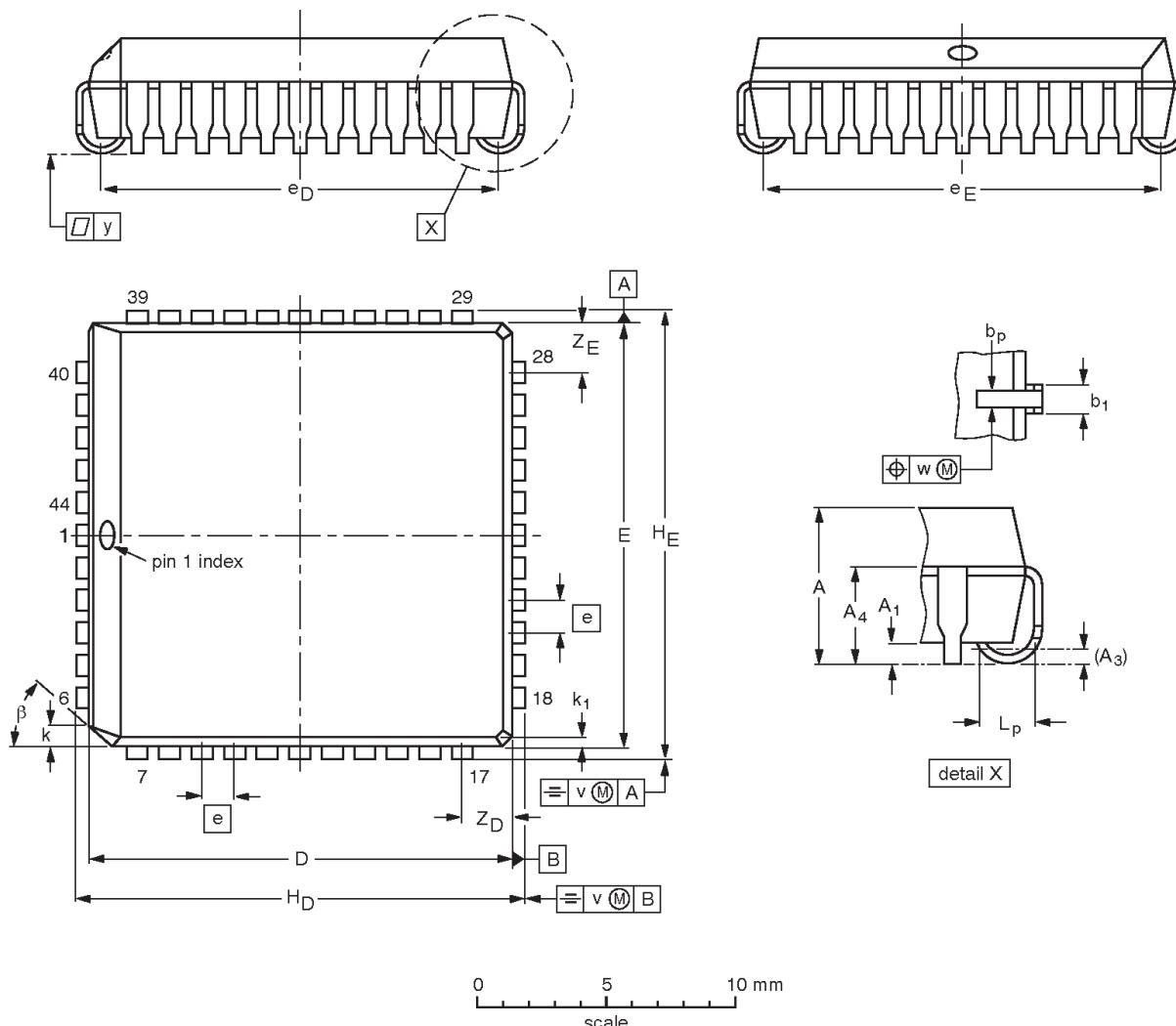
80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047				97-12-16 99-12-27

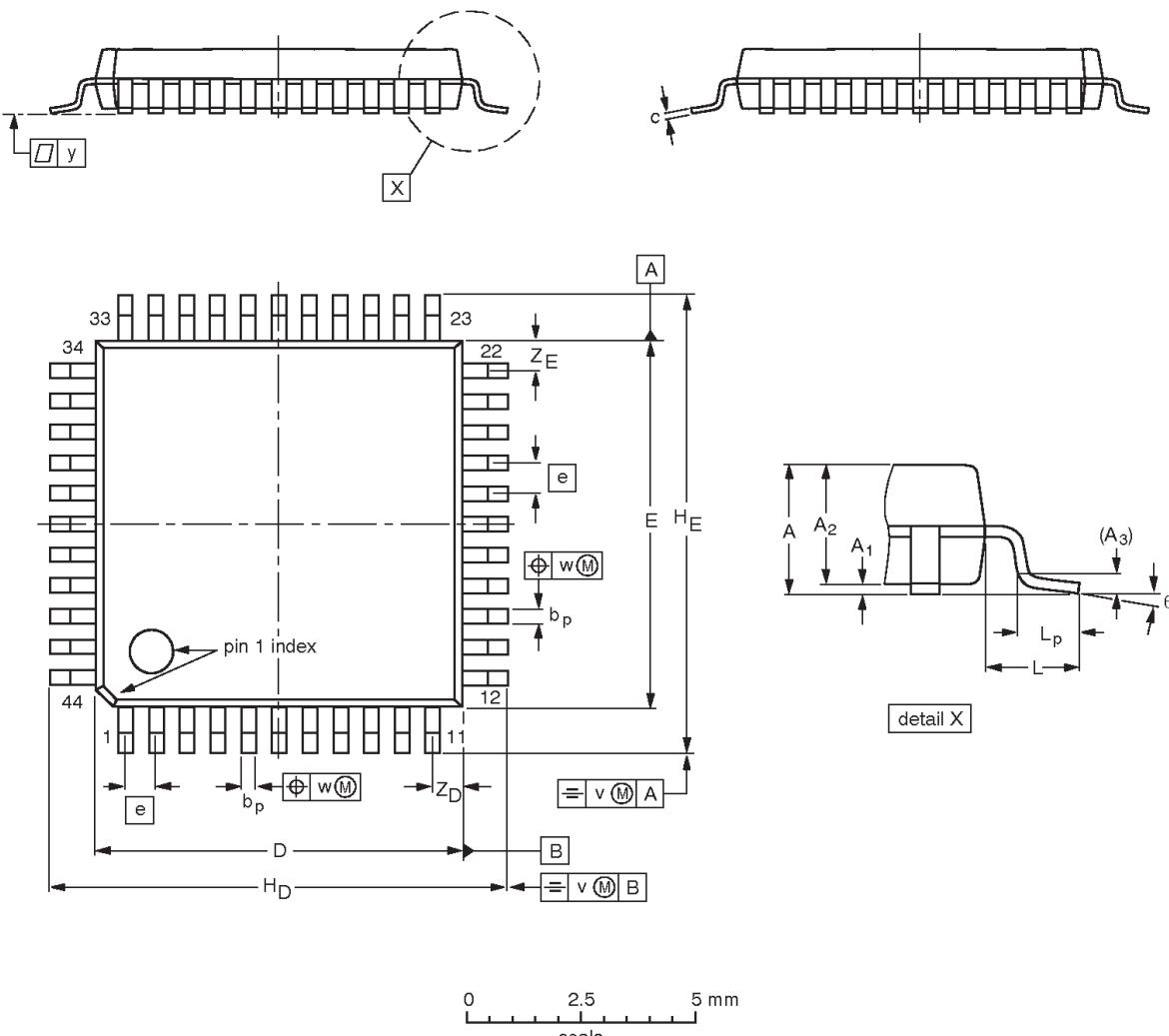
80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	2.10 0.05	0.25 1.65	1.85 0.25	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

- Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						-95-02-04 97-08-01

80C51 8-bit microcontroller family

4 K/8 K OTP/ROM low voltage (2.7 V–5.5 V),
low power, high speed (33 MHz), 128/256 B RAM

80C51/87C51/80C52/87C52**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 08-00

Document order number:

9397 750 07404

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PHILIPS

1. Introduction

Motor 1 Specification – 12V DC Motor

Features

- ◆ 12V – 200RPM –
- ◆ 3.6KG•CM torque DC gearhead motor
- ◆ 30:1 Gear Ratio
- ◆ 2mm rear encoder shaft
- ◆ Good compromise between speed and torque for small robotic designs.

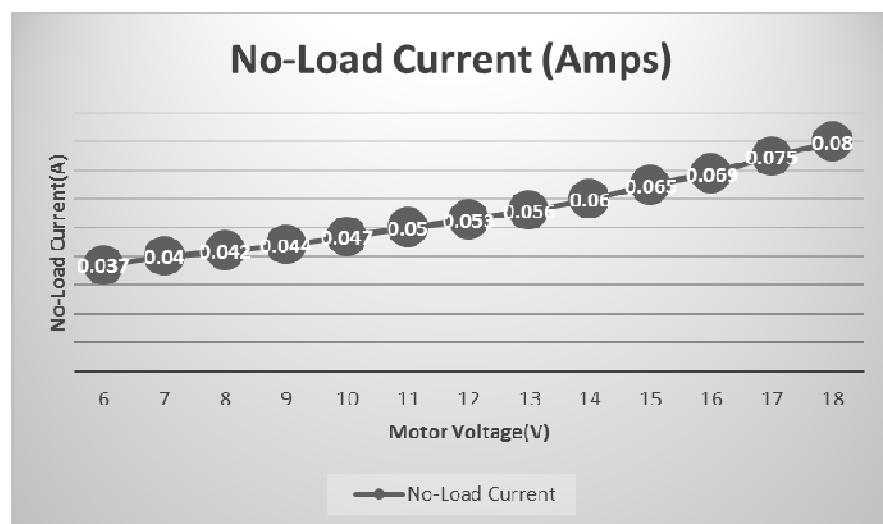
1.1 Description

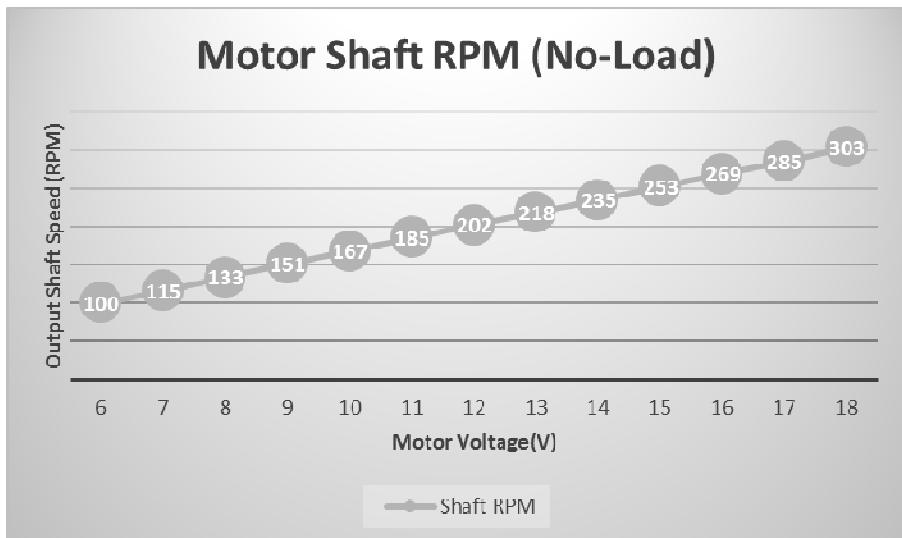
Motor1 is a 12V DC geared motor with a .25" motor output shaft and a 2mm rear encoder shaft. The 2mm shaft works with our ENC300 quadrature encoder to allow the motor to be used in position control applications. Motor controllers that are rated for 12V@2A are ideal for controlling this motor. However, motor controllers with lower current ratings can also be used if they have over-current and over-temperature protection.

2. Motor1 Specifications

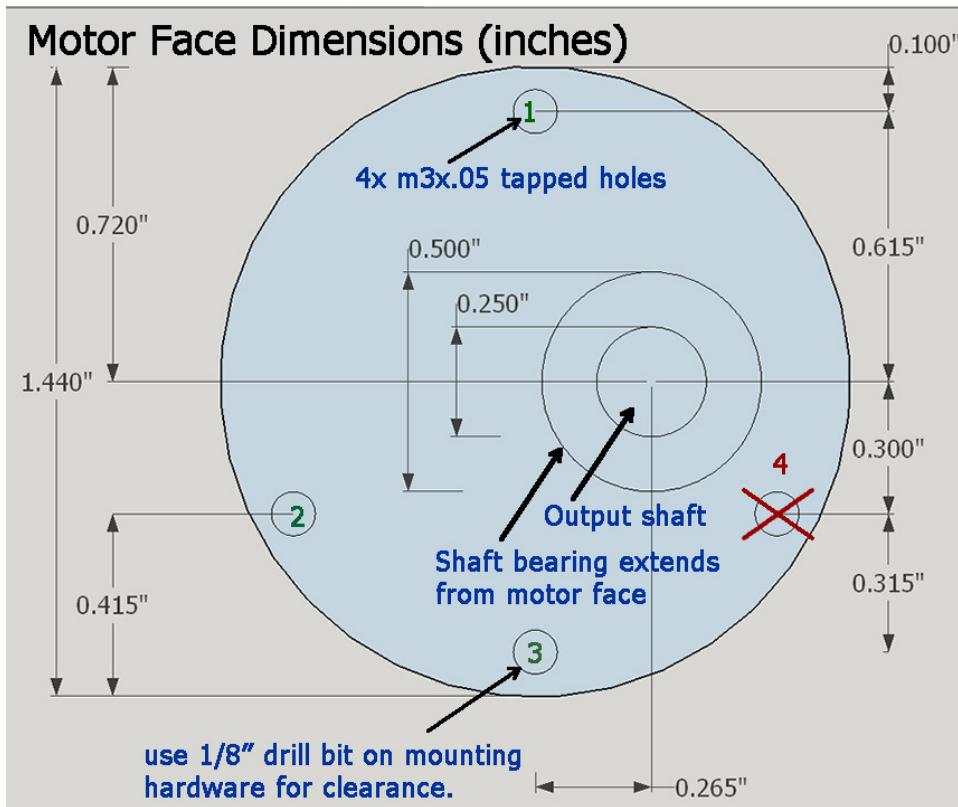
2.1 DC Gearhead Motor Characteristics

Characteristic	Value	Unit
Operating voltage	4.5-18	V
Startup torque (kilogram-force centimeter)	3.6	KG•CM
Startup torque (inch-pound)	3.1	Inch•lbf
Gear ratio	30:1	
No-Load Current (12V)	0.053	A
Stall Current	1.5	A
No-Load Speed (12V)	200	RPM

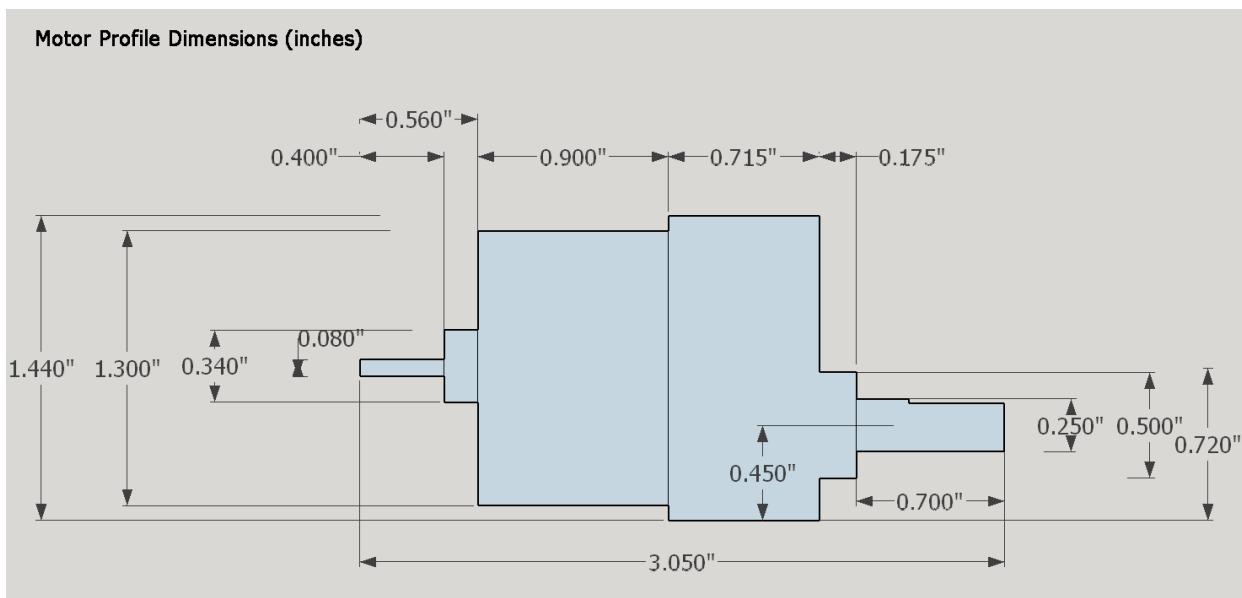




3. Mechanics



Notes on mounting hardware: The motor has 4 mounting holes on its face (labeled 1-4 in the image above). They are threaded for m3 x .05 metric machine screws. We have used 8mm long screws successfully to mount the motor to a 1/8" thick L-bracket. However, mounting hole 4 is in close proximity to the internal motor mechanics, and it is recommended that you avoid using it.



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[ABI-009-RC](#)

EN

This Datasheet is presented by
the manufacturer

DE

Dieses Datenblatt wird vom
Hersteller bereitgestellt

FR

Cette fiche technique est
présentée par le fabricant



Features

- Black in colour
- With internal drive circuit
- Sealed structure
- Wave solderable and washable
- Housing material: Noryl

**RoHS
Compliant**

Applications

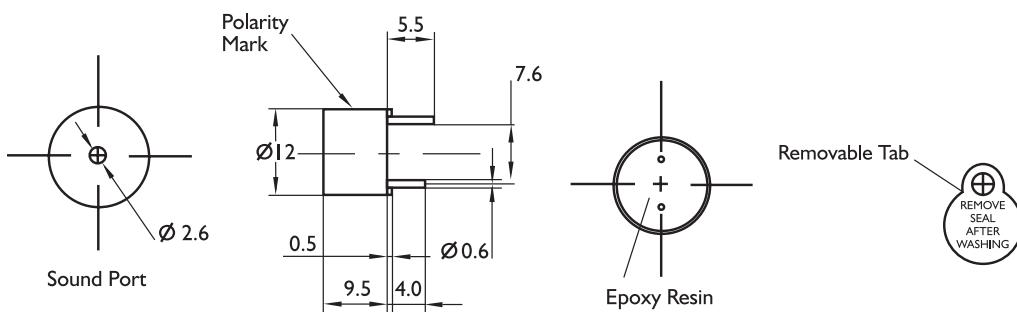
- Computer and peripherals
- Communications equipment
- Portable equipment
- Automobile electronics
- POS system
- Electronic cash register

Specifications:

Rated Voltage	: 6V DC
Operating Voltage	: 4 to 8V DC
Rated Current*	: ≤30mA
Sound Output at 10cm*	: ≥85dB
Resonant Frequency	: 2300 ±300Hz
Tone	: Continuous
Operating Temperature	: -25°C to +80°C
Storage Temperature	: -30°C to +85°C
Weight	: 2g

*Value applying at rated voltage (DC)

Diagram



Dimensions : Millimetres

Tolerance : ±0.5mm

Part Number Table

Description	Part Number
Buzzer, Electromech, 6V DC	ABI-009-RC

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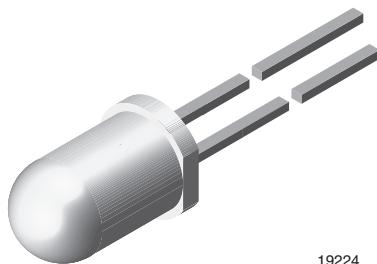
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Cette fiche technique est
présentée par le fabricant

Universal LED in Ø 5 mm Tinted Diffused Package



PRODUCT GROUP AND PACKAGE DATA

- Product group: LED
- Package: 5 mm
- Product series: standard
- Angle of half intensity: $\pm 30^\circ$

FEATURES

- For DC and pulse operation
- Luminous intensity categorized
- Standard T-1¾ package
- TLUR640. without stand-offs
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN FREE
GREEN
(5-2008)

APPLICATIONS

- General indicating and lighting purposes

PARTS TABLE

PART	COLOR	LUMINOUS INTENSITY (mcd)			at I_F (mA)	WAVELENGTH (nm)			at I_F (mA)	FORWARD VOLTAGE (V)			at I_F (mA)	TECHNOLOGY
		MIN.	TYP.	MAX.		MIN.	TYP.	MAX.		MIN.	TYP.	MAX.		
TLUR6400	Red	4	15	-	10	-	630	-	10	-	2	3	20	GaAsP on GaAs
TLUR6401	Red	4	15	32	10	-	630	-	10	-	2	3	20	GaAsP on GaAs

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^\circ C$, unless otherwise specified) TLUR6401

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	6	V
DC forward current		I^F	20	mA
Surge forward current	$t_p \leq 10 \mu s$	I_{FSM}	1	A
Power dissipation	$T_{amb} \leq 65^\circ C$	P_V	60	mW
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	- 40 to + 100	°C
Storage temperature range		T_{stg}	- 55 to + 100	°C
Soldering temperature	$t \leq 5 s$, 2 mm from body	T_{sd}	260	°C
Thermal resistance junction/ambient		R_{thJA}	500	K/W

OPTICAL AND ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^\circ C$, unless otherwise specified) TLUR640., RED

PARAMETER	TEST CONDITION	PART	MIN.	TYP.	MAX.	UNIT	MIN.
Luminous intensity ⁽¹⁾	$I_F = 10 \text{ mA}$	TLUR6400	I_V	4	15	-	mcd
		TLUR6401	I_V	4	15	32	mcd
Dominant wavelength	$I_F = 10 \text{ mA}$		λ_d	-	630	-	nm
Peak wavelength	$I_F = 10 \text{ mA}$		λ_p	-	640	-	nm
Angle of half intensity	$I_F = 10 \text{ mA}$		φ	-	± 30	-	deg
Forward voltage	$I_F = 20 \text{ mA}$		V_F	-	2	3	V
Reverse voltage	$I_R = 10 \mu A$		V_R	6	15	-	V
Junction capacitance	$V_R = 0 \text{ V}$, $f = 1 \text{ MHz}$		C_j	-	50	-	pF

Note

⁽¹⁾ In one packing unit $I_{Vmin}/I_{Vmax} \leq 0.5$

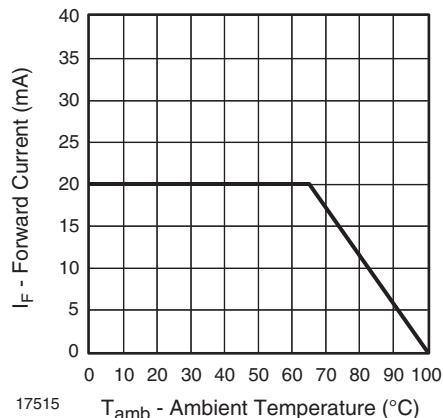
TYPICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified)


Fig. 1 - Forward Current vs. Ambient Temperature

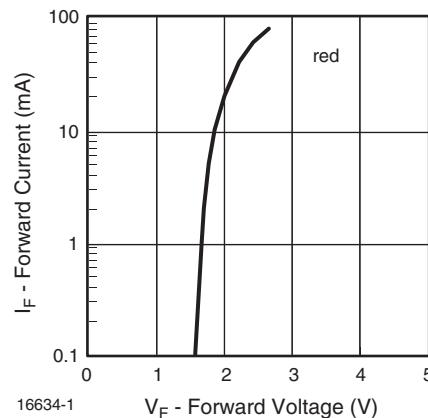


Fig. 4 - Forward Current vs. Forward Voltage

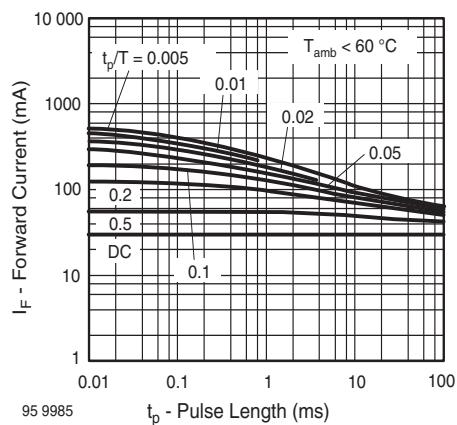


Fig. 2 - Pulse Forward Current vs. Pulse Duration

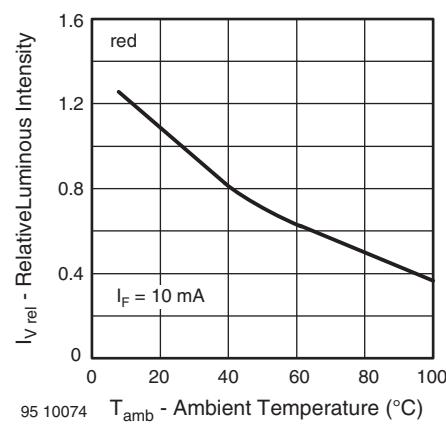


Fig. 5 - Relative Luminous Intensity vs. Ambient Temperature

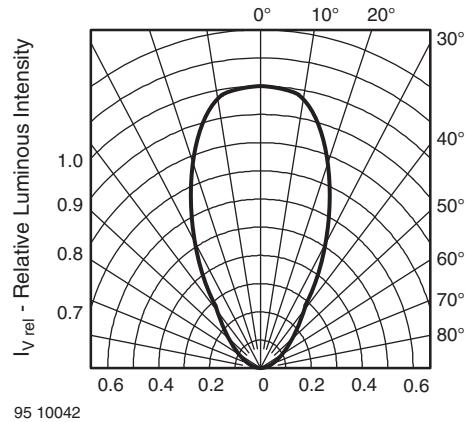


Fig. 3 - Relative Luminous Intensity vs. Angular Displacement

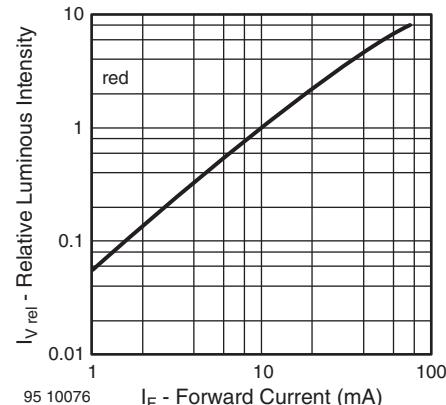


Fig. 6 - Relative Luminous Intensity vs. Forward Current

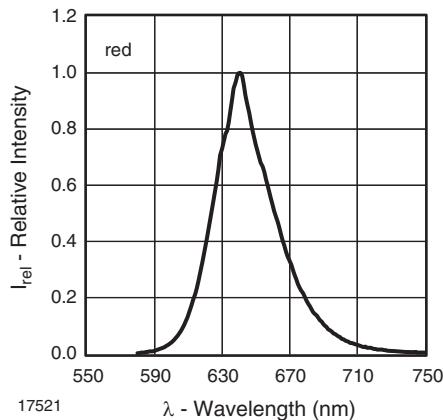
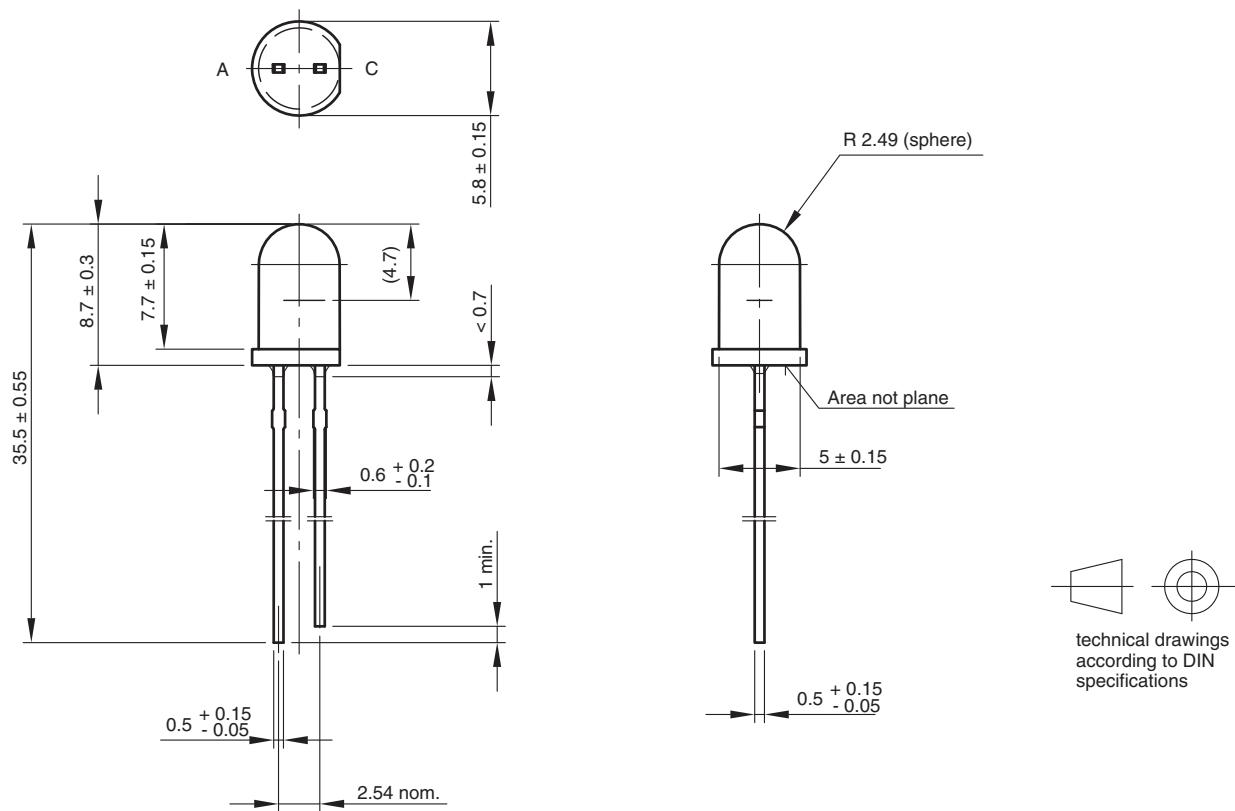


Fig. 7 - Relative Intensity vs. Wavelength

PACKAGE DIMENSIONS in millimeters



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LM340, LM340A and LM7805 Family Wide V_{IN} 1.5-A Fixed Voltage Regulators

1 Features

- Output Current up to 1.5 A
- Available in Fixed 5-V, 12-V, and 15-V Options
- Output Voltage Tolerances of $\pm 2\%$ at $T_J = 25^\circ\text{C}$ (LM340A)
- Line Regulation of 0.01% / V of at 1-A Load (LM340A)
- Load Regulation of 0.3% / A (LM340A)
- Internal Thermal Overload, Short-Circuit and SOA Protection
- Available in Space-Saving SOT-223 Package
- Output Capacitance Not Required for Stability

2 Applications

- Industrial Power Supplies
- SMPS Post Regulation
- HVAC Systems
- AC Invertors
- Test and Measurement Equipment
- Brushed and Brushless DC Motor Drivers
- Solar Energy String Invertors

Available Packages

Pin 1. Input

2. Ground

3. Output

Tab/Case is Ground or Output



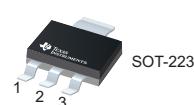
TO-3



TO-220



TO-263



SOT-223

3 Description

The LM340 and LM7805 Family monolithic 3-terminal positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.5-A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Considerable effort was expended to make the entire series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

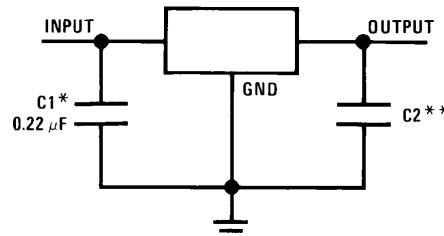
LM7805 is also available in a higher accuracy and better performance version (LM340A). Refer to LM340A specifications in the [LM340A Electrical Characteristics](#) table.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM340x LM7805 Family	DDPAK/TO-263 (3)	10.18 mm x 8.41 mm
	SOT-223 (4)	6.50 mm x 3.50 mm
	TO-220 (3)	14.986 mm x 10.16 mm
	TO-3 (2)	38.94 mm x 25.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Fixed Output Voltage Regulator



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*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1- μF , ceramic disc).



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		11.7 Glossary	20
		12 Mechanical, Packaging, and Orderable Information	21

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

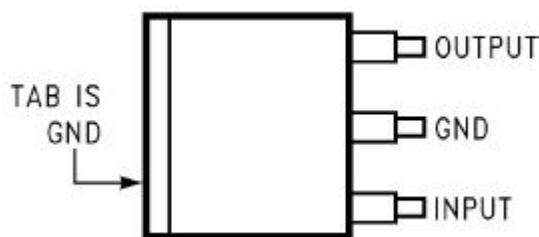
Changes from Revision K (November 2015) to Revision L	Page
• Changed pinout number order for the TO-220 and SOT-223 packages from: 2, 3, 1 to: 1, 2, 3	1

Changes from Revision J (December 2013) to Revision K	Page
• Added <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted obsolete LM140 and LM7808C devices from the data sheet	1
• Changed Figure 13 caption from <i>Line Regulation 140AK-5.0</i> to <i>Line Regulation LM340</i> ,	11
• Changed Figure 14 caption from <i>Line Regulation 140AK-5.0</i> to <i>Line Regulation LM340</i> ,	11

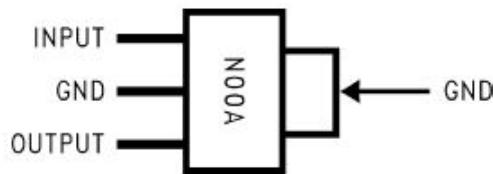
Changes from Revision I (March 2013) to Revision J	Page
• Changed 0.5 from typ to max	5

5 Pin Configuration and Functions

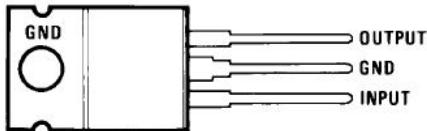
LM7805 and LM7812 KTT Package
3-Pin DDPAK/TO-263
Top View



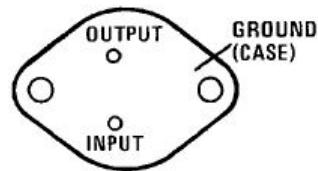
LM7805 DCY Package
4-Pin SOT-223
Side View



LM7805, LM7812, and LM7815 NDE Package
3-Pin TO-220
Top View



LM340K-5.0 NDS Package
2-Pin TO-3
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INPUT	1	I	Input voltage pin
GND	2	I/O	Ground pin
OUTPUT	3	O	Output voltage pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
DC input voltage		35		V
Internal power dissipation ⁽³⁾		Internally Limited		
Maximum junction temperature		150		°C
Lead temperature (soldering, 10 sec.)	TO-3 package (NDS)	300		°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s	230		°C
Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) The maximum allowable power dissipation at any ambient temperature is a function of the maximum junction temperature for operation ($T_{JMAX} = 125^{\circ}\text{C}$ or 150°C), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A). $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature rises above T_{JMAX} and the electrical specifications do not apply. If the die temperature rises above 150°C , the device goes into thermal shutdown. For the TO-3 package (NDS), the junction-to-ambient thermal resistance (θ_{JA}) is $39^{\circ}\text{C}/\text{W}$. When using a heat sink, θ_{JA} is the sum of the $4^{\circ}\text{C}/\text{W}$ junction-to-case thermal resistance (θ_{JC}) of the TO-3 package and the case-to-ambient thermal resistance of the heat sink. For the TO-220 package (NDE), θ_{JA} is $54^{\circ}\text{C}/\text{W}$ and θ_{JC} is $4^{\circ}\text{C}/\text{W}$. If SOT-223 is used, the junction-to-ambient thermal resistance is $174^{\circ}\text{C}/\text{W}$ and can be reduced by a heat sink (see Applications Hints on heat sinking). If the DDPAKTO-263 package is used, the thermal resistance can be reduced by increasing the PCB copper area thermally connected to the package: Using 0.5 square inches of copper area, θ_{JA} is $50^{\circ}\text{C}/\text{W}$; with 1 square inch of copper area, θ_{JA} is $37^{\circ}\text{C}/\text{W}$; and with 1.6 or more inches of copper area, θ_{JA} is $32^{\circ}\text{C}/\text{W}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) ⁽¹⁾	±2000	V

- (1) ESD rating is based on the human-body model, 100 pF discharged through 1.5 kΩ.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Temperature (T_A)	LM340A, LM340	0	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM340, LM7805 Family				UNIT
		NDE (TO-220)	KTT (DDPAK/TO-263)	DCY (SOT-223)	NDS (TO-3)	
			3 PINS	3 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.9	44.8	62.1	39	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	16.7	45.6	44	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.3	24.4	10.7	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.2	11.2	2.7	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.3	23.4	10.6	—	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	1.7	1.5	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 LM340A Electrical Characteristics, $V_O = 5 \text{ V}$, $V_I = 10 \text{ V}$

$I_{\text{OUT}} = 1 \text{ A}$, $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ (LM340A) unless otherwise specified⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	$T_J = 25^\circ\text{C}$		4.9	5	5.1	V
		$P_D \leq 15 \text{ W}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$ $7.5 \text{ V} \leq V_{\text{IN}} \leq 20 \text{ V}$		4.8		5.2	V
ΔV_O	Line regulation	7.5 V $\leq V_{\text{IN}} \leq 20$ V	$T_J = 25^\circ\text{C}$		3	10	mV
			Over temperature, $I_O = 500 \text{ mA}$			10	mV
		8 V $\leq V_{\text{IN}} \leq 12$ V	$T_J = 25^\circ\text{C}$			4	mV
			Over temperature			12	mV
ΔV_O	Load regulation	$T_J = 25^\circ\text{C}$	5 mA $\leq I_O \leq 1.5$ A		10	25	mV
			250 mA $\leq I_O \leq 750$ mA			15	mV
		Over temperature, 5 mA $\leq I_O \leq 1$ A				25	mV
I_Q	Quiescent current	$T_J = 25^\circ\text{C}$			6	mA	
		Over temperature			6.5	mA	
ΔI_Q	Quiescent current change	$T_J = 25^\circ\text{C}$, $I_O = 1 \text{ A}$ $7.5 \text{ V} \leq V_{\text{IN}} \leq 20 \text{ V}$				0.8	mA
		Over temperature, 5 mA $\leq I_O \leq 1$ A				0.5	mA
		Over temperature, $I_O = 500 \text{ mA}$ $8 \text{ V} \leq V_{\text{IN}} \leq 25 \text{ V}$				0.8	mA
V_N	Output noise voltage	$T_A = 25^\circ\text{C}$, 10 Hz $\leq f \leq 100$ kHz			40		μV
$\frac{\Delta V_{\text{IN}}}{\Delta V_{\text{OUT}}}$	Ripple rejection	f = 120 Hz	$T_J = 25^\circ\text{C}$, , $I_O = 1 \text{ A}$	68	80		dB
		8 V $\leq V_{\text{IN}} \leq 18$ V		68			dB
R_O	Dropout voltage	$T_J = 25^\circ\text{C}$, $I_O = 1 \text{ A}$			2		V
	Output resistance	f = 1 kHz			8		$\text{m}\Omega$
	Short-circuit current	$T_J = 25^\circ\text{C}$			2.1		A
	Peak output current	$T_J = 25^\circ\text{C}$			2.4		A
	Average TC of V_O	Min, $T_J = 0^\circ\text{C}$, $I_O = 5 \text{ mA}$			-0.6		$\text{mV}/^\circ\text{C}$
V_{IN}	Input voltage required to maintain line regulation	$T_J = 25^\circ\text{C}$		7.5			V

- (1) All characteristics are measured with a 0.22- μF capacitor from input to ground and a 0.1- μF capacitor from output to ground. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10 \text{ ms}$, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

6.6 LM340 / LM7805 Electrical Characteristics, $V_O = 5 \text{ V}$, $V_I = 10 \text{ V}$

$0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ unless otherwise specified⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	$T_J = 25^\circ\text{C}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$	4.8	5	5.2	V
		$P_D \leq 15 \text{ W}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$ $7.5 \text{ V} \leq V_{IN} \leq 20 \text{ V}$	4.75		5.25	V
ΔV_O	Line regulation	$I_O = 500 \text{ mA}$	$T_J = 25^\circ\text{C}$ $7\text{V} \leq V_{IN} \leq 25\text{V}$	3	50	mV
			Over temperature $8\text{V} \leq V_{IN} \leq 20\text{V}$		50	mV
		$I_O \leq 1 \text{ A}$	$T_J = 25^\circ\text{C}$ $7.5\text{V} \leq V_{IN} \leq 20\text{V}$		50	mV
			Over temperature $8\text{V} \leq V_{IN} \leq 12\text{V}$		25	mV
ΔV_O	Load regulation	$T_J = 25^\circ\text{C}$	$5 \text{ mA} \leq I_O \leq 1.5 \text{ A}$	10	50	mV
			$250 \text{ mA} \leq I_O \leq 750 \text{ mA}$		25	mV
			Over temperature, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$		50	mV
I_Q	Quiescent current	$I_O \leq 1 \text{ A}$	$T_J = 25^\circ\text{C}$	8		mA
			Over temperature		8.5	mA
ΔI_Q	Quiescent current change	$0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$		0.5		mA
			$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$		1	mA
		7 V $\leq V_{IN} \leq 20 \text{ V}$	Over temperature, $I_O \leq 500 \text{ mA}$		1	mA
V_N	Output noise voltage	$T_A = 25^\circ\text{C}$, $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$		40		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple rejection	$f = 120 \text{ Hz}$ $8 \text{ V} \leq V_{IN} \leq 18 \text{ V}$	$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$	62	80	dB
			Over temperature, $I_O \leq 500 \text{ mA}$	62		dB
R_O	Dropout voltage	$T_J = 25^\circ\text{C}$, $I_O = 1 \text{ A}$		2		V
	Output resistance	$f = 1 \text{ kHz}$		8		$\text{m}\Omega$
	Short-circuit current	$T_J = 25^\circ\text{C}$		2.1		A
	Peak output current	$T_J = 25^\circ\text{C}$		2.4		A
	Average TC of V_{OUT}	Over temperature, $I_O = 5 \text{ mA}$		-0.6		$\text{mV}/^\circ\text{C}$
V_{IN}	Input voltage required to maintain line regulation	$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$		7.5		V

- (1) All characteristics are measured with a $0.22\text{-}\mu\text{F}$ capacitor from input to ground and a $0.1\text{-}\mu\text{F}$ capacitor from output to ground. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10 \text{ ms}$, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

6.7 LM340 / LM7812 Electrical Characteristics, $V_O = 12 \text{ V}$, $V_I = 19 \text{ V}$

$0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ unless otherwise specified⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	$T_J = 25^\circ\text{C}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$	11.5	12	12.5	V
		$P_D \leq 15 \text{ W}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$ $14.5 \text{ V} \leq V_{IN} \leq 27 \text{ V}$	11.4		12.6	V
ΔV_O	Line regulation	$I_O = 500 \text{ mA}$	$T_J = 25^\circ\text{C}$ $14.5 \text{ V} \leq V_{IN} \leq 30 \text{ V}$	4	120	mV
			Over temperature $15 \text{ V} \leq V_{IN} \leq 27 \text{ V}$		120	mV
		$I_O \leq 1 \text{ A}$	$T_J = 25^\circ\text{C}$ $14.6 \text{ V} \leq V_{IN} \leq 27 \text{ V}$		120	mV
			Over temperature $16 \text{ V} \leq V_{IN} \leq 22 \text{ V}$		60	mV
ΔV_O	Load regulation	$T_J = 25^\circ\text{C}$	$5 \text{ mA} \leq I_O \leq 1.5 \text{ A}$	12	120	mV
			$250 \text{ mA} \leq I_O \leq 750 \text{ mA}$		60	mV
		Over temperature, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$			120	mV
I_Q	Quiescent current	$I_O \leq 1 \text{ A}$	$T_J = 25^\circ\text{C}$	8	mA	
			Over temperature		8.5	mA
ΔI_Q	Quiescent current change	$5 \text{ mA} \leq I_O \leq 1 \text{ A}$		0.5		mA
			$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$ $14.8 \text{ V} \leq V_{IN} \leq 27 \text{ V}$		1	mA
		Over temperature, $I_O \leq 500 \text{ mA}$ $14.5 \text{ V} \leq V_{IN} \leq 30 \text{ V}$			1	mA
V_N	Output noise voltage	$T_A = 25^\circ\text{C}$, $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$		75		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple rejection	$f = 120 \text{ Hz}$	$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$	55	72	dB
		$15 \text{ V} \leq V_{IN} \leq 25 \text{ V}$	Over temperature, $I_O \leq 500 \text{ mA}$	55		dB
R_O	Dropout voltage	$T_J = 25^\circ\text{C}$, $I_O = 1 \text{ A}$			2	V
	Output resistance	$f = 1 \text{ kHz}$			18	$\text{m}\Omega$
	Short-circuit current	$T_J = 25^\circ\text{C}$			1.5	A
	Peak output current	$T_J = 25^\circ\text{C}$			2.4	A
	Average TC of V_{OUT}	Over temperature, $I_O = 5 \text{ mA}$			-1.5	$\text{mV}/^\circ\text{C}$
V_{IN}	Input voltage required to maintain line regulation	$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$			14.6	V

- (1) All characteristics are measured with a $0.22\text{-}\mu\text{F}$ capacitor from input to ground and a $0.1\text{-}\mu\text{F}$ capacitor from output to ground. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10 \text{ ms}$, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

6.8 LM340 / LM7815 Electrical Characteristics, $V_O = 15 \text{ V}$, $V_I = 23 \text{ V}$

$0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ unless otherwise specified⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	$T_J = 25^\circ\text{C}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$	14.4	15	15.6	V
		$P_D \leq 15 \text{ W}$, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$ $17.5 \text{ V} \leq V_{IN} \leq 30 \text{ V}$	14.25		15.75	V
ΔV_O	Line regulation	$I_O = 500 \text{ mA}$	$T_J = 25^\circ\text{C}$ $17.5 \text{ V} \leq V_{IN} \leq 30 \text{ V}$	4	150	mV
			Over temperature $18.5 \text{ V} \leq V_{IN} \leq 30 \text{ V}$		150	mV
		$I_O \leq 1 \text{ A}$	$T_J = 25^\circ\text{C}$ $17.7 \text{ V} \leq V_{IN} \leq 30 \text{ V}$		150	mV
			Over temperature $20 \text{ V} \leq V_{IN} \leq 26 \text{ V}$		75	mV
ΔV_O	Load regulation	$T_J = 25^\circ\text{C}$	$5 \text{ mA} \leq I_O \leq 1.5 \text{ A}$	12	150	mV
			$250 \text{ mA} \leq I_O \leq 750 \text{ mA}$		75	mV
			Over temperature, $5 \text{ mA} \leq I_O \leq 1 \text{ A}$,		150	mV
I_Q	Quiescent current	$I_O \leq 1 \text{ A}$	$T_J = 25^\circ\text{C}$	8	mA	
			Over temperature		8.5	mA
ΔI_Q	Quiescent current change	$5 \text{ mA} \leq I_O \leq 1 \text{ A}$		0.5		mA
			$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$ $17.9 \text{ V} \leq V_{IN} \leq 30 \text{ V}$		1	mA
		Over temperature, $I_O \leq 500 \text{ mA}$ $17.5 \text{ V} \leq V_{IN} \leq 30 \text{ V}$			1	mA
V_N	Output noise voltage	$T_A = 25^\circ\text{C}$, $10 \text{ Hz} \leq f \leq 100 \text{ kHz}$		90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple rejection	$f = 120 \text{ Hz}$	$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$	54	70	dB
		$18.5 \text{ V} \leq V_{IN} \leq 28.5 \text{ V}$	Over temperature, $I_O \leq 500 \text{ mA}$	54		dB
R_O	Dropout voltage	$T_J = 25^\circ\text{C}$, $I_O = 1 \text{ A}$			2	V
	Output resistance	$f = 1 \text{ kHz}$			19	$\text{m}\Omega$
	Short-circuit current	$T_J = 25^\circ\text{C}$			1.2	A
	Peak output current	$T_J = 25^\circ\text{C}$			2.4	A
	Average TC of V_{OUT}	Over temperature, $I_O = 5 \text{ mA}$			-1.8	$\text{mV}/^\circ\text{C}$
V_{IN}	Input voltage required to maintain line regulation	$T_J = 25^\circ\text{C}$, $I_O \leq 1 \text{ A}$			17.7	V

- (1) All characteristics are measured with a $0.22\text{-}\mu\text{F}$ capacitor from input to ground and a $0.1\text{-}\mu\text{F}$ capacitor from output to ground. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10 \text{ ms}$, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

6.9 Typical Characteristics

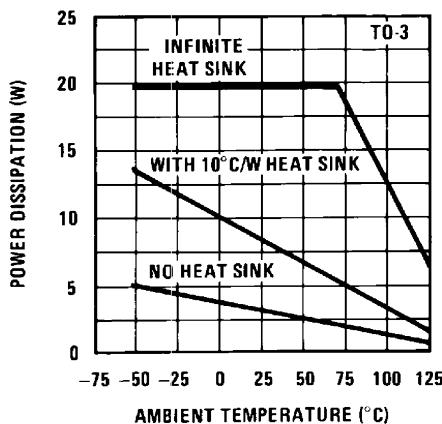


Figure 1. Maximum Average Power Dissipation

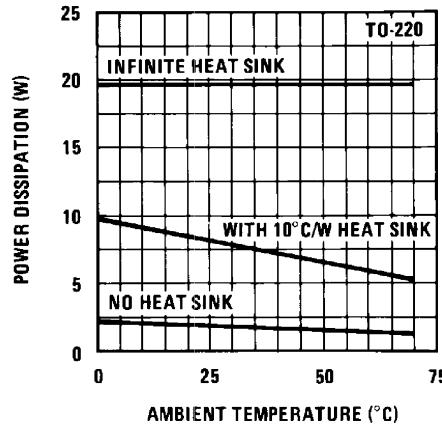


Figure 2. Maximum Average Power Dissipation

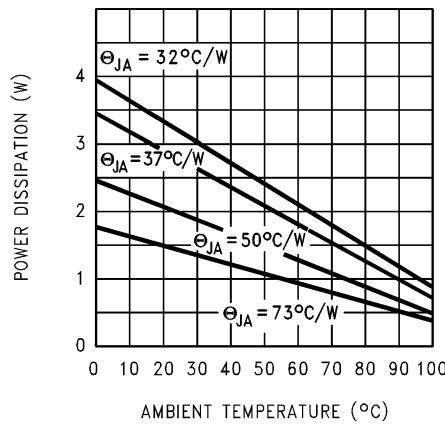
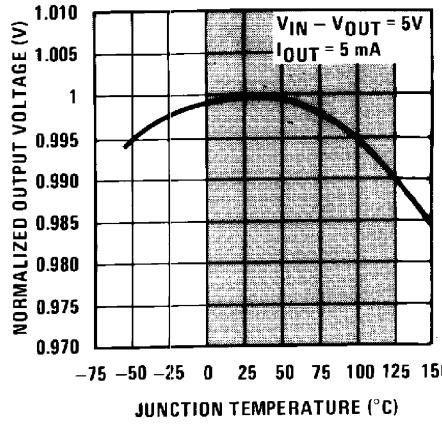


Figure 3. Maximum Power Dissipation (DDPAK/TO-263)



Shaded area refers to LM340A/LM340, LM7805, LM7812 and LM7815.

Figure 4. Output Voltage (Normalized to 1 V at $T_J = 25^\circ\text{C}$)

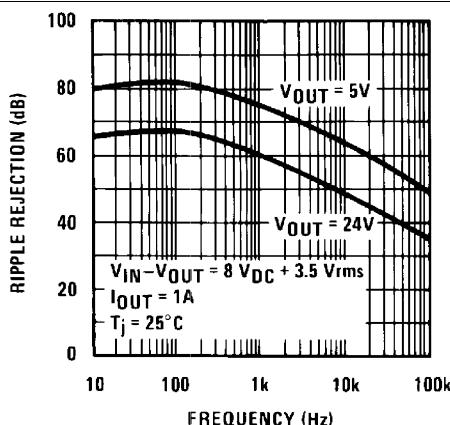


Figure 5. Ripple Rejection

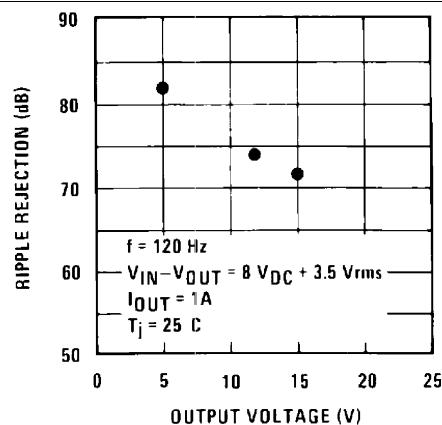


Figure 6. Ripple Rejection

Typical Characteristics (continued)

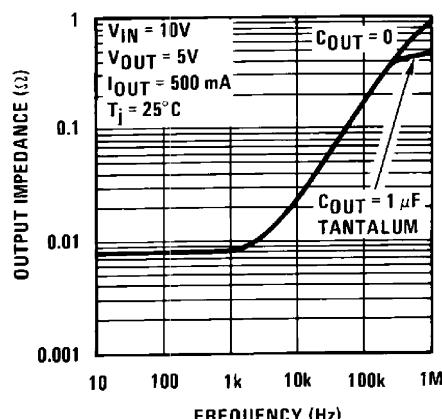


Figure 7. Output Impedance

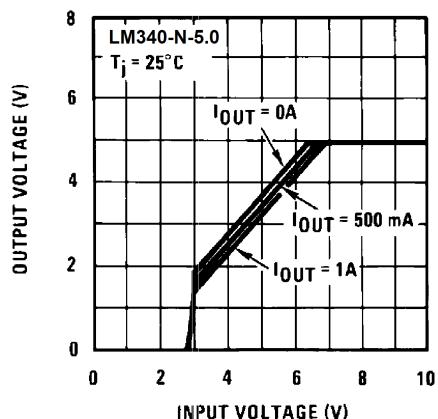
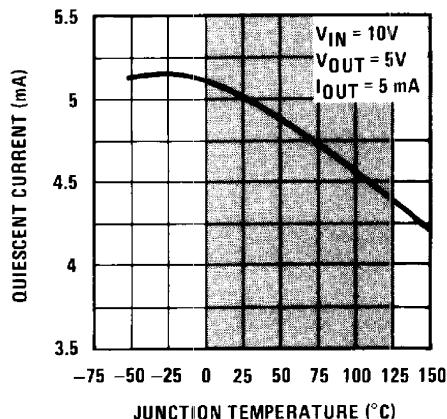


Figure 8. Dropout Characteristics



Shaded area refers to LM340A/LM340, LM7805, LM7812, and LM7815.

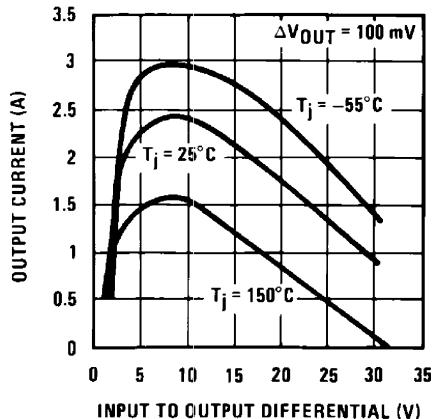
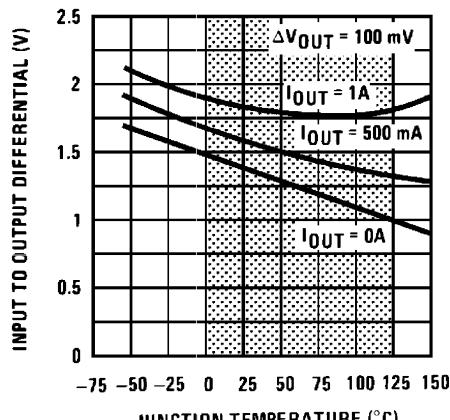


Figure 10. Peak Output Current



Shaded area refers to LM340A/LM340, LM7805, LM7812, and LM7815.

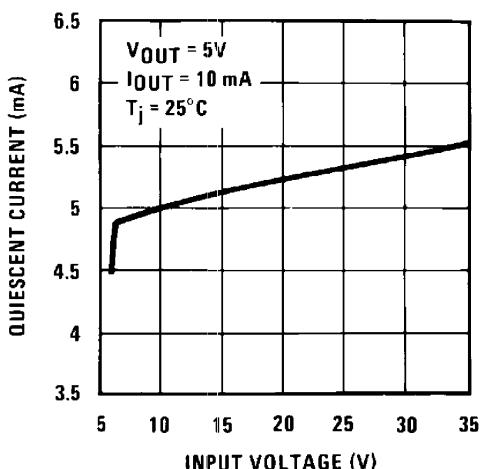
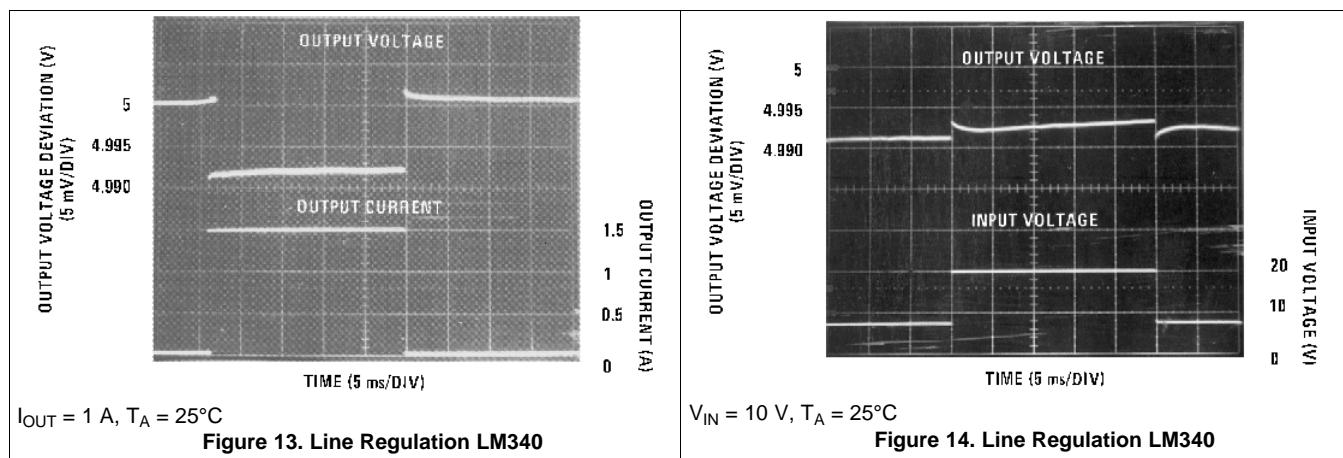


Figure 12. Quiescent Current

Typical Characteristics (continued)

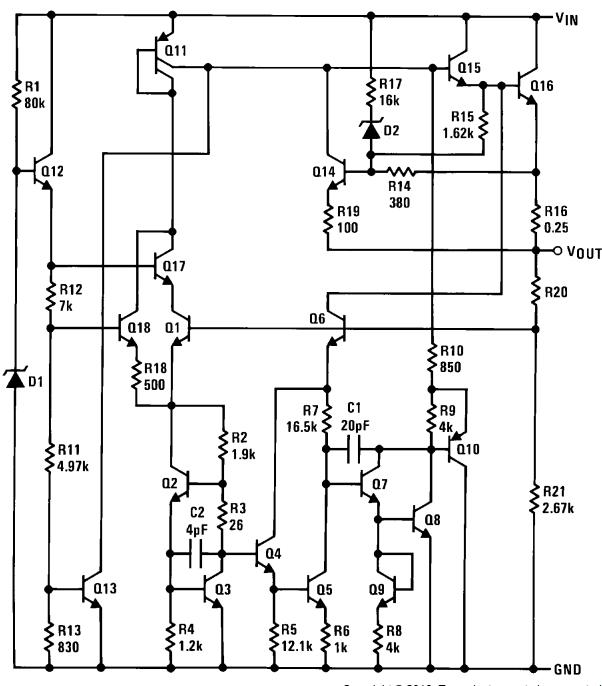


7 Detailed Description

7.1 Overview

The LM340 and LM7805 devices are a family of fixed output positive voltage regulators with outputs ranging from 3 V to 15 V. They accept up to 35 V of input voltage and with proper heat dissipation can provide over 1.5 A of current. With a combination of current limiting, thermal shutdown, and safe area protection, these regulators eliminate any concern of damage. These features paired with excellent line and load regulation make the LM340 and LM7805 Family versatile solutions to a wide range of power management designs. Although the LM340 and LM7805 Family were designed primarily as fixed-voltage regulators, these devices can be used with external component for adjustable voltage and current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Current

With proper considerations, the LM340 and LM7805 Family can exceed 1.5-A output current. Depending on the desired package option, the effective junction-to-ambient thermal resistance can be reduced through heat sinking, allowing more power to be dissipated in the device.

7.3.2 Current Limiting Feature

In the event of a short circuit at the output of the regulator, each device has an internal current limit to protect it from damage. The typical current limits for the LM340 and LM7805 Family is 2.4 A.

7.3.3 Thermal Shutdown

Each package type employs internal current limiting and thermal shutdown to provide safe operation area protection. If the junction temperature is allowed to rise to 150°C, the device will go into thermal shutdown.

7.4 Device Functional Modes

There are no functional modes for this device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM340x and LM7805 series is designed with thermal protection, output short-circuit protection, and output transistor safe area protection. However, as with any IC regulator, it becomes necessary to take precautions to assure that the regulator is not inadvertently damaged. The following describes possible misapplications and methods to prevent damage to the regulator.

8.1.1 Shorting the Regulator Input

When using large capacitors at the output of these regulators, a protection diode connected input to output (Figure 15) may be required if the input is shorted to ground. Without the protection diode, an input short causes the input to rapidly approach ground potential, while the output remains near the initial V_{OUT} because of the stored charge in the large output capacitor. The capacitor will then discharge through a large internal input to output diode and parasitic transistors. If the energy released by the capacitor is large enough, this diode, low current metal, and the regulator are destroyed. The fast diode in Figure 15 shunts most of the capacitors discharge current around the regulator. Generally no protection diode is required for values of output capacitance $\leq 10 \mu\text{F}$.

8.1.2 Raising the Output Voltage Above the Input Voltage

Because the output of the device does not sink current, forcing the output high can cause damage to internal low current paths in a manner similar to that just described in [Shorting the Regulator Input](#).

8.1.3 Regulator Floating Ground

When the ground pin alone becomes disconnected, the output approaches the unregulated input, causing possible damage to other circuits connected to V_{OUT} . If ground is reconnected with power ON, damage may also occur to the regulator. This fault is most likely to occur when plugging in regulators or modules with on card regulators into powered up sockets. The power must be turned off first, the thermal limit ceases operating, or the ground must be connected first if power must be left on. See [Figure 16](#).

8.1.4 Transient Voltages

If transients exceed the maximum rated input voltage of the device, or reach more than 0.8 V below ground and have sufficient energy, they will damage the regulator. The solution is to use a large input capacitor, a series input breakdown diode, a choke, a transient suppressor or a combination of these.

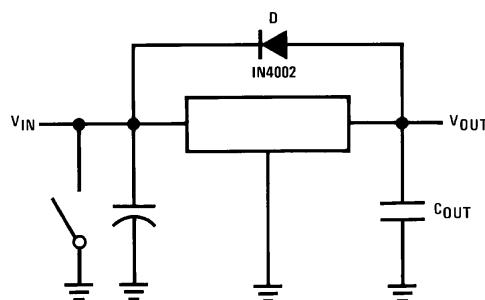


Figure 15. Input Short

Application Information (continued)

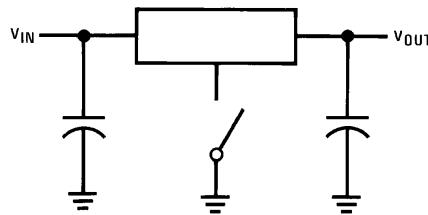


Figure 16. Regulator Floating Ground

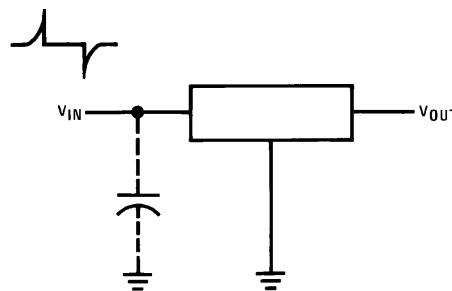


Figure 17. Transients

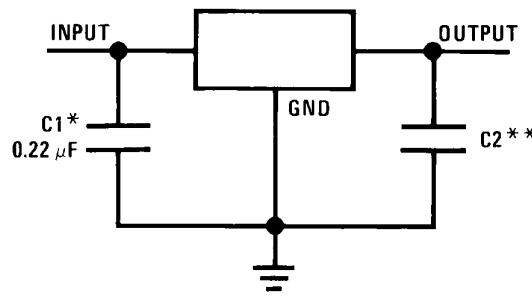
When a value for $\theta_{(H-A)}$ is found, a heat sink must be selected that has a *value that is less than or equal to this number*.

$\theta_{(H-A)}$ is specified numerically by the heat sink manufacturer in this catalog or shown in a curve that plots temperature rise vs power dissipation for the heat sink.

8.2 Typical Applications

8.2.1 Fixed Output Voltage Regulator

The LM340x and LM7805 Family devices are primarily designed to provide fixed output voltage regulation. The simplest implementation of LM340x and LM7805 Family is shown in Figure 18.



*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1-μF, ceramic disc).

Figure 18. Fixed Output Voltage Regulator

8.2.1.1 Design Requirements

The device component count is very minimal. Although not required, TI recommends employing bypass capacitors at the output for optimum stability and transient response. These capacitors must be placed as close as possible to the regulator. If the device is located more than 6 inches from the power supply filter, it is required to employ input capacitor.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

The output voltage is set based on the device variant. LM340x and LM7805 Family are available in 5-V, 12-V and 15-V regulator options.

8.2.1.3 Application Curve

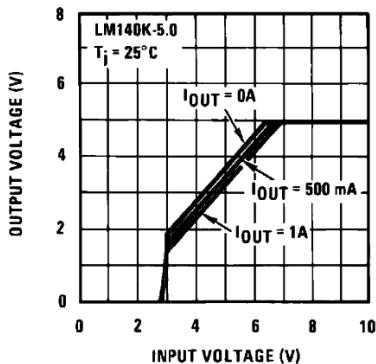
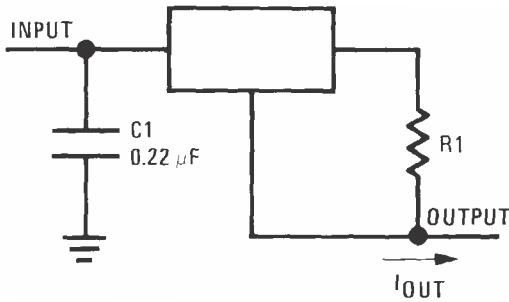


Figure 19. V_{OUT} vs V_{IN} , $V_{OUT} = 5$ V

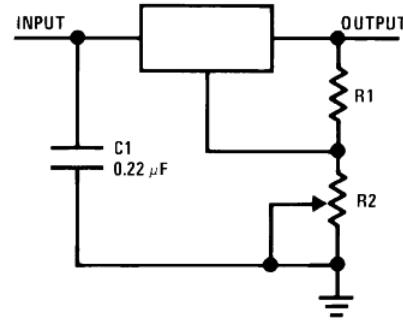
8.3 System Examples



$$I_{OUT} = V_2 - 3 / R_1 + I_Q$$

$$\Delta I_Q = 1.3 \text{ mA over line and load changes.}$$

Figure 20. Current Regulator



$$V_{OUT} = 5 \text{ V} + (5 \text{ V}/R_1 + I_Q) R_2 \quad 5 \text{ V}/R_1 > 3 I_Q,$$

load regulation (L_r) $\approx [(R_1 + R_2)/R_1] (L_r \text{ of LM340-5})$.

Figure 21. Adjustable Output Regulator

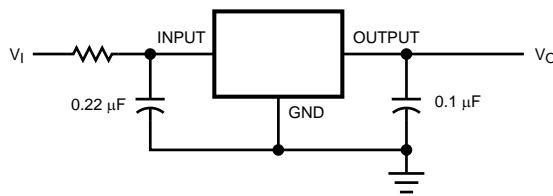


Figure 22. High Input Voltage Circuit With Series Resistor

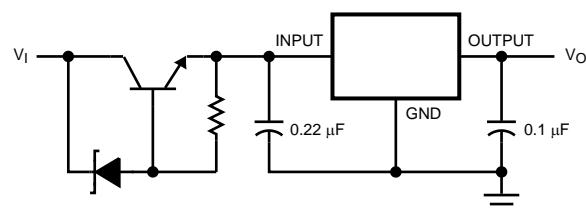
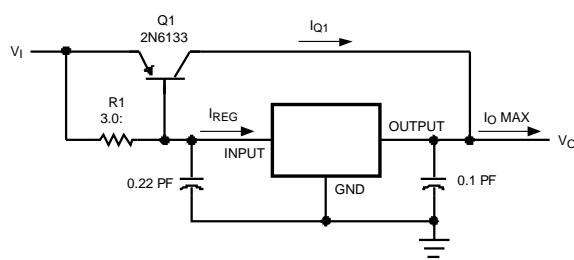


Figure 23. High Input Voltage Circuit implementation With Transistor

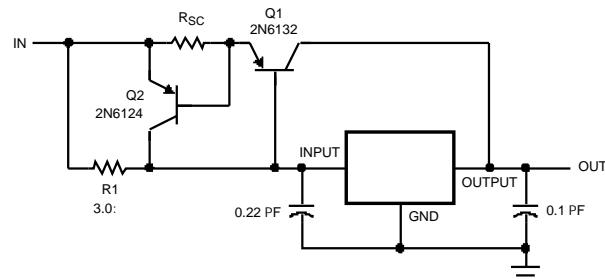
System Examples (continued)



$$\beta(Q1) \geq I_{O \text{ Max}} / I_{REG \text{ Max}}$$

$$R1 = 0.9 / I_{REG} = \beta(Q1) V_{BE(Q1)} / I_{REG \text{ Max}} (\beta + 1) - I_{O \text{ Max}}$$

Figure 24. High Current Voltage Regulator



$$R_{SC} = 0.8 / I_{SC}$$

$$R1 = \beta V_{BE(Q1)} / I_{REG \text{ Max}} (\beta + 1) - I_{O \text{ Max}}$$

Figure 25. High Output Current With Short-Circuit Protection

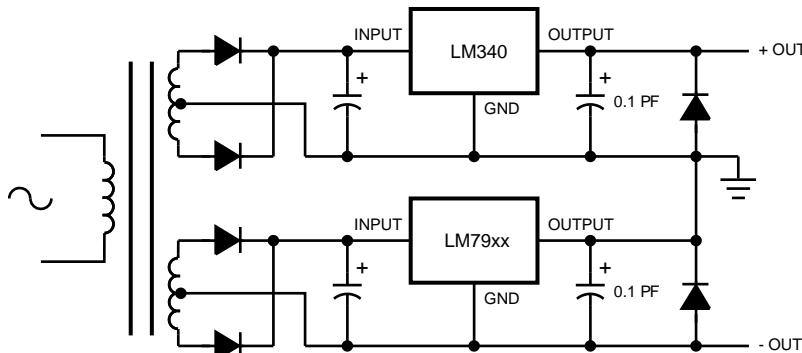


Figure 26. LM340 Used With Negative Regulator LM79xx

9 Power Supply Recommendations

The LM340 is designed to operate from a wide input voltage up to 35 V. Please refer to electrical characteristics tables for the minimum input voltage required for line/load regulation. If the device is more than six inches from the input filter capacitors, an input bypass capacitor, 0.1 μ F or greater, of any type is needed for stability.

10 Layout

10.1 Layout Guidelines

Some layout guidelines must be followed to ensure proper regulation of the output voltage with minimum noise. Traces carrying the load current must be wide to reduce the amount of parasitic trace inductance. To improve PSRR, a bypass capacitor can be placed at the OUTPUT pin and must be placed as close as possible to the IC. All that is required for the typical fixed output regulator application circuit is the LM340x/LM7805 Family IC and a 0.22- μ F input capacitor if the regulator is placed far from the power supply filter. A 0.1- μ F output capacitor is recommended to help with transient response. In cases when VIN shorts to ground, an external diode must be placed from VOUT to VIN to divert the surge current from the output capacitor and protect the IC.

10.2 Layout Example

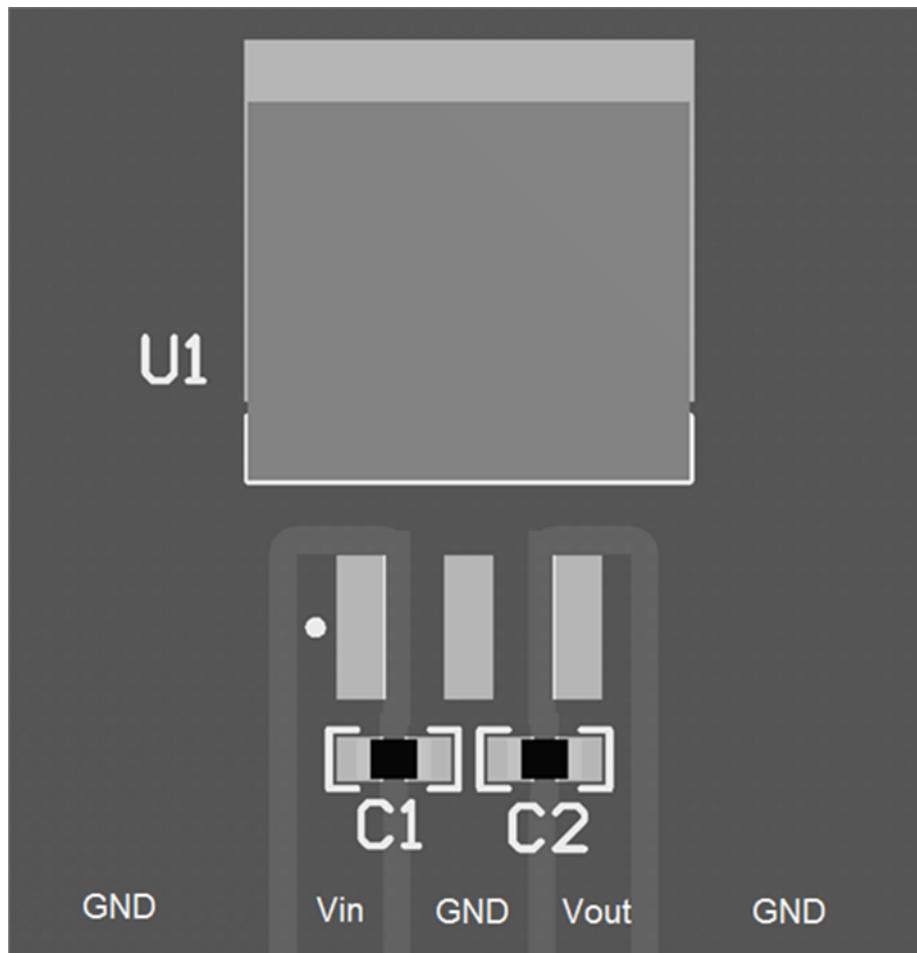


Figure 27. Layout Example DDPAK

Layout Example (continued)

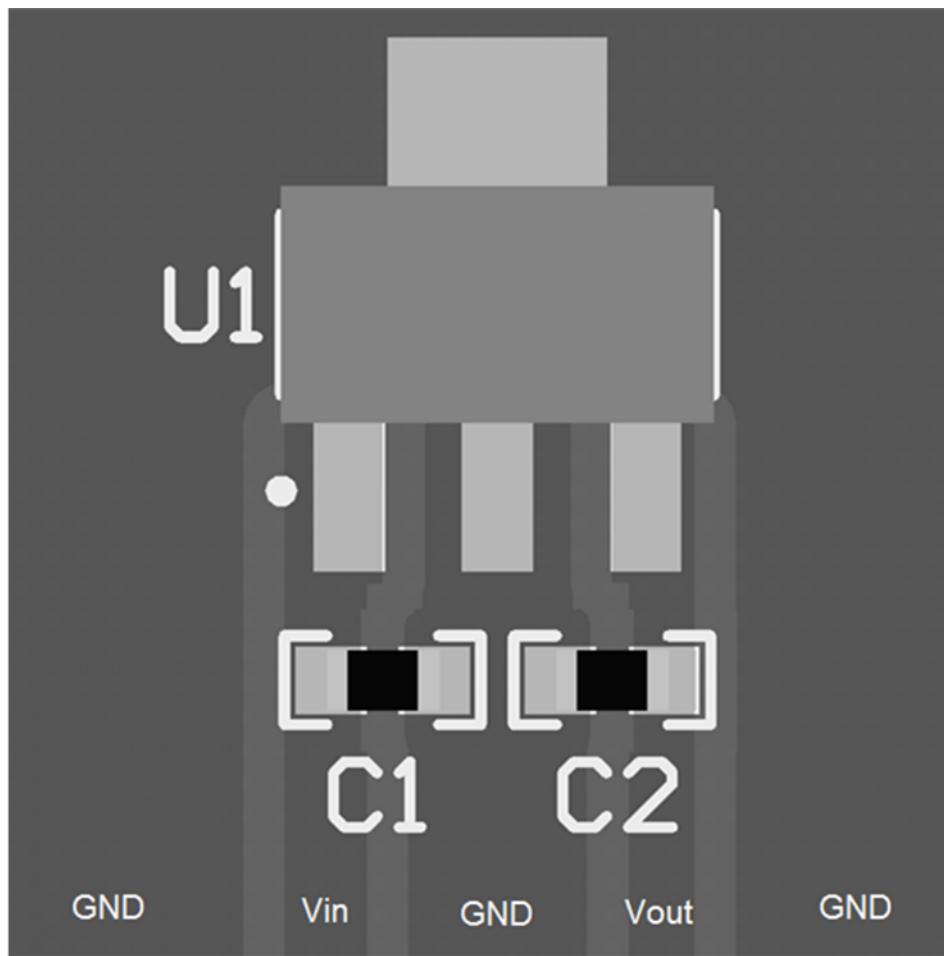


Figure 28. Layout Example SOT-223

10.3 Heat Sinking DDPAK/TO-263 and SOT-223 Package Parts

Both the DDPAK/TO-263 (KTT) and SOT-223 (DCY) packages use a copper plane on the PCB and the PCB itself as a heat sink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the plane.

Figure 29 shows for the DDPAK/TO-263 the measured values of $\theta_{(J-A)}$ for different copper area sizes using a typical PCB with 1-oz copper and no solder mask over the copper area used for heat sinking.

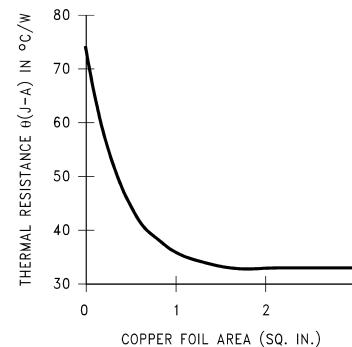


Figure 29. (J-A) vs Copper (1 Ounce) Area for the DDPAK/TO-263 Package

Heat Sinking DDPAK/TO-263 and SOT-223 Package Parts (continued)

As shown in [Figure 29](#), increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $\theta_{(J-A)}$ for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

As a design aid, [Figure 30](#) shows the maximum allowable power dissipation compared to ambient temperature for the DDPAK/TO-263 device (assuming $\theta_{(J-A)}$ is 35°C/W and the maximum junction temperature is 125°C).

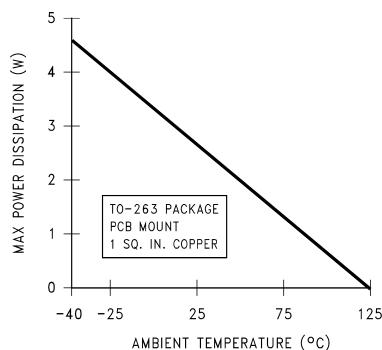


Figure 30. Maximum Power Dissipation vs T_{AMB} for the DDPAK/TO-263 Package

[Figure 31](#) and [Figure 32](#) show the information for the SOT-223 package. [Figure 31](#) assumes a $\theta_{(J-A)}$ of 74°C/W for 1-oz. copper and 51°C/W for 2-oz. copper and a maximum junction temperature of 125°C.

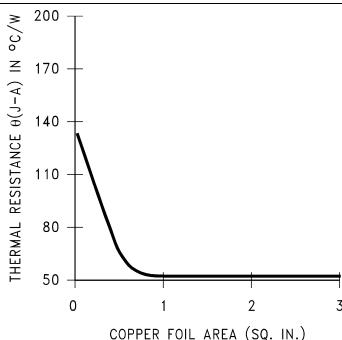


Figure 31. (J-A) vs Copper (2 Ounce) Area for the SOT-223 Package

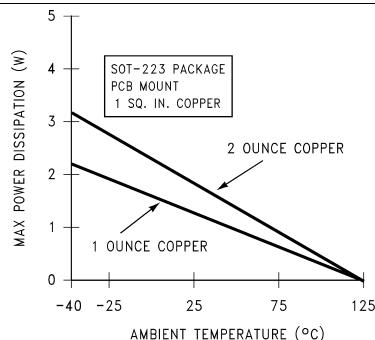


Figure 32. Maximum Power Dissipation vs T_{AMB} for the SOT-223 Package

See [AN-1028 LMX2370 PLLatinum Dual Freq Synth for RF Pers Comm LMX2370 2.5GHz/1.2GHz](#) (SNVA036) for power enhancement techniques to be used with the SOT-223 package.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- [AN-1028 LMX2370 PLLatinum Dual Freq Synth for RF Pers Comm LMX2370 2.5GHz/1.2GHz](#) (SNVA036)
- [LM140K Series 3-Terminal Positive Regulators](#) (SNVS994)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM340	Click here				
LM340A	Click here				
LM7805	Click here				
LM7812	Click here				
LM7815	Click here				

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

[SLYZ022 — TI Glossary.](#)

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM340AT-5.0	NRND	TO-220	NDE	3	45	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM340AT 5.0 P+	
LM340AT-5.0/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS-Exempt & Green	SN	Level-1-NA-UNLIM	0 to 125	LM340AT 5.0 P+	Samples
LM340K-5.0	ACTIVE	TO-3	NDS	2	50	Non-RoHS & Non-Green	Call TI	Call TI	0 to 125	LM340K -5.0 7805P+	Samples
LM340K-5.0/NOPB	ACTIVE	TO-3	NDS	2	50	RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 125	LM340K -5.0 7805P+	Samples
LM340MP-5.0	NRND	SOT-223	DCY	4	1000	Non-RoHS & Green	Call TI	Call TI	0 to 70	N00A	
LM340MP-5.0/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	N00A	Samples
LM340MPX-5.0/NOPB	ACTIVE	SOT-223	DCY	4	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	N00A	Samples
LM340S-12/NOPB	ACTIVE	DDPAK/TO-263	KT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -12 P+	Samples
LM340S-5.0	NRND	DDPAK/TO-263	KT	3	45	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM340S -5.0 P+	
LM340S-5.0/NOPB	ACTIVE	DDPAK/TO-263	KT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -5.0 P+	Samples
LM340SX-12/NOPB	ACTIVE	DDPAK/TO-263	KT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -12 P+	Samples
LM340SX-5.0	NRND	DDPAK/TO-263	KT	3	500	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM340S -5.0 P+	
LM340SX-5.0/NOPB	ACTIVE	DDPAK/TO-263	KT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -5.0 P+	Samples
LM340T-12	NRND	TO-220	NDE	3	45	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM340T12 7812 P+	
LM340T-12/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM		LM340T12 7812 P+	Samples
LM340T-15	NRND	TO-220	NDE	3	45	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM340T15 7815 P+	
LM340T-15/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	0 to 125	LM340T15 7815 P+	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM340T-5.0	NRND	TO-220	NDE	3	45	Non-RoHS & Green	Call TI	Call TI	0 to 70	LM340T5 7805 P+	
LM340T-5.0/LF01	ACTIVE	TO-220	NDG	3	45	RoHS-Exempt & Green	SN	Level-4-260C-72 HR	0 to 125	LM340T5 7805 P+	Samples
LM340T-5.0/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS-Exempt & Green	SN	Level-1-NA-UNLIM	0 to 125	LM340T5 7805 P+	Samples
LM7805CT	NRND	TO-220	NDE	3	45	Non-RoHS & Green	Call TI	Call TI	0 to 125	LM340T5 7805 P+	
LM7805CT/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS-Exempt & Green	SN	Level-1-NA-UNLIM	0 to 125	LM340T5 7805 P+	Samples
LM7805MP/NOPB	ACTIVE	SOT-223	DCY	4	1000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	N00A	Samples
LM7805MPX/NOPB	ACTIVE	SOT-223	DCY	4	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	N00A	Samples
LM7805S/NOPB	ACTIVE	DDPAK/ TO-263	KT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -5.0 P+	Samples
LM7805SX/NOPB	ACTIVE	DDPAK/ TO-263	KT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -5.0 P+	
LM7812CT/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LM340T12 7812 P+	Samples
LM7812S/NOPB	ACTIVE	DDPAK/ TO-263	KT	3	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -12 P+	Samples
LM7812SX/NOPB	ACTIVE	DDPAK/ TO-263	KT	3	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	0 to 125	LM340S -12 P+	
LM7815CT/NOPB	ACTIVE	TO-220	NDE	3	45	RoHS & Green	SN	Level-1-NA-UNLIM	0 to 125	LM340T15 7815 P+	Samples
LM78S40CN/NOPB	ACTIVE	PDIP	NFG	16	25	RoHS & Non-Green	SN	Level-1-NA-UNLIM	0 to 70	LM78S40CN	Samples
LM78S40N/NOPB	LIFEBUY	PDIP	NFG	16	25	RoHS & Green	SN	Level-1-NA-UNLIM	0 to 125	LM78S40N	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

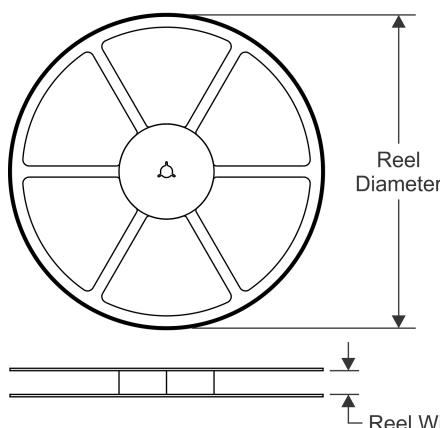
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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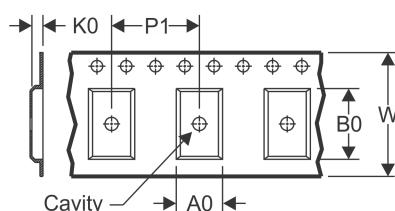
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

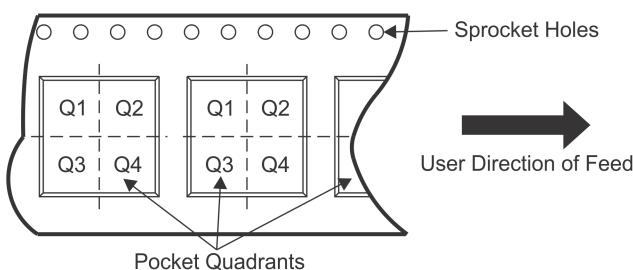


TAPE DIMENSIONS



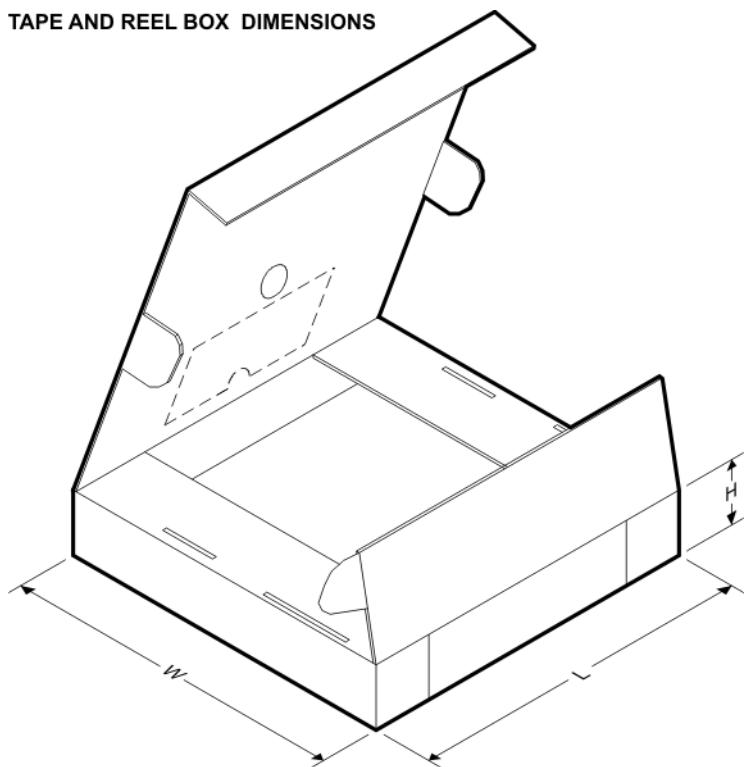
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM340MP-5.0	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM340MP-5.0/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM340MPX-5.0/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM340SX-12/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM340SX-5.0	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM340SX-5.0/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM7805MP/NOPB	SOT-223	DCY	4	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM7805MPX/NOPB	SOT-223	DCY	4	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LM7805SX/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM7812SX/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

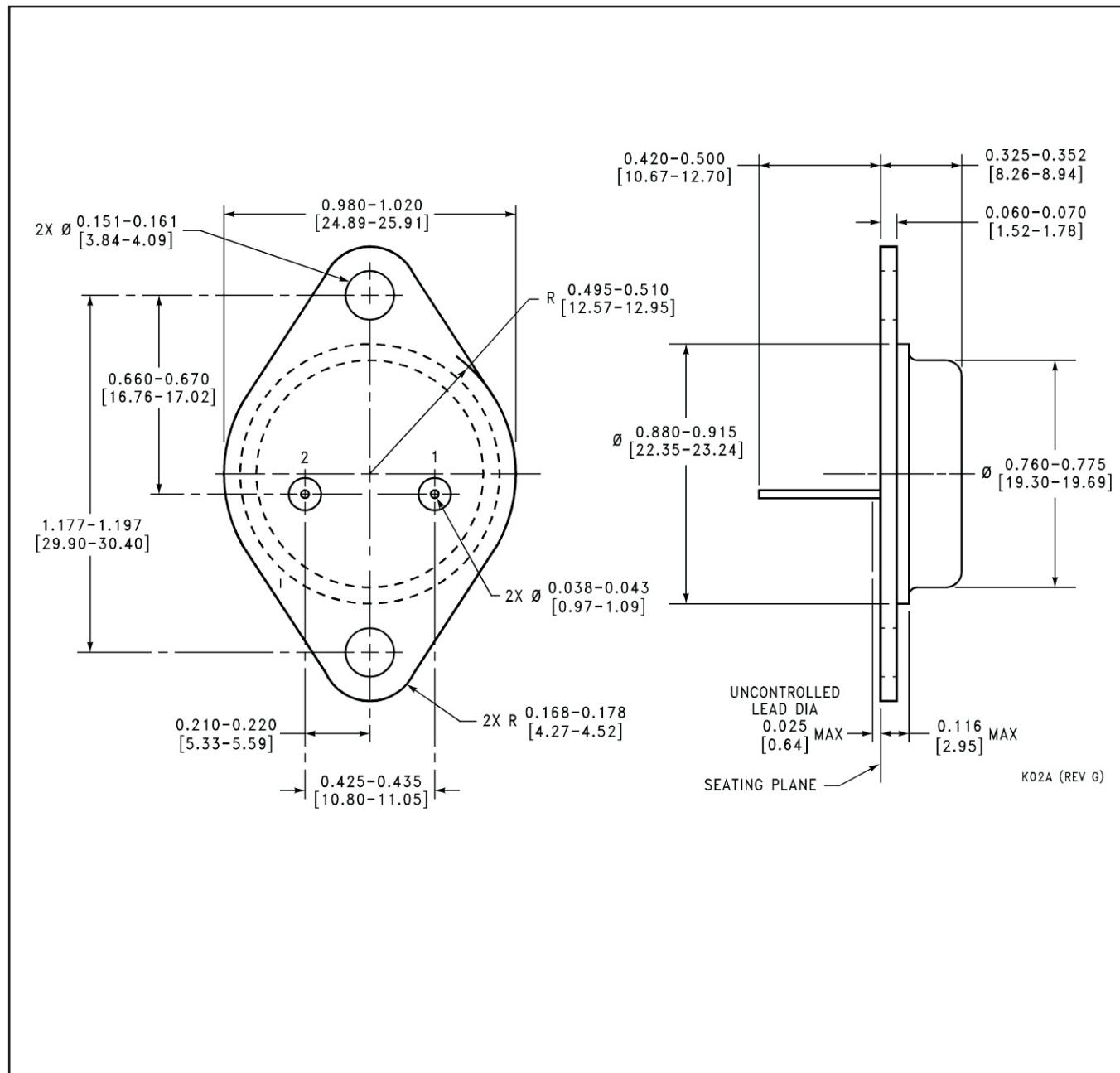
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM340MP-5.0	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM340MP-5.0/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM340MPX-5.0/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM340SX-12/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM340SX-5.0	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM340SX-5.0/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM7805MP/NOPB	SOT-223	DCY	4	1000	367.0	367.0	35.0
LM7805MPX/NOPB	SOT-223	DCY	4	2000	367.0	367.0	35.0
LM7805SX/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM7812SX/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0

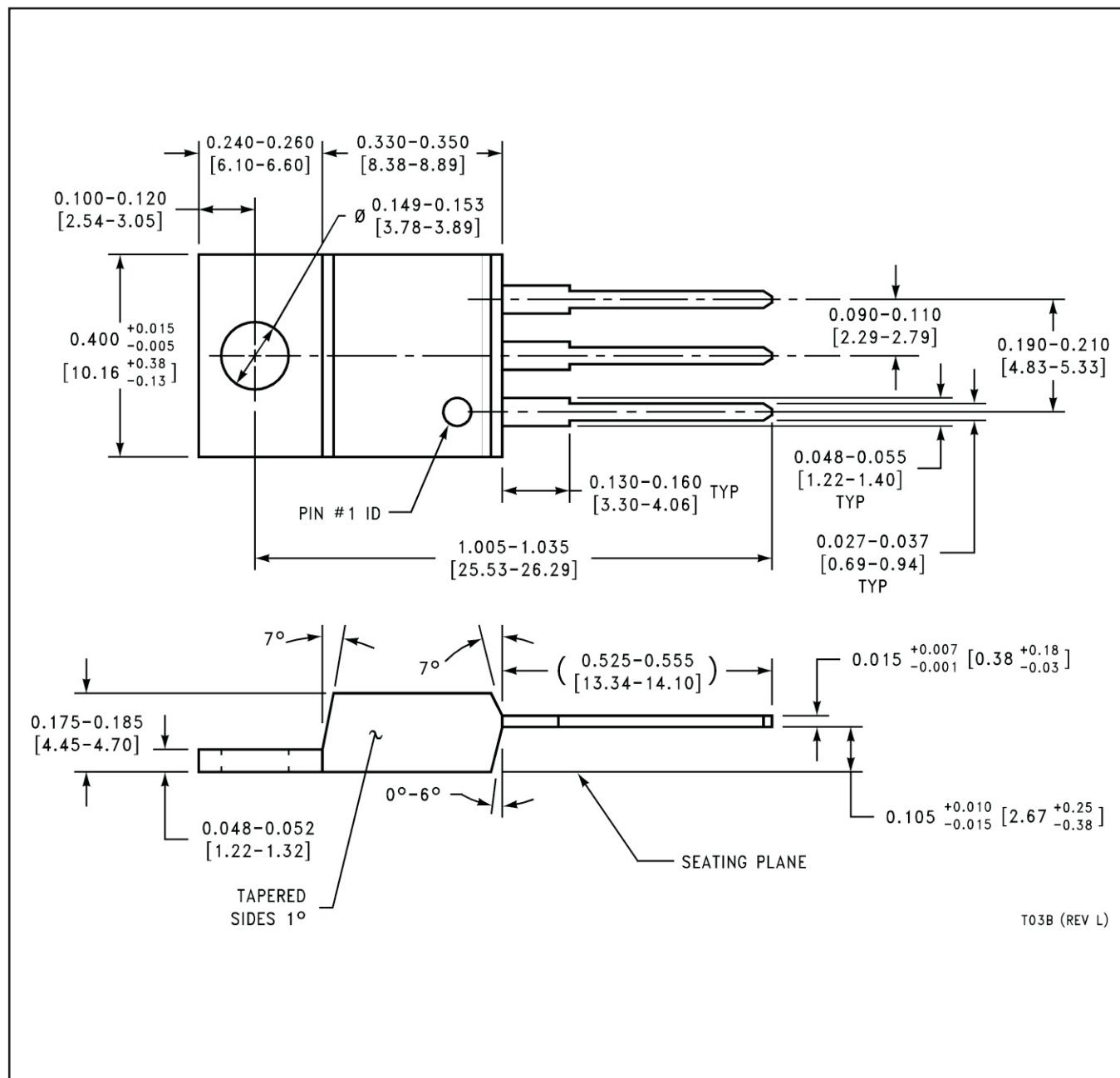
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NDS002A



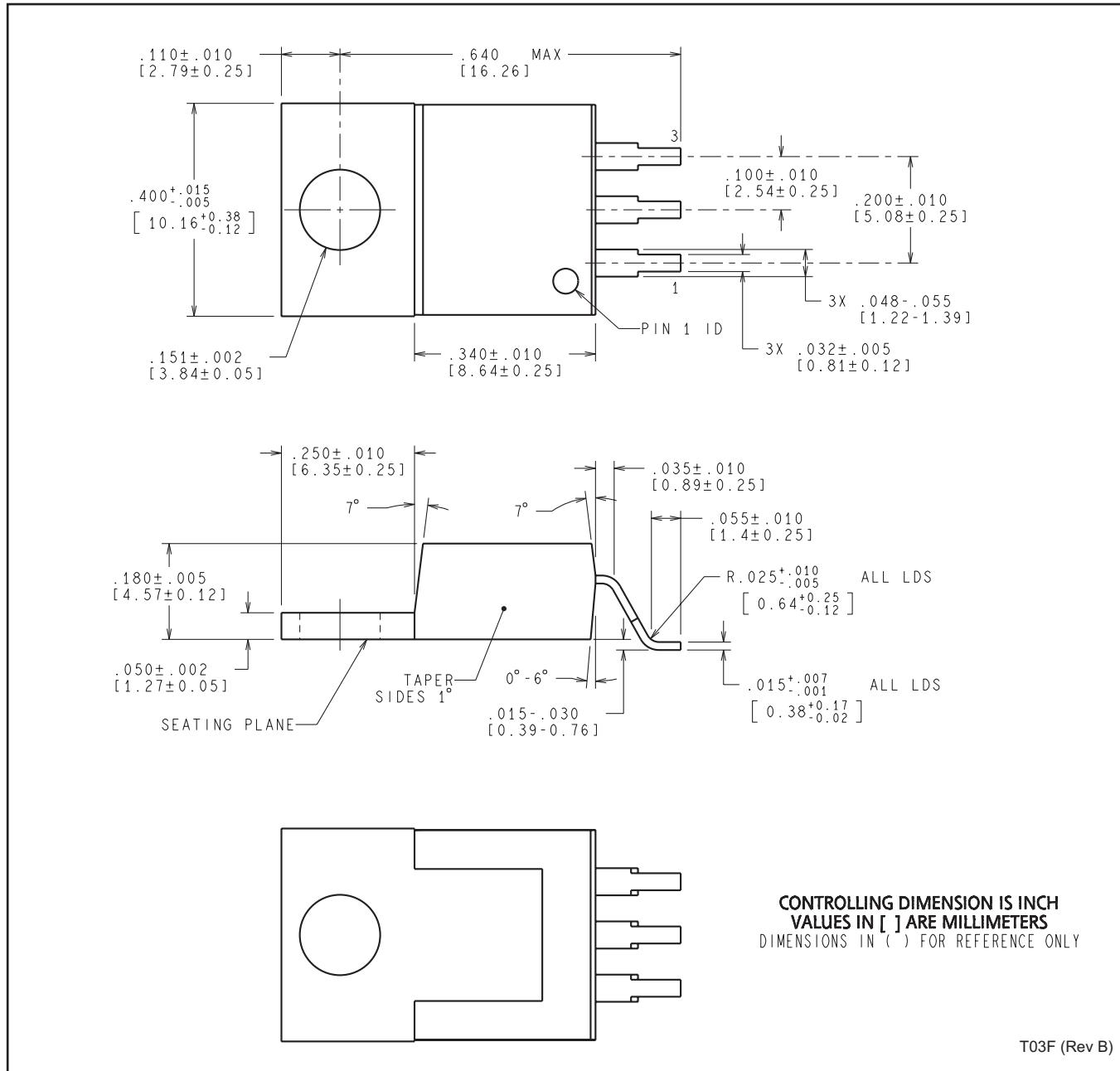
MECHANICAL DATA

NDE0003B



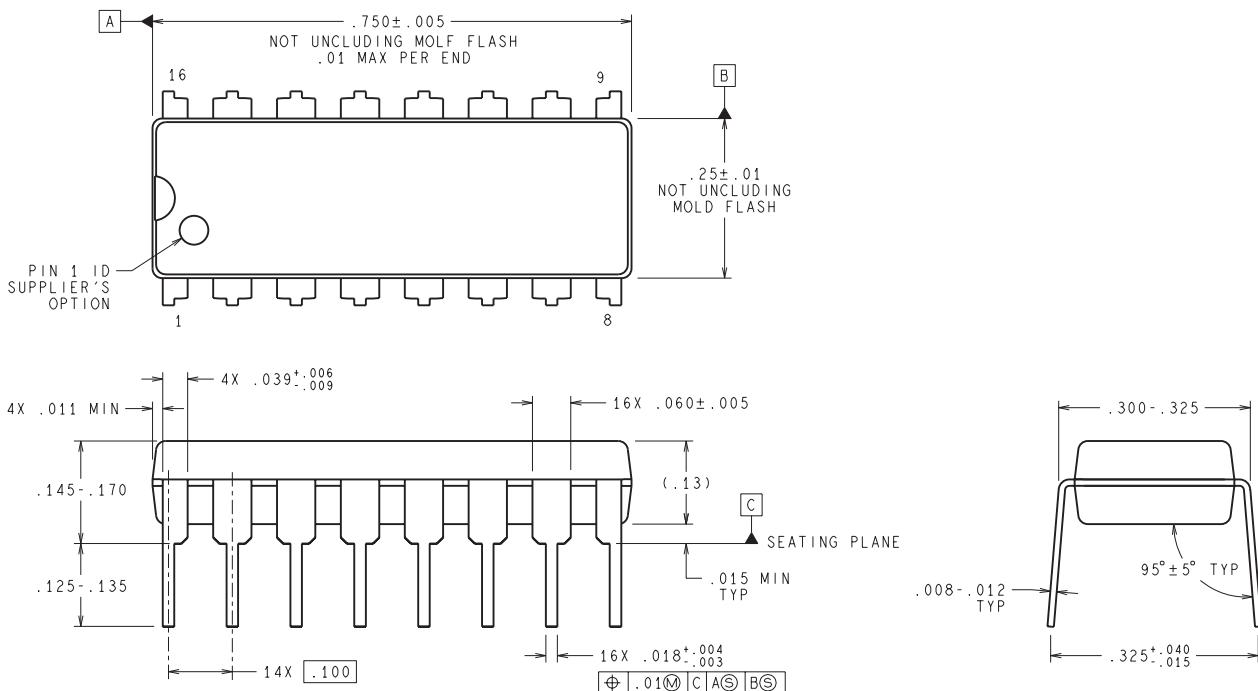
MECHANICAL DATA

NDG0003F



MECHANICAL DATA

N0016E

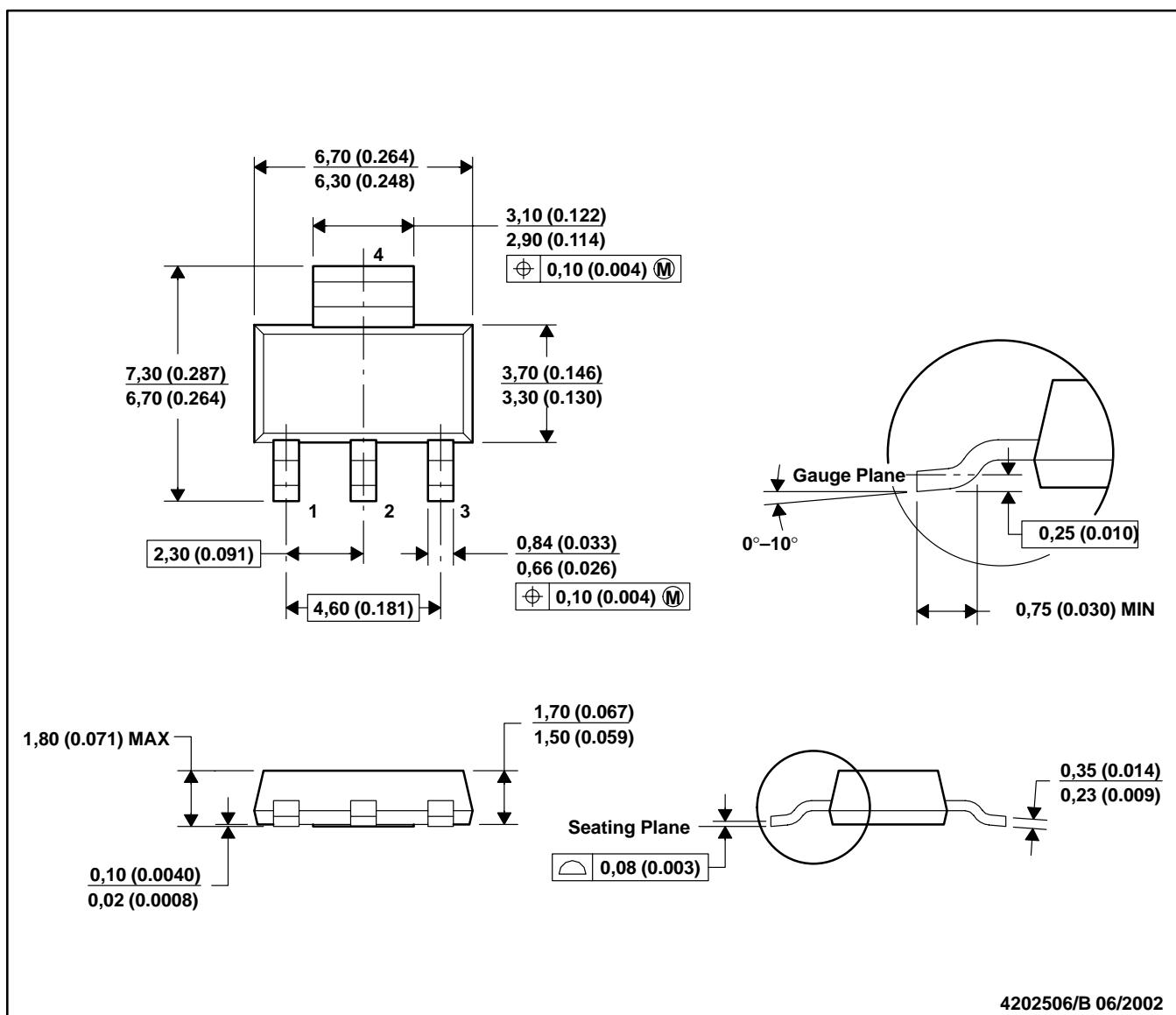


DIMENSIONS ARE IN INCHES
DIMENSIONS IN () FOR REFERENCE ONLY

N16E (Rev G)

DCY (R-PDSO-G4)

PLASTIC SMALL-OUTLINE



NOTES:

- A. All linear dimensions are in millimeters (inches).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC TO-261 Variation AA.

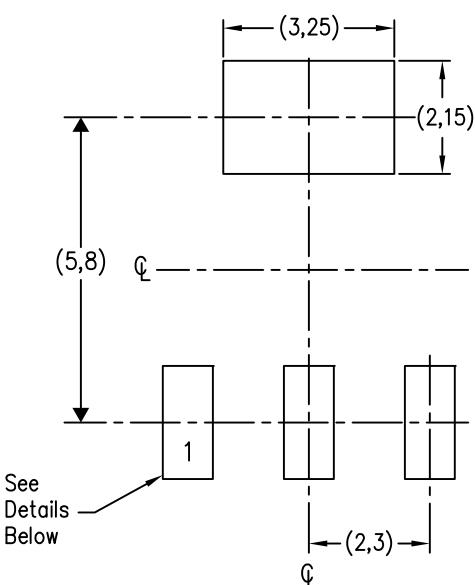
4202506/B 06/2002

LAND PATTERN DATA

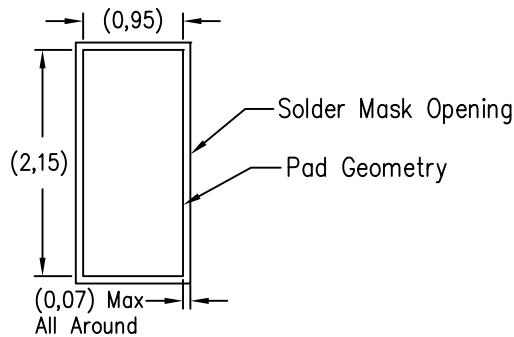
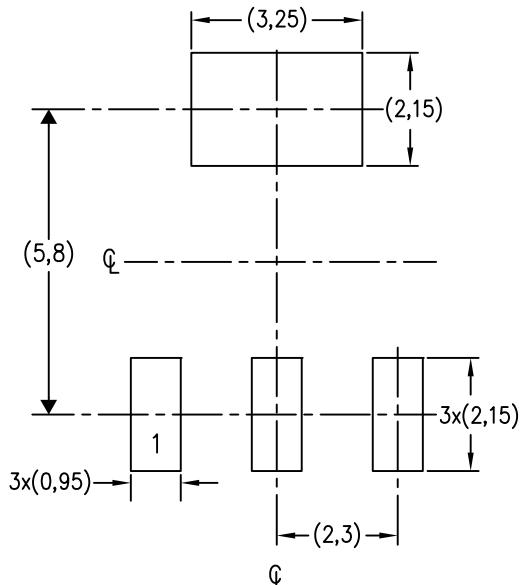
DCY (R-PDSO-G4)

PLASTIC SMALL OUTLINE

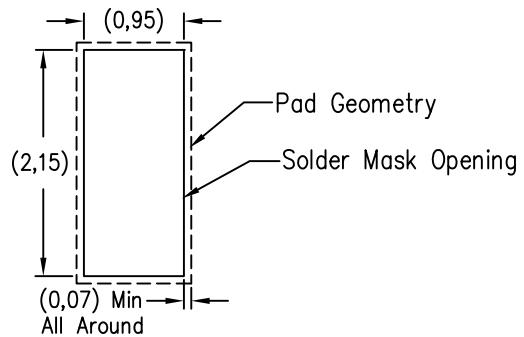
Example Board Layout



Example Stencil Design
0.125 Thick Stencil
(Note D)



Example, non-solder mask defined pad.
(Preferred)



Example, solder mask defined pad.

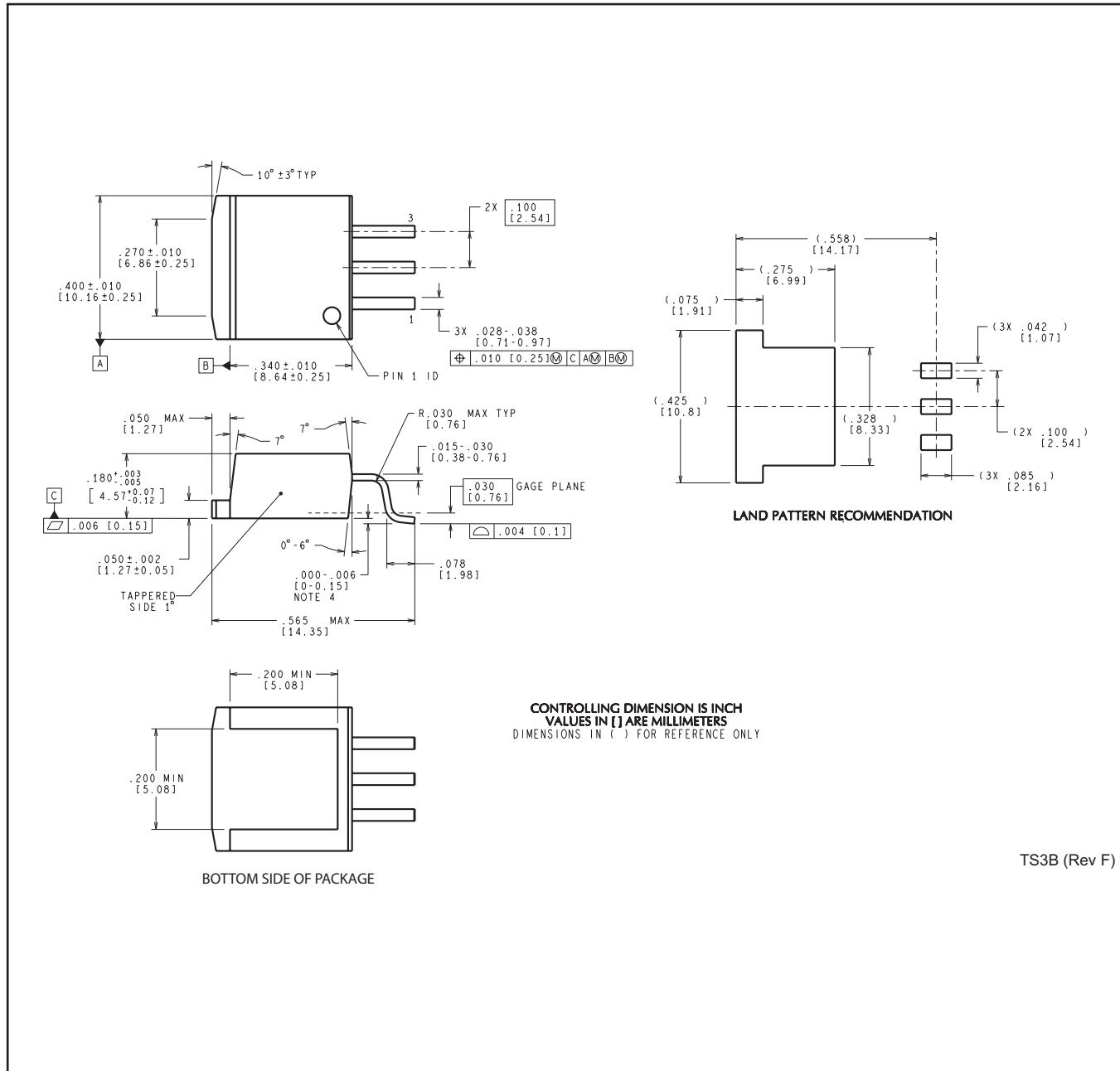
4210278/C 07/13

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

MECHANICAL DATA

KTT0003B



TS3B (Rev F)

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