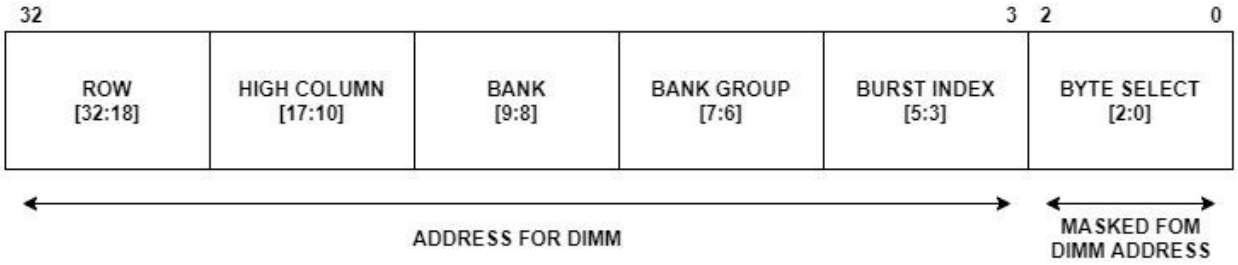
ECE 585 - Fall 21 - Group 9 Checkpoint 2 Report



Address Mapping reasoning:

- Since the DIMM provides a 64 bit bus, [2:0] address bits are masked from the DIMM.
- Bits [5:3] are used to take advantage of burst mode which is considered as 8 here.
- Bank Group address bits are on the lower index compared to Bank because in DDR4, prefetch can be done in 2 different bank groups independently.
- High Column Address is next because the memory controller implements open page policy. This means that keeping maximum pages open at once is gonna increase the likelihood of finding the requested address in an open page.
- Row address lies on the MSB since it requires pre-charging (to close the open row) and activating (to open a new row) a new row.