THE IMAGINATION UNIVERSITY PROGRAMME

RVfpga Lab 0
Overview of RVfpga Labs

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0. PREFACE

This RVfpga course in Computer Architecture provides hands-on understanding of a commercial RISC-V processor, RISC-V SoC, and the RISC-V ecosystem. The course provides an understanding of the system from the underlying digital design and signals to the instruction set architecture and processor to the programming environment, boot code, and compiler. The fact that RVfpga users walk away with this top to bottom understanding of the RISC-V system is remarkable. They not only have a working RISC-V SoC and ecosystem, but they know how to use and expand the RISC-V processor and system for future projects and research.

Professor David Patterson, who shared the ACM A.M. Turing Award with John Hennessy for their contribution to RISC, says, “RISC-V is transforming processor design and software/hardware co-design. RISC-V is an open architecture, which enables open-source hardware implementations. This new option means that software development can occur alongside hardware development, accelerating the design path. The RVfpga course enhances the understanding of not only RISC-V processors but also the RISC-V ecosystem and RISC-V SoCs. This course provides a deep understanding of an industrial-strength processor architecture and system of increasing popularity, which will prove useful throughout their academic and industry careers.”

1. RVfpga LABS OVERVIEW

These RVfpga Labs provide hands-on understanding of RISC-V hardware and software. Before starting RVfpga Labs, you must have already completed the RVfpga Getting Started Guide provided by the Imagination University Programme (https://university.imgtec.com/). For example, if you have not already, install Xilinx's Vivado, PlatformIO and Verilator following the instructions in that guide. Also, make sure that you have copied the ***RVfpga*** folder that you downloaded from Imagination's University Programme to your machine. We will refer to the absolute path of the directory where you place folder RVfpga as [*RVfpgaPath*]. The RVfpga/src folder contains the Verilog and SystemVerilog sources for the RVfpga System, the RISC-V SoC that we will use and modify throughout the labs. The RVfpga/Labs folder contains resources for the labs, listed in Table 1.

Table 1. RVfpga Labs

	#	Title
Part 1	0	RVfpga Labs Overview
	1	Creating a Vivado Project
	2	C Programming
	3	RISC-V Assembly Language
	4	Function Calls
	5	Image Processing: Projects with C & Assembly
	6	Introduction to I/O
	7	7-Segment Displays
	8	Timers
	9	Interrupt-Driven I/O
	10	Serial Buses
Part 2	11	SweRV EH1 Configuration and Organization. Performance Monitoring
	12	Arithmetic/Logical Instructions: `add`
	13	Memory Instructions: the `lw` and `sw` Instructions
	14	Structural Hazards
	15	Data Hazards
	16	Control Hazards. Branch Instructions: `beq` and the Branch Predictor
	17	Superscalar Execution
	18	Adding New Features (Instructions, Hardware Counters) to the Core
	19	Memory Hierarchy: The Instruction Cache (I$)
	20	I$, ICCM, DCCM, and Benchmarking
		SweRV EH1 Reference

Labs 1-10 (Part 1) show how to use the RISC-V SoC and toolchain (compilers and simulators), and they show how to add peripherals to the SoC. Specifically, Lab 1 shows how to view the SweRVolfX SoC source code and target it to an FPGA (Lab 1), how to run programs on RVfpgaNexys, RVfpgaSim and Whisper (Labs 2-5), and how to modify the RVfpga System to add peripherals (Labs 6-10).

Labs 11-20 (Part 2) focus on microarchitecture and memory hierarchy; they show how to understand the RISC-V pipeline and use or add features to the RISC-V core, including additional instructions, other branch predictors, and memory features.

These labs are well-suited for two-semester course for undergraduates. Labs 11-20 could also be taught to master's level students. Prior to completing this RVfpga course, students should understand the fundamentals of logic design, computer architecture, processor design, input/output systems and C/assembly programming. This material is covered in the textbook *Digital Design & Computer Architecture: RISC-V Edition*, Harris & Harris, © Elsevier October, 2021.

Table 2 lists the required software and optional hardware needed to use these labs. All of the software is free. The Nexys A7 FPGA board (or, equivalently, Nexys DDR FPGA board) is not required to complete the labs. Instead, you can complete these labs using Whisper (Western Digital's Instruction Set Simulator) and Verilator (an open-source HDL simulator).

Table 2. Required Software and Optional Hardware

Software	
Vivado 2019.2 WebPACK*	https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2019-2.html
VS Code	https://code.visualstudio.com/Download
PlatformIO	https://platformio.org/ (Installed within VSCode)
Verilator and GTKWave	https://github.com/verilator/verilator http://gtkwave.sourceforge.net/
Whisper (Western Digital's RISC-V Instruction Set Simulator)	https://github.com/chipsalliance/SweRV-ISS (Installed within PlatformIO)
RISC-V Toolchain and OpenOCD	https://github.com/riscv/riscv-gnu-toolchain, https://github.com/riscv/riscv-openocd (Installed within PlatformIO)
Hardware	
Nexys A7 FPGA Board*	https://store.digilentinc.com/nexys-a7-fpga-trainer-board-recommended-for-ece-curriculum/
RISC-V Core and System-on-Chip (SoC)	
Western Digital's SweRV EH1	https://github.com/chipsalliance/Cores-SweRV (included in RVfpga package)
SweRVolf	https://github.com/chipsalliance/Cores-SweRVolf (included in RVfpga package)

* optional

The organization of the **RVfpga/src** folder is explained in the GSG and in Labs 1-20.

The organization of the **RVfpga/Labs** folder is as follows:

- Folder **LabInstructions:**
  - Instructions for each lab, including tasks and exercises.
  - Folder **Figures**: Figures used in the instructions for each lab.

- Folders **Lab1, Lab2, … , Lab19, Lab20:** Resources to be used while completing the labs.

- Folder **RVfpgaLabsSolutions:** Exercise solutions for each of the labs. **Instructors should remove this folder before distributing RVfpga to students**.
  - Folder **Programs_Solutions:** documents and software with the solutions for the proposed tasks and exercises.
  - Folder **RVfpga_Solutions:** Modified RVfpga System source code (Verilog and SystemVerilog) extended as guided by the exercises in Labs 6-10. The source code is in folder [RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/RVfpga_Solutions/src, where the bitstream (rvfpganexys.bit) is also provided. The document [RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/RVfpga_Solutions/RVfpgaModifications.docx describes the modifications performed to RVfpga System in the Exercises of Labs 6-10. Note that not all exercises have solutions provided.