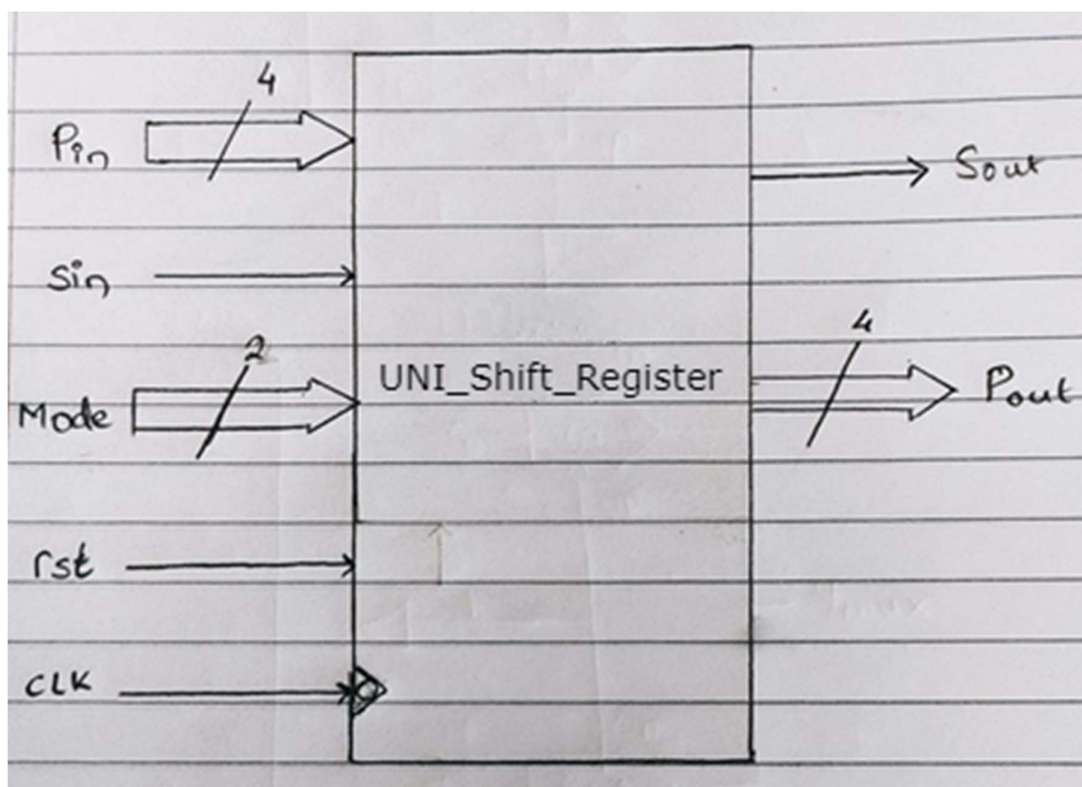


Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	A.2
Assignment Name	:	Universal Shift Register (4 Modes : SISO , SIPO , PISO , PIPO)
Date Of Performance	:	

BLOCK DIAGRAM



FUNCTION TABLE

rst	clk	MODE		Output
		M ₁	M ₀	
1	x	x	x	x
0	↓	0	0	Serial In Serial Out (SISO)
0	↓	0	1	Serial In Parallel Out (SIPO)
0	↓	1	0	Parallel In Serial Out (PISO)
0	↓	1	1	Parallel In Parallel Out (PIPO)

MAIN VHDL MODEL (MVM)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity UNI_Shift_Register is
  Port ( rst : in  STD_LOGIC;
        clk : in  STD_LOGIC;
        Sin : in  STD_LOGIC;
        mode : in  STD_LOGIC_VECTOR (1 downto 0);
        Pin : in  STD_LOGIC_VECTOR (3 downto 0);
        Sout : out STD_LOGIC;
        Pout : out STD_LOGIC_VECTOR (3 downto 0)
        );
end UNI_Shift_Register;

architecture UNI_Shift_Register_arch of UNI_Shift_Register is
  SIGNAL temp : STD_LOGIC_VECTOR (3 downto 0):="0000";
  begin
    PROCESS(rst, clk, mode, Sin, Pin)
    BEGIN
      IF rst = '1' THEN
        Pout <= "0000";
        Sout <= '0';

      ELSIF FALLING_EDGE(clk) THEN

        CASE mode IS

          WHEN "00" =>
            temp(3 downto 1) <= temp(2 downto 0);
            temp(0) <= Sin;

            Sout <= temp(3);
            Pout <= "0000";

          WHEN "01" =>
            temp(3 downto 1) <= temp(2 downto 0);
            temp(0) <= Sin;
            Pout <= temp;
            Sout <= '0';

          WHEN "10" =>
            temp <= Pin;
            Sout <= temp(3);
            temp(3 downto 1) <= temp(2 downto 0);
```

```

        Pout <= "0000";

        WHEN OTHERS =>
            Pout <= Pin;
            Sout <= '0';

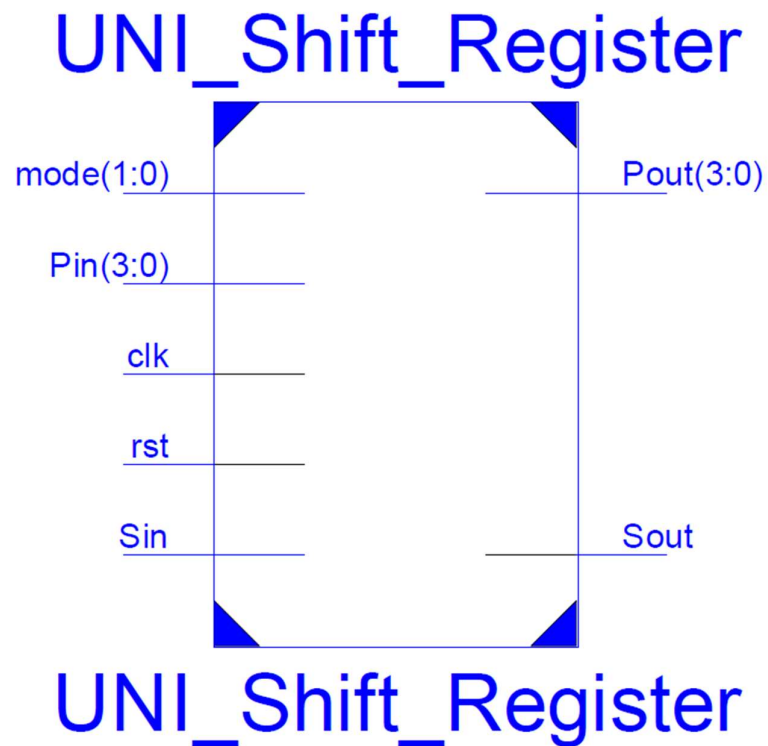
        END CASE;

    END IF;
END PROCESS;

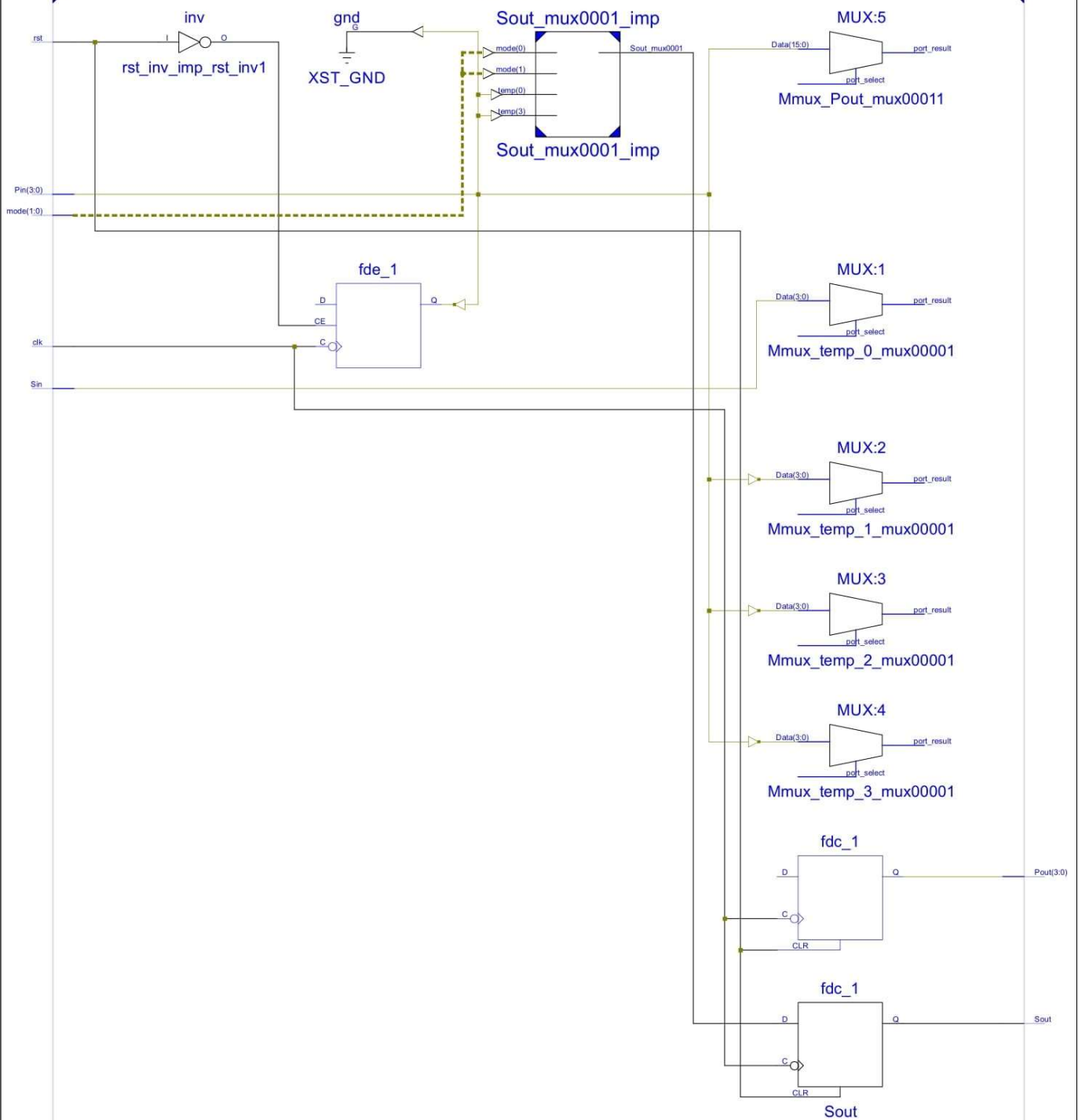
end UNI_Shift_Register_arch;

```

RTL SCHEMATIC:

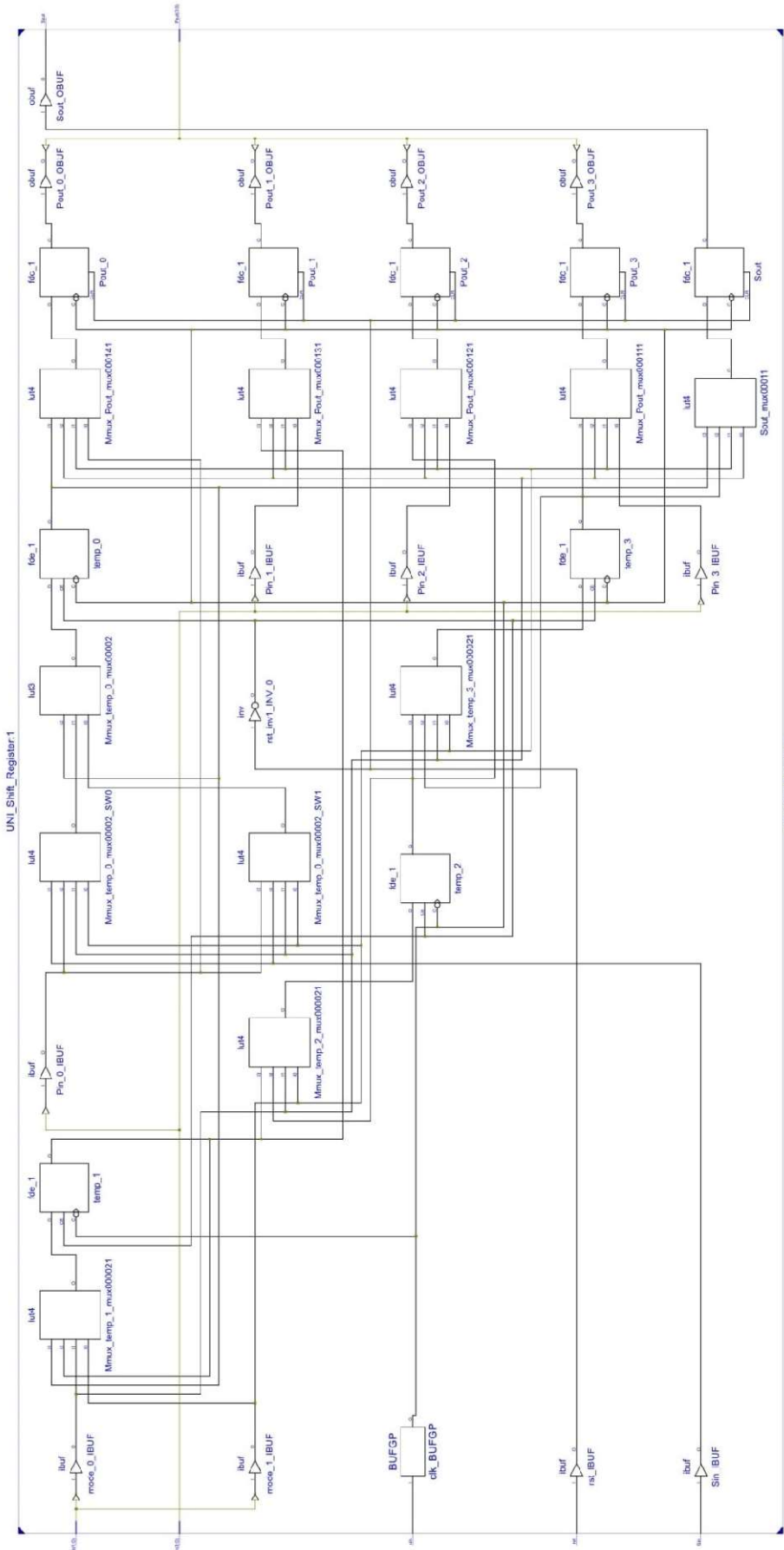


UNI_Shift_Register:1



UNI_Shift_Register

TECHNOLOGY SCHEMATIC



SYNTHESIS REPORT

a) Device Utilization Summary:

```
=====
*                               *
Final Report
=====
```

Final Results

RTL Top Level Output File Name : UNI_Shift_Register.ngc
Top Level Output File Name : UNI_Shift_Register
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : No

Design Statistics

IOs : 14

Cell Usage :

BELS : 12
INV : 1
LUT3 : 1
LUT4 : 10
FlipFlops/Latches : 9
FDC_1 : 5
FDE_1 : 4
Clock Buffers : 1
BUFGP : 1
IO Buffers : 13
IBUF : 8
OBUF : 5

Device utilization summary:

Selected Device : 3s250epq208-5

Number of Slices:	6 out of 2448	0%
Number of Slice Flip Flops:	9 out of 4896	0%
Number of 4 input LUTs:	12 out of 4896	0%
Number of IOs:	14	
Number of bonded IOBs:	14 out of 158	8%
Number of GCLKs:	1 out of 24	4%

b) TIMING REPORT:

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

```
-----+-----+-----+
Clock Signal | Clock buffer(FF name) | Load |
```

clk	BUFGP	9	
-----	-------	---	--

Asynchronous Control Signals Information:

Control Signal	Buffer(FF name)	Load	
rst	IBUF	5	

Timing Summary:

Speed Grade: -5

Minimum period: 1.923ns (Maximum Frequency: 520.034MHz)

Minimum input arrival time before clock: 4.009ns

Maximum output required time after clock: 4.040ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

TESTBENCH VHDL MODEL (TVM)

LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

ENTITY UNI_Shift_Register_tb IS

END UNI_Shift_Register_tb;

ARCHITECTURE behavior OF UNI_Shift_Register_tb IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT UNI_Shift_Register

PORT(

rst : IN std_logic;

clk : IN std_logic;

mode : IN std_logic_vector(1 downto 0);

Sin : IN std_logic;

Pin : IN std_logic_vector(3 downto 0);

Sout : OUT std_logic;

Pout : OUT std_logic_vector(3 downto 0)

);

END COMPONENT;


```
--Inputs
signal rst : std_logic := '0';
signal clk : std_logic := '1';
signal mode : std_logic_vector(1 downto 0) := (others => '0');
signal Sin : std_logic := '0';
signal Pin : std_logic_vector(3 downto 0) := "1010";
```

```
--Outputs
signal Sout : std_logic;
signal Pout : std_logic_vector(3 downto 0);
```

```
-- Clock period definitions
constant clk_period : time := 10 ns;
```

```
BEGIN
```

```
-- Instantiate the Unit Under Test (UUT)
 uut: UNI_Shift_Register PORT MAP (
    rst => rst,
    clk => clk,
    mode => mode,
    Sin => Sin,
    Pin => Pin,
    Sout => Sout,
    Pout => Pout
 );
```

```
-- Clock process definitions
clk_process : process
begin

    clk<=NOT(clk);
    wait for clk_period/2 ;
end process;
```

```
-- Stimulus process
stim_proc_mode: process
begin
    mode<="00";
    wait for 80 ns;

    mode<="01";
    wait for 50 ns;

    mode<="10";
    wait for 50 ns;

    mode<="11";
```

```
        wait for 20 ns;  
end process;
```

```
stim_proc_Sin:process  
begin  
wait for 10 ns;
```

```
Sin<='1';  
wait for 10 ns;
```

```
Sin<='0';  
wait for 10 ns;
```

```
Sin<='1';  
wait for 10 ns;
```

```
Sin<='0';  
wait for 10 ns;
```

```
Sin<= '0';  
wait for 40 ns;
```

```
Sin<='1';  
wait for 10 ns;
```

```
Sin<='0';  
wait for 10 ns;
```

```
Sin<='1';  
wait for 10 ns;
```

```
Sin<='0';  
wait for 10 ns;
```

```
Sin<= '0';  
wait ;
```

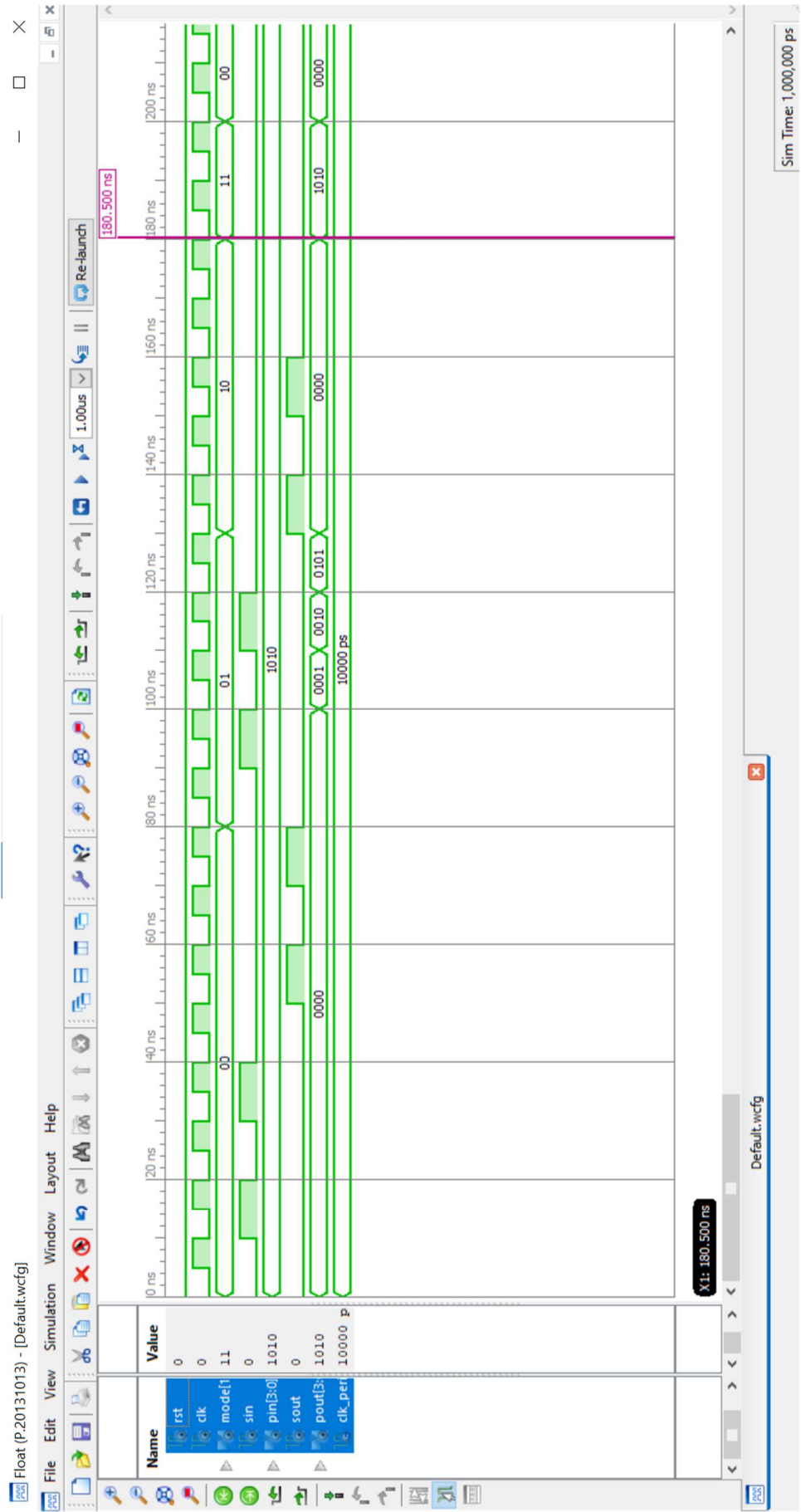
```
end process;
```

```
stim_proc_rst:process  
begin  
rst<='0';  
wait for 300 ns;
```

```
rst<='1';  
wait for 10 ns;  
end process;
```

```
END;
```

ISIM WAVEFORMS



PIN-LOCKING REPORT

PlanAhead Generated physical constraints

NET "clk" LOC = P132;
NET "rst" LOC = P204;
NET "mode[1]" LOC = P205;
NET "mode[0]" LOC = P206;
NET "Sin" LOC = P203;
NET "Pin[3]" LOC = P202;
NET "Pin[2]" LOC = P197;
NET "Pin[1]" LOC = P199;
NET "Pin[0]" LOC = P196;
NET "Sout" LOC = P193;
NET "Pout[3]" LOC = P186;
NET "Pout[2]" LOC = P187;
NET "Pout[1]" LOC = P185;
NET "Pout[0]" LOC = P181;

CONCLUSION

Thus, we have:

- 1) Modeled a Universal Shift Register using Behavioral Modeling Style.
- 2) Observed following Schematics: **RTL & Technology Schematics** generated **Post-Synthesis**.
- 3) Interpreted **Device Utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
- 4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
- 5) Written a TESTBENCH to verify the functionality of Universal Shift Register & verified the functionality as per the FUNCTION-TABLE, by observing ISIM Waveforms.
- 6) Used PlanAhead Editor for pin-locking.
- 7) Prototyped the FPGA **XC3S250EPQ208-5** to realize Universal Shift Register & verified its operation by giving suitable input combinations.