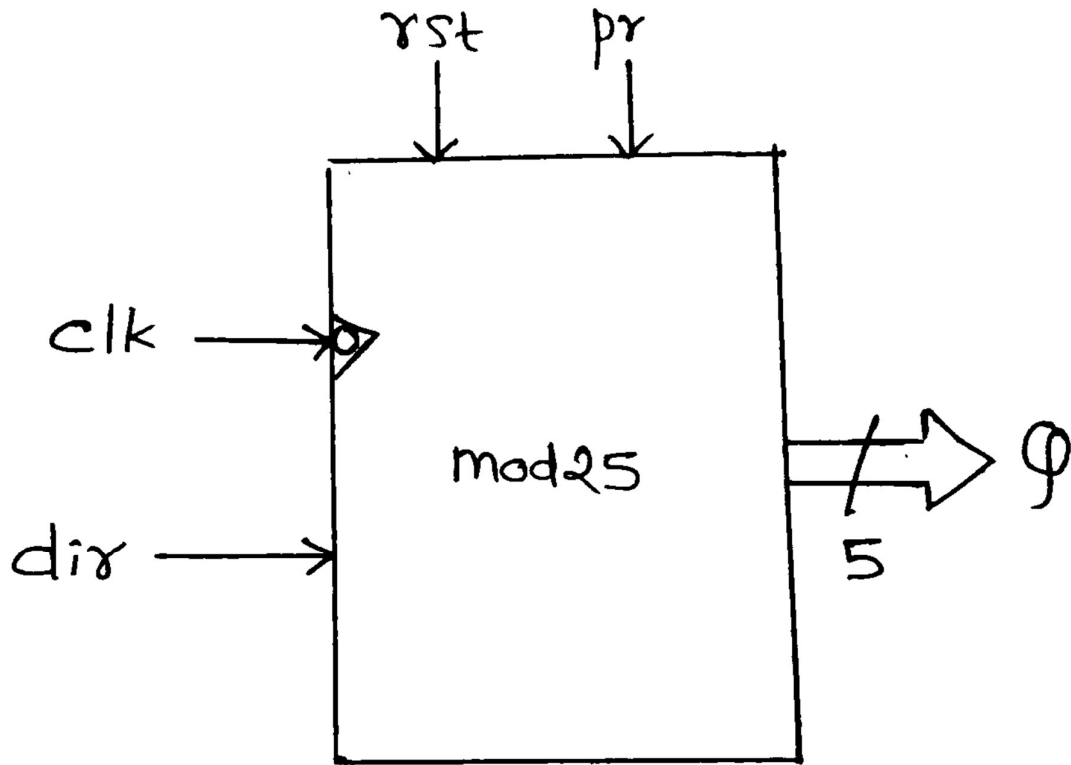


Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	A.4
Assignment Name	:	MOD-N Counter (25 States ,Up-Down Counter with Async-Reset , Preset)
Date Of Performance	:	

BLOCK DIAGRAM



FUNCTION TABLE

rst	pr	clk	dir	Q_{n+1} (Next State)	Operation
1	0	x	x	00000	Reset
0	1	x	x	11111	Set
0	0	↓	1	$Q_n + 1$	$(0)_{10} \rightarrow (24)_{10}$
0	0	↓	0	$Q_n - 1$	$(24)_{10} \rightarrow (0)_{10}$

MAIN VHDL MODEL (MVM)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity mod25 is
    Port ( rst : in STD_LOGIC;
          pr : in STD_LOGIC;
          clk : in STD_LOGIC;
          dir : in STD_LOGIC;
          Q : out STD_LOGIC_VECTOR (4 downto 0));
end mod25;

architecture mod25_arch of mod25 is
    signal Qtemp : STD_LOGIC_VECTOR (4 downto 0) := "00000";

begin
    process(rst,pr,clk,dir)
    begin
        if rst ='1' then
            Qtemp <= (OTHERS =>'0');
        elsif pr='1' then
            Qtemp <= (OTHERS =>'1');
        elsif falling_edge(clk) then
            if dir = '1' then
                if Qtemp < 24 then
                    Qtemp <= Qtemp + 1;
                else
                    Qtemp <= "00000";
                end if;
            else
                if Qtemp > 7 then
                    Qtemp <= Qtemp - 1;
                else
                    Qtemp <= "11111";
                end if;
            end if;
        end if;

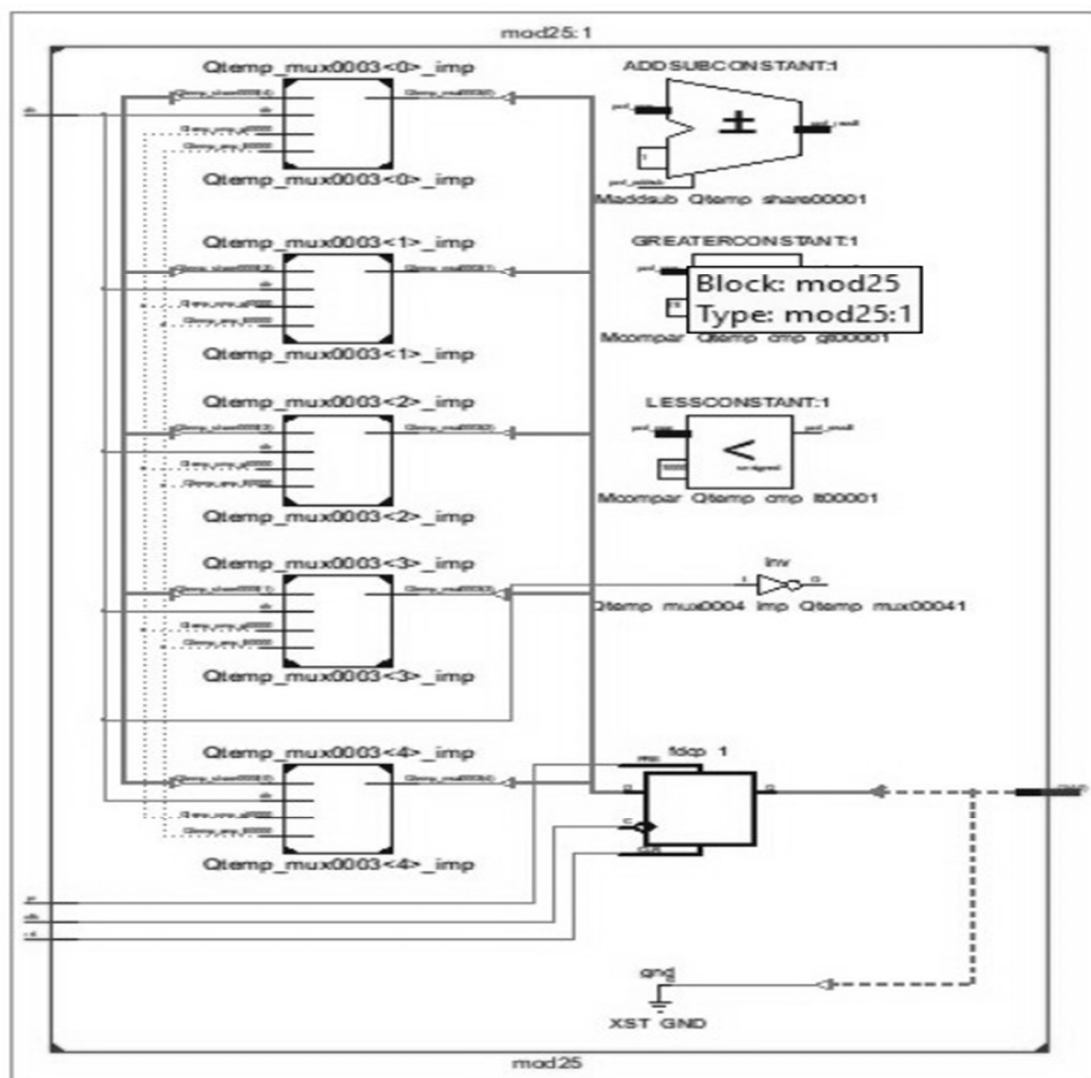
        Q<=Qtemp;
    end process;

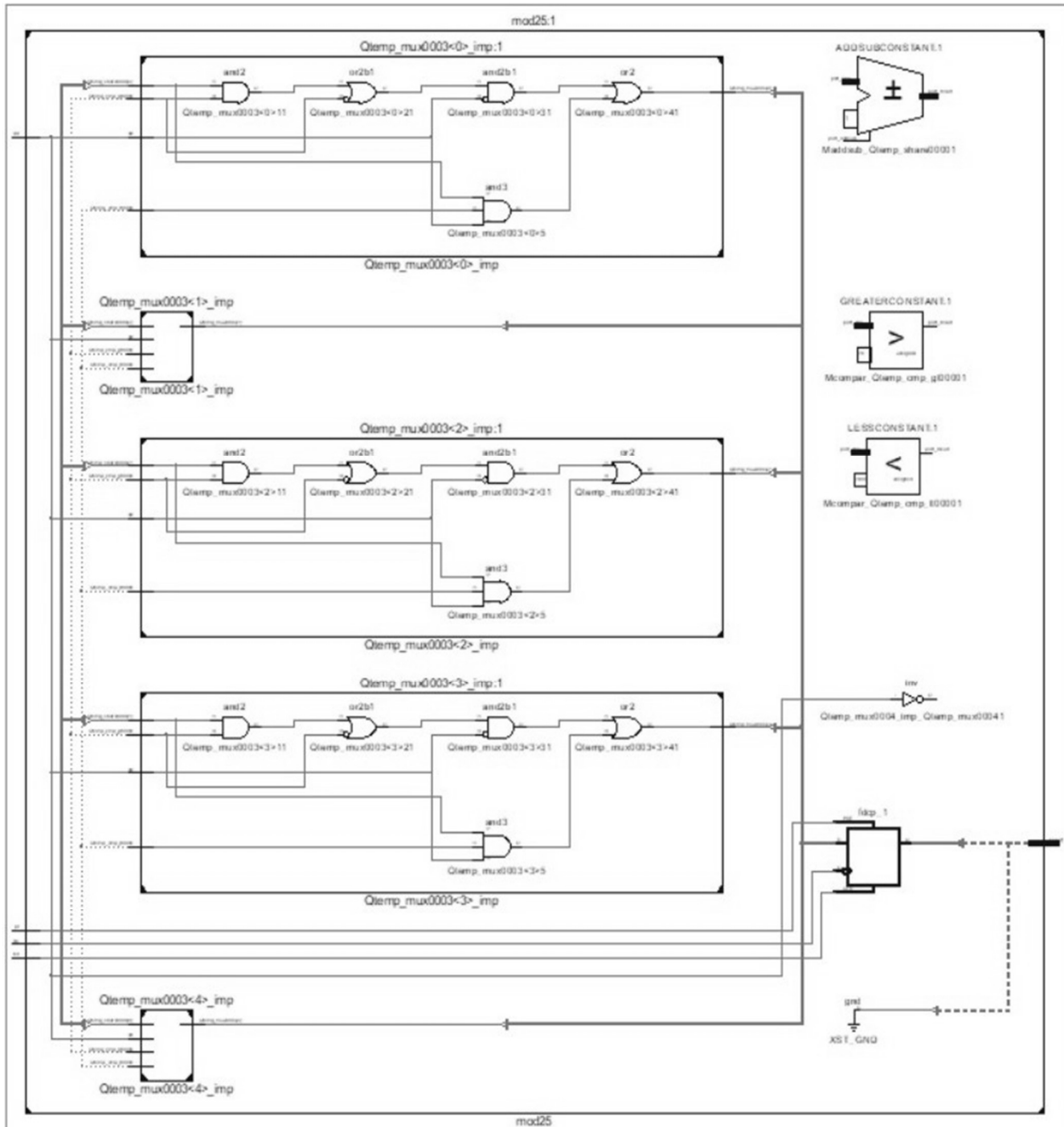
end mod25_arch;
```

```

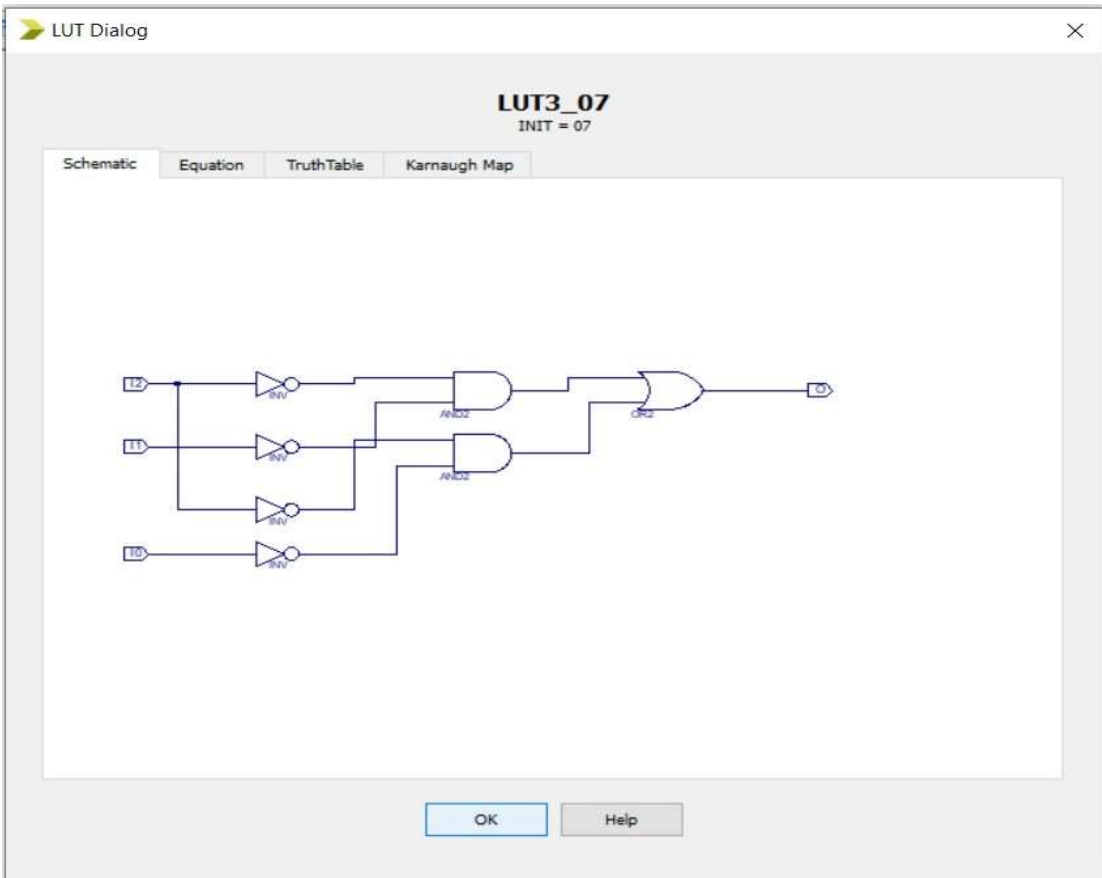
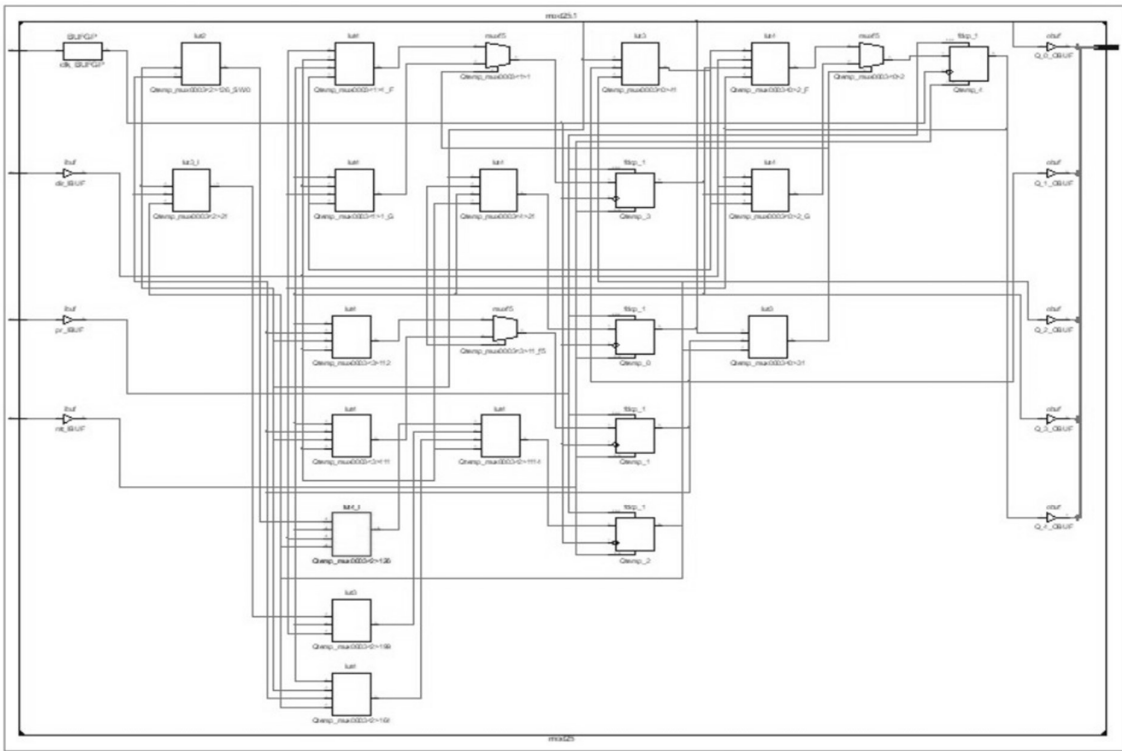
graph LR
    clk[clk] --> mod25
    dir[dir] --> mod25
    pr[pr] --> mod25
    rst[rst] --> mod25
    mod25 --> Q["Q(4:0)"]
    style mod25 fill:#fff,stroke:#000,stroke-width:2px

```





TECHNOLOGY SCHEMATIC



SYNTHESIS REPORT

a) Device Utilization Summary:

```
=====
*                               Final Report                               *
=====
```

Final Results

RTL Top Level Output File Name : mod25.ngr

Top Level Output File Name : mod25

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 9

Cell Usage :

BELS : 18

LUT2 : 1

LUT3 : 3

LUT3_L : 1

LUT4 : 9

LUT4_L : 1

MUXF5 : 3

FlipFlops/Latches : 5

FDCP_1 : 5

Clock Buffers : 1

BUFGP : 1

IO Buffers : 8

IBUF : 3

OBUF : 5

Device utilization summary:

Selected Device : 3s250epq208-5

Number of Slices: 8 out of 2448 0%

Number of Slice Flip Flops: 5 out of 4896 0%

Number of 4 input LUTs: 15 out of 4896 0%

Number of IOs: 9

Number of bonded IOBs: 9 out of 158 5%

Number of GCLKs: 1 out of 24 4%

b) TIMING REPORT:

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Speed Grade: -5

Minimum period: 3.876ns (Maximum Frequency: 257.968MHz)

Minimum input arrival time before clock: 3.059ns

Maximum output required time after clock: 4.476ns

Maximum combinational path delay: No path found

TESTBENCH VHDL MODEL (TVM)

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY mod25_tb IS
END mod25_tb;

ARCHITECTURE behavior OF mod25_tb IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT mod25
    PORT(
        rst : IN  std_logic;
                                pr  : IN  std_logic;
        clk : IN  std_logic;
        dir : IN  std_logic;
        Q : OUT std_logic_vector(4 downto 0)
    );
    END COMPONENT;

    --Inputs
    signal rst : std_logic := '0';
        signal pr : std_logic := '0';
    signal clk : std_logic := '0';
    signal dir : std_logic := '0';

    --Outputs
    signal Q : std_logic_vector(4 downto 0);

    -- Clock period definitions
    constant clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test (UUT)
    uut: mod25 PORT MAP (
        rst => rst,
                                pr  => pr,
        clk => clk,
        dir => dir,
        Q => Q
    );

    -- Clock process definitions
    clk_process : process
    begin
        clk <= '0';
        wait for clk_period/2;
        clk <= '1';
```



```

        wait for clk_period/2;
    end process;

    -- Stimulus process

    stim_proc_dir: process
    begin

        dir <= not(dir);
        wait for 320 ns;

    end process;

    stim_proc_rst: process
    begin
        wait for 680 ns;
        rst <= '1';
        wait for 40 ns;
        rst <= '0';
        wait;

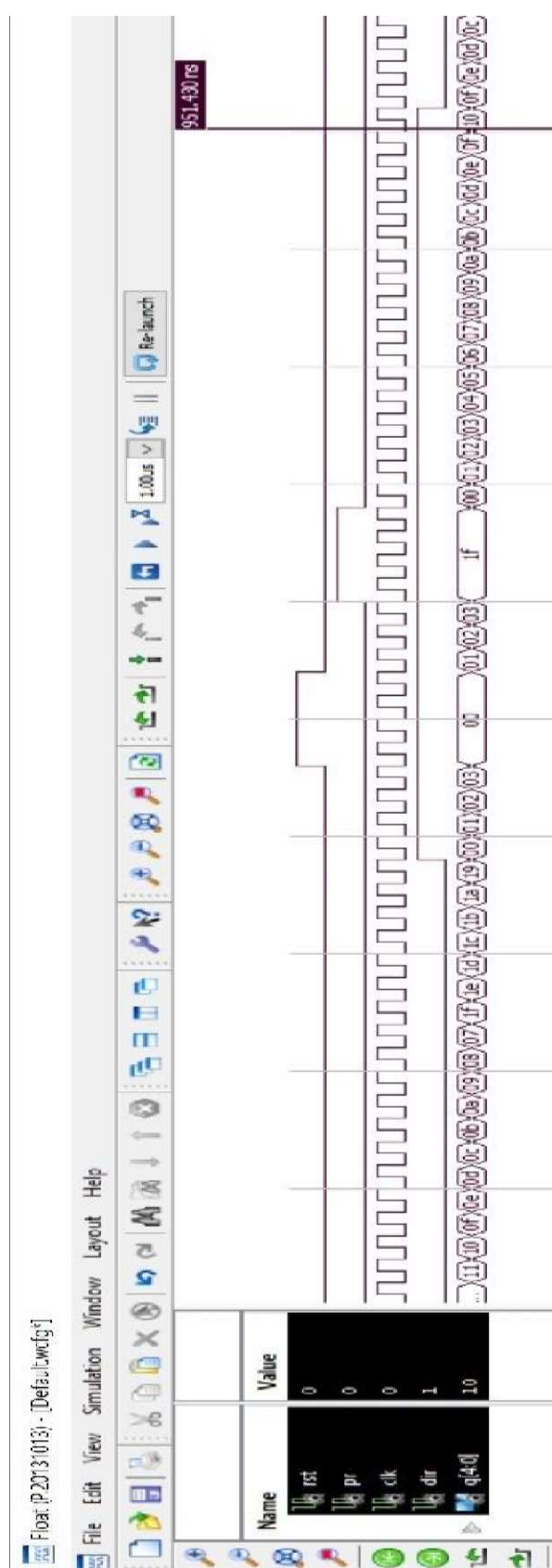
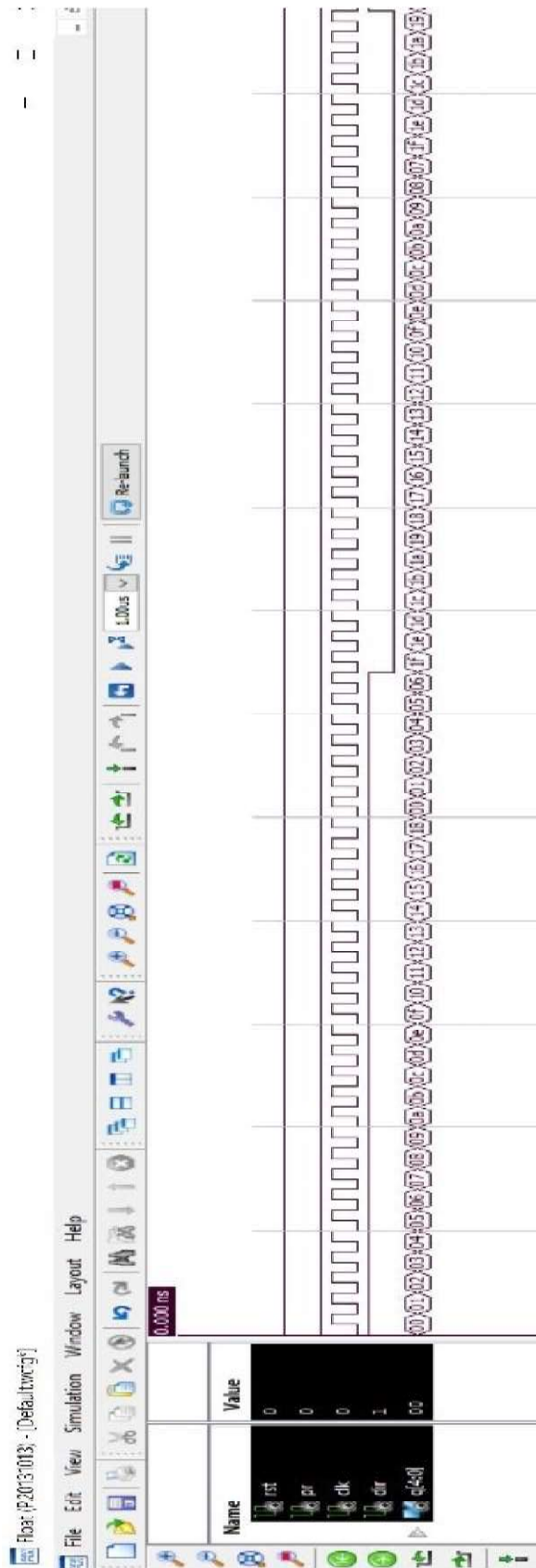
    end process;

    stim_proc_pr: process
    begin
        wait for 750 ns;
        pr <= '1';
        wait for 40 ns;
        pr <= '0';
        wait;

    end process;

END;
```

ISIM WAVEFORMS



PIN-LOCKING REPORT

PlanAhead Generated physical constraints

NET "Q[4]" LOC = P164;
NET "Q[3]" LOC = P162;
NET "Q[2]" LOC = P161;
NET "Q[1]" LOC = P160;
NET "Q[0]" LOC = P153;
NET "clk" LOC = P132;
NET "dir" LOC = P202;
NET "pr" LOC = P204;
NET "rst" LOC = P194;

CONCLUSION

Thus, we have:

- 1) Modeled a MOD-25 UP-DOWN Counter using Behavioral Modeling Style.
- 2) Observed following Schematics: **RTL & Technology Schematics** generated **Post-Synthesis**.
- 3) Interpreted **Device Utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
- 4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
- 5) Written a TESTBENCH to verify the functionality of FPGA-LCD Interfacing & verified the functionality as per the FUNCTION-TABLE, by observing ISIM Waveforms.
- 6) Used PlanAhead Editor for pin-locking.
- 7) Prototyped the FPGA **XC3S250EPQ208-5** to realize FPGA-LCD Interfacing & verified its operation by giving suitable input combinations.