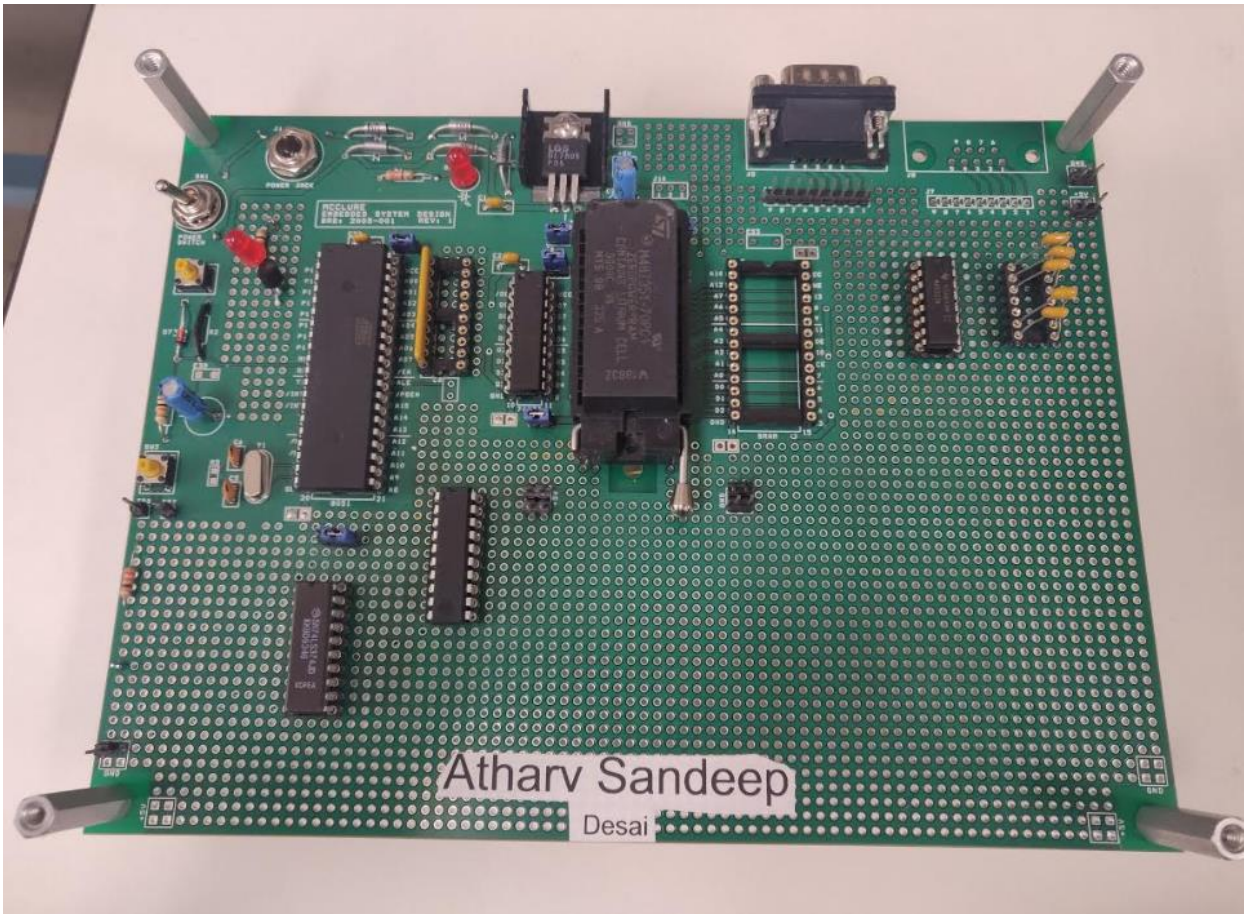
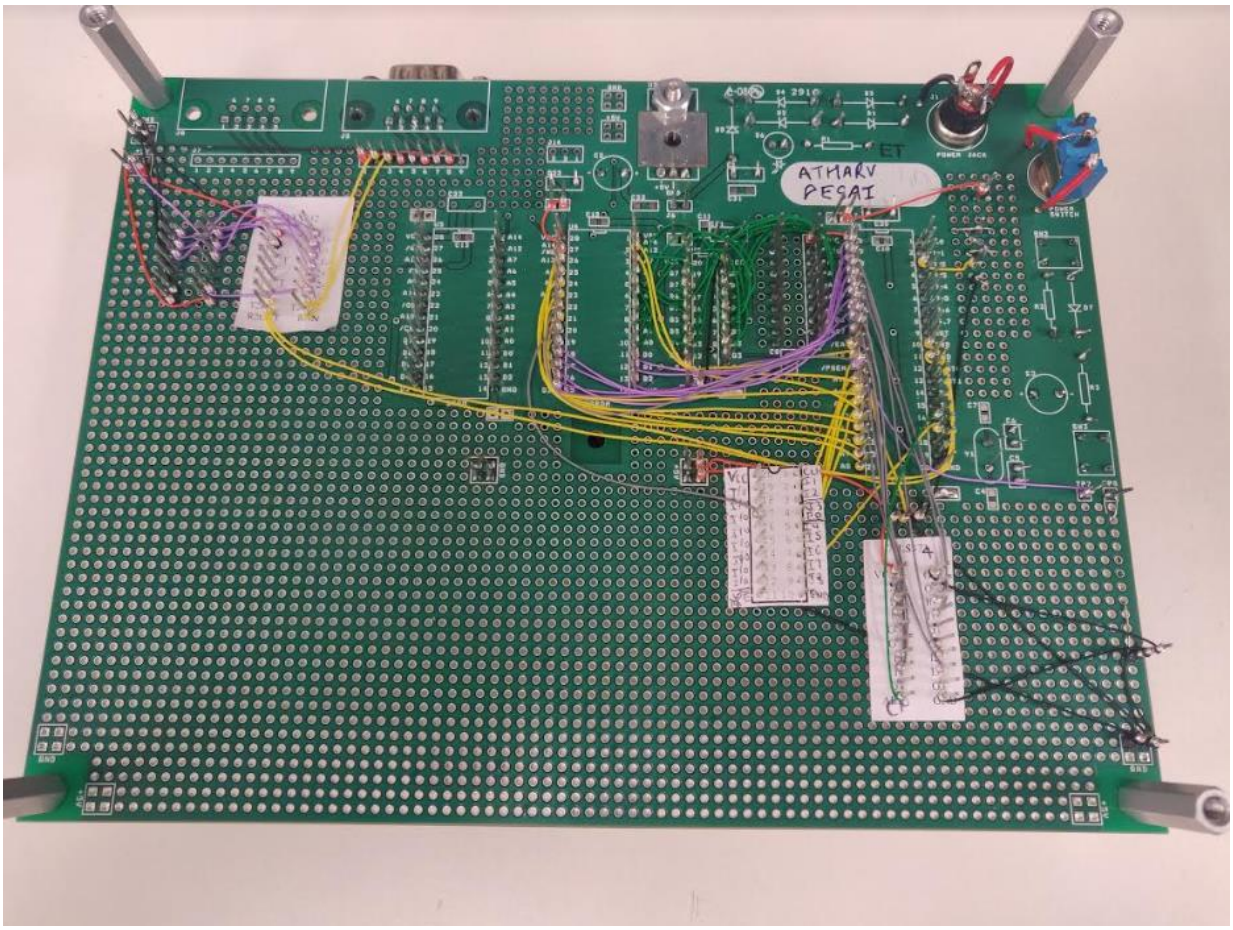
Lab 2 Writeup

Board View

1. Top view

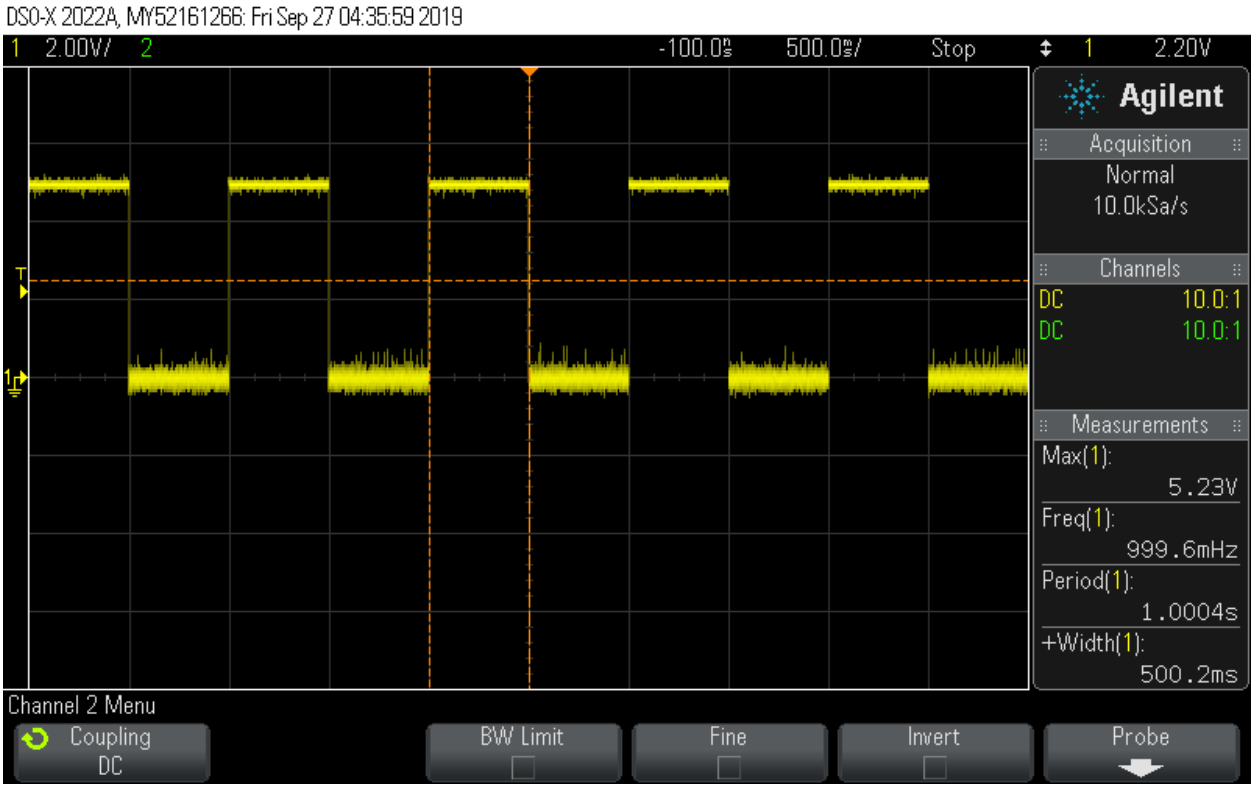


2. Bottom View



Lab 2 Part 1 Screenshots and Description

1. LED toggle at ISR interfaced with 8051:



➔ ISR has been implemented to get the LED toggling at 0.5 Sec.

➔ Since the XTAL Oscillator frequency is 11.0592Mhz and there are 12 Machine Cycles, each instruction takes 1.085 uS to be executed.

➔ Calculation:

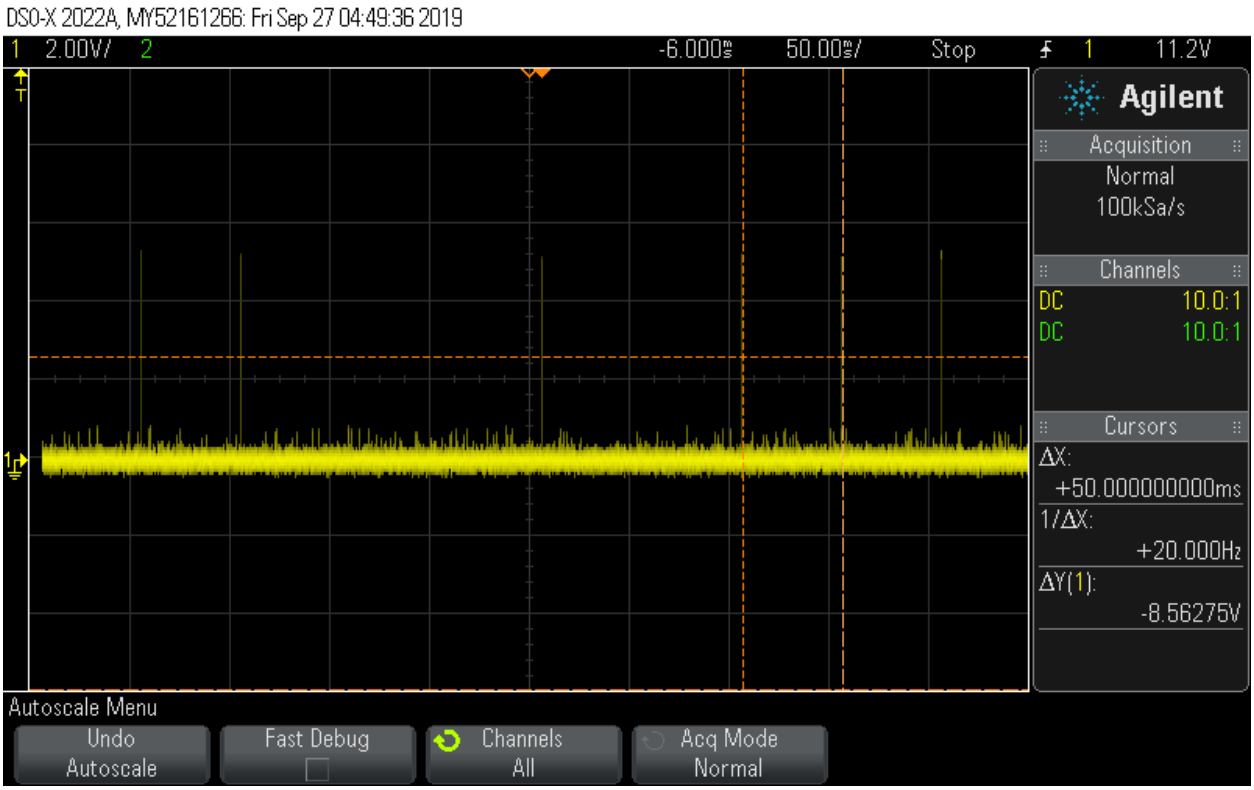
i. Used Timer 0 as an interrupt and loaded the TH0 and TL0 with hex values 4B and FC. Also, Executed the loop 10 times.

ii. This is because, the Timer 0 will count from 19452 (4BFC in hex) till 65535. The difference between them is 46083 (No of ticks to call ISR on Timer Overflow.

iii. Multiplying this value by 10 times since blinking the LED after every 10 times ISR executed: 46083 X 10 = 460830

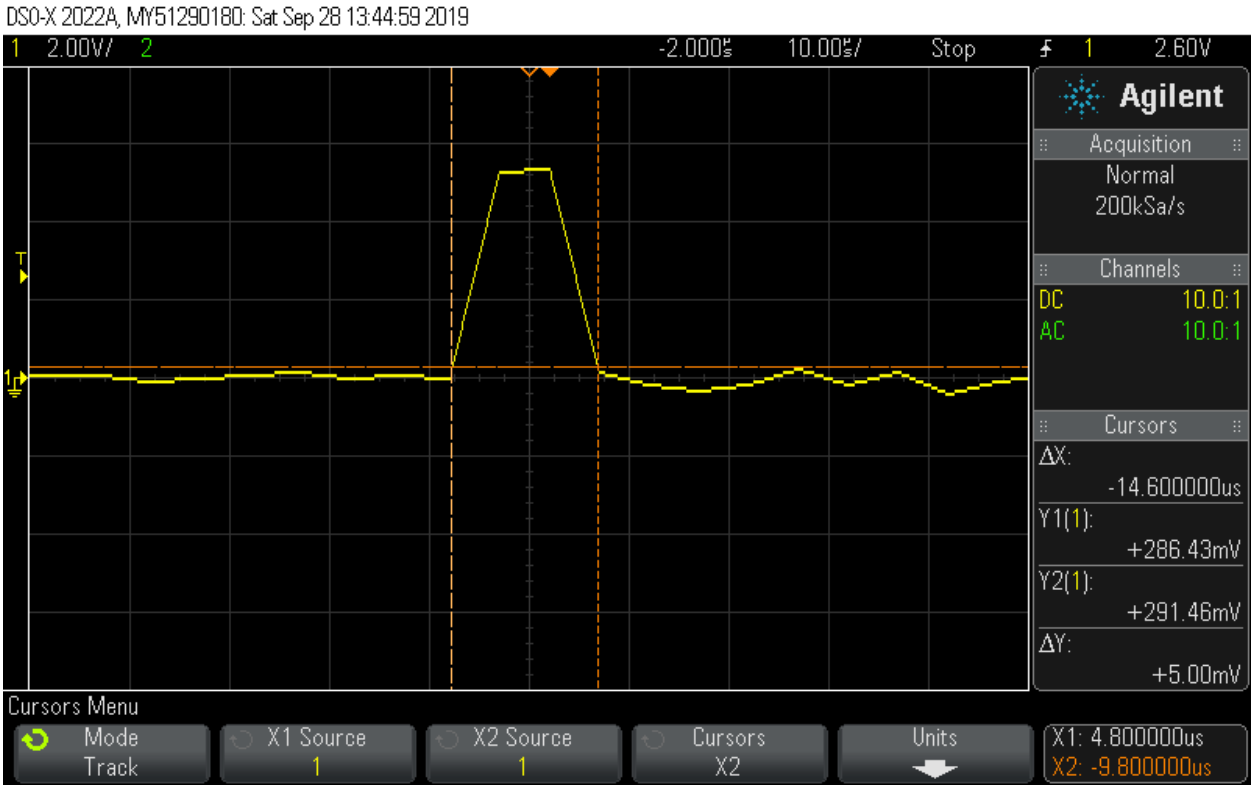
iv. Total time to blink LED:
460830 X 1.085 uSec = 500 mSec

2. Time difference between two ISR calls:



➔ As seen in the X cursor difference in the spikes of P1.1 (P1.1 set very time we enter ISR and set low when we exit) in the screenshot , the time difference is 50 ms which is the difference between 2 ISR.

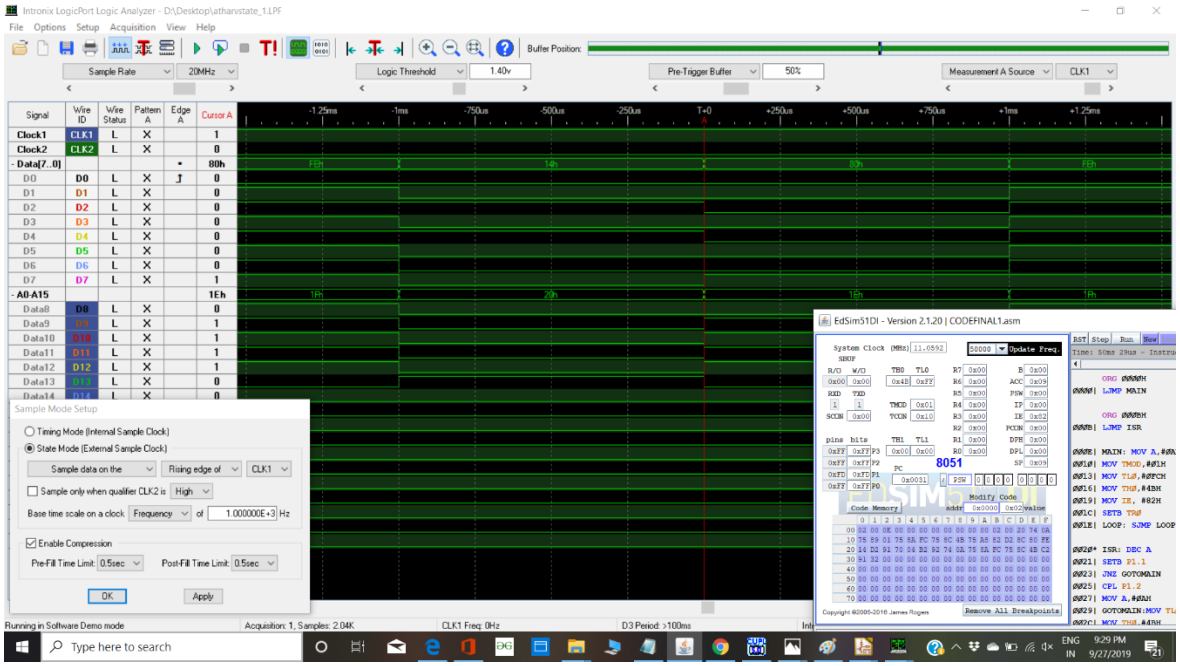
3. ISR Execution time:



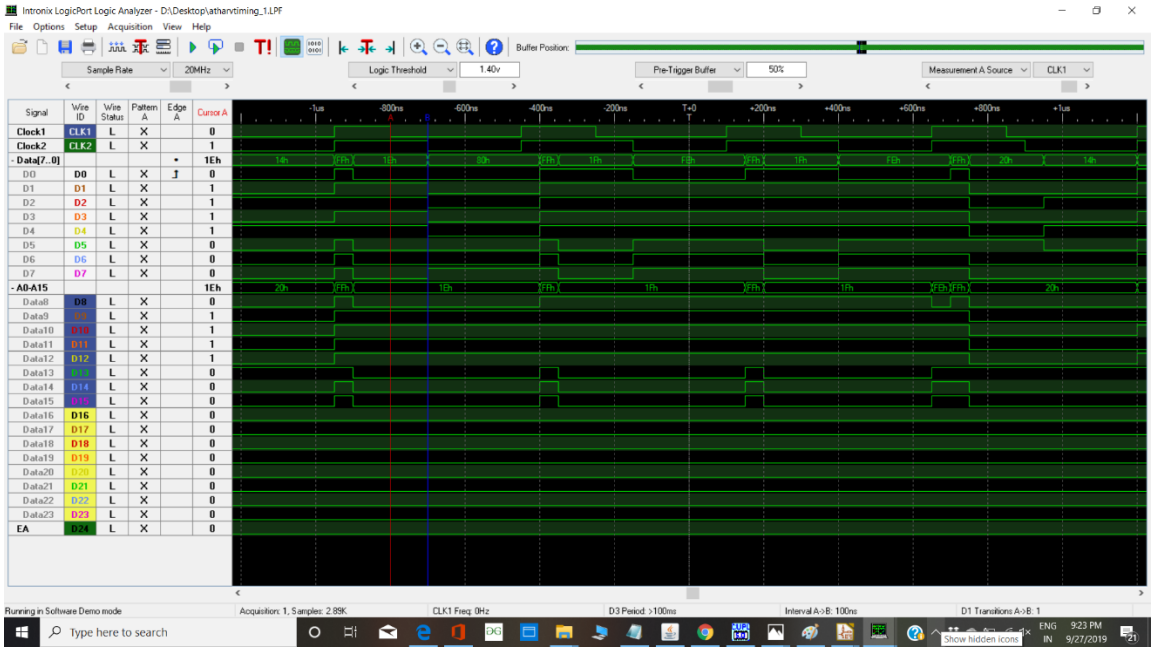
➔ As seen in the screenshot, the X1 X2 cursor difference is 14.6 uSec which is the ISR execution time.

4. Logic Port Analyser

i. Timing Mode Screenshot

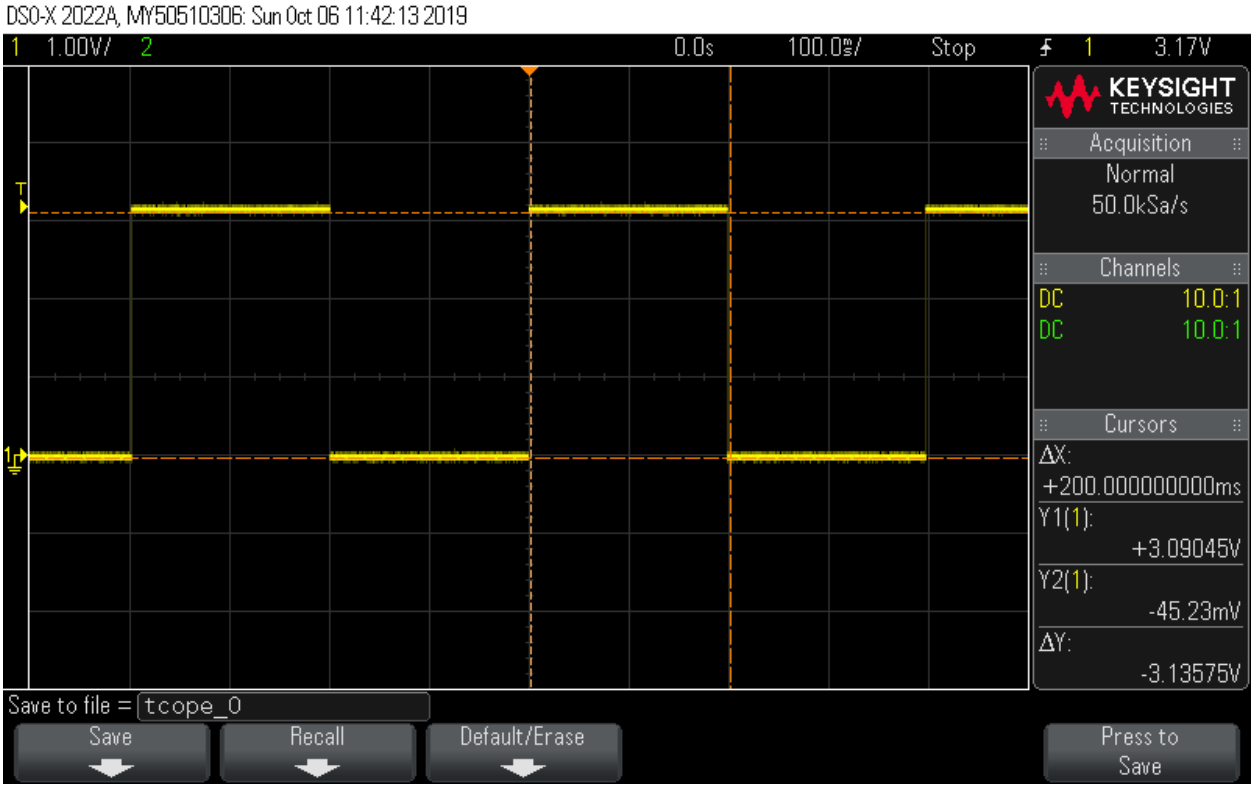


ii. State Mode Screenshot

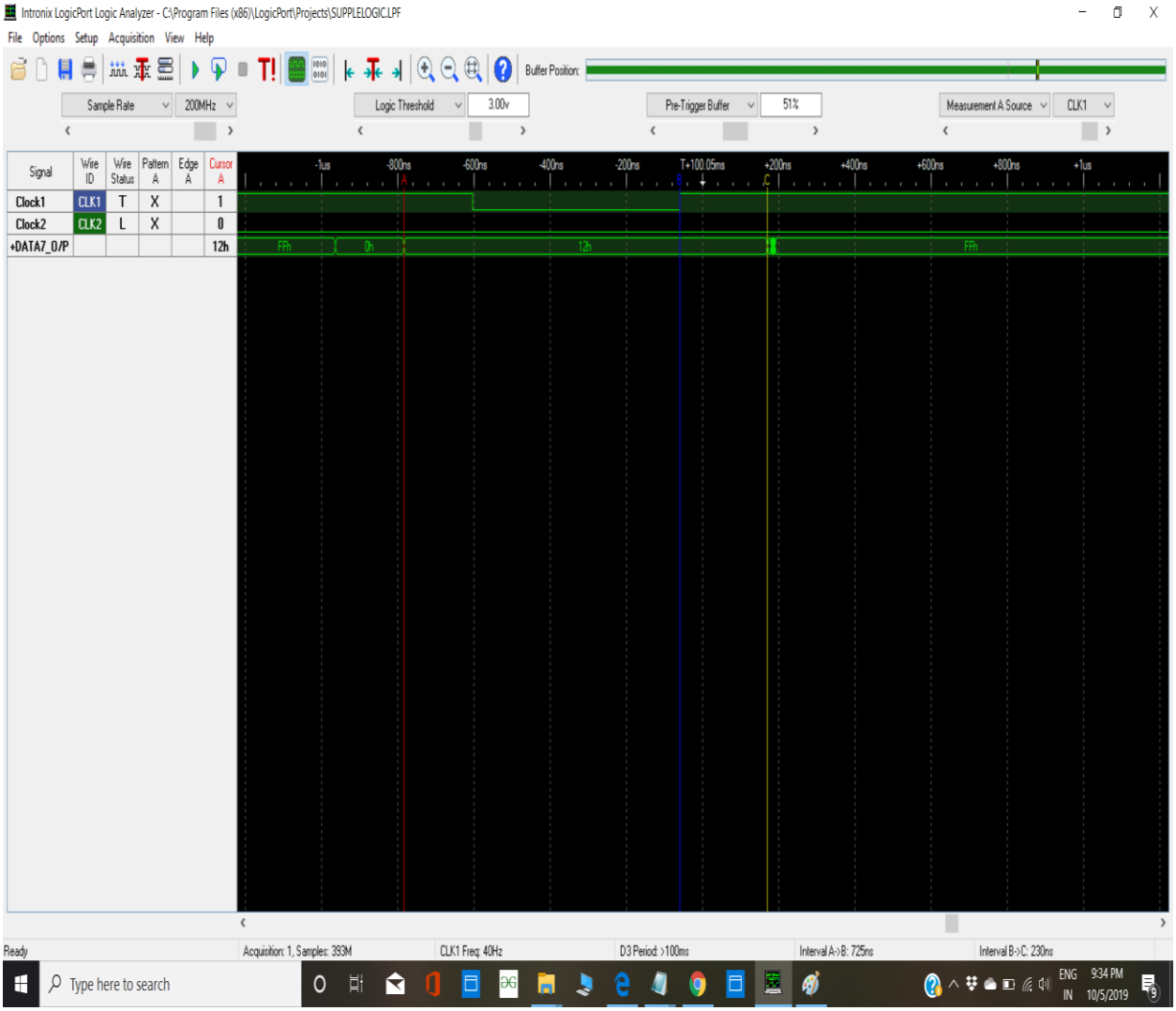


Lab 2 Part 2 Screenshots and Description

1. MSP432 LED Toggle at 200 ms Screenshot



2. 74LS374 Supplementary latch Setup and Hold time



➔ As seen in the screenshot, the setup and hold time for the Write signal has been calculated

➔ The time difference between cursor A->B is setup time which is 725 ns and hold time i.e between B and C cursor is 230 ns

➔ As seen in PDF screenshot below, the setup and hold time is 20 ns and 0 ns respectively

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency				35	50		MHz	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	
t_{PLH} t_{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C_L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t_W	Clock Pulse Width	15		15		ns
t_S	Setup Time	5.0		20		ns
t_h	Hold Time	20		0		ns

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

LAB Outcome:

Thus, Lab 2 acquainted me with the following Concepts, Hardware and Software

- ➔ NVRAM, 74LS374 interfacing with 80521
- ➔ Logic Port Analyser
- ➔ MSP432 architecture
- ➔ Code Composer Studio
- ➔ Functioning of ISR
- ➔ Flip Programming