FMEA

Process/Product Name: UART Communications with PC

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Reference: goleansixsigma.com

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Process Feature	Potential Failure Mode	Potential Failure Effects	SEVERITY (1 - 10)	Potential Causes	OCCURRENCE (1 - 10)	Current Controls	DETECTION (1 - 10)	RPN							
Description about process step, change or feature under investigation	Poterntial modes where features coulo wrong	Impact on the customer if this failure is not prevented or corrected		Potential reasons for which the feature or process could go wrong		Actions or controls to be taken to avoid the potential failure									
Data Loading in Circular Buffer	*Buffer Full and Overwrite Starts*	*Important Data can be lost due to overwrite*	*8*	*Insufficient Circular Buffer size allocation*	*4*	*Reallocate Larger buffer size for data accommodation*	*4*	*128*							
KL25Z Firmware Updation	*Hard Bricking of KL25Z board*	*Firmware Corruption & Board Functionality Halts*	*10*	*Interruption while Firmware Updation, Malware*	*3*	*Using Debug Board to access memory, User Created Modifier Programs*	*4*	*120*							
UART communication in data receiver mode	*UART Receiver Buffer Data Loss*	*UART Communication becomes unreliable to handle real time critical data*	*3*	*Data Overwrite takes place as soon as new data loaded in receiver buffer.*	*6*	*Using Polling or Interrupt to check if Rx Data present in Rx buffer before new data overwritten*	*5*	*90*							
Circular Buffer Memory Allocation in heap segment	*Circular Buffer initialization fails due to heap overflow.*	*Buffer allocation failure causes problem to store and transmit UART data*	*4*	*Memory Leakage , large memory block dynamic allocation*	*6*	*Free the allocated memory after use. Also, Reallocate new memory with small increments to avoid memory wastage*	*6*	*144*							
UART Baud Rate Configuration	*Baud Rate mismatch betwwen KL25Z and PC*	*Echoed Data printed as garbage on serial terminal*	*4*	*Improper BDL,BDH values or selection of inaccurate prescalar.*	*6*	*Select correct clock source and compute SBR value to calculate accurate prescalar*	*4*	*96*							
Data Send and receive operation using Polling	*In Polling Uart mode, Data checked in register according to configured clock*	*Processing overhead increased in polling and data loss probability high at low clock speeds*	*3*	*Though Polling Mechanism makes it easier to implement, but its inefficient to check register status.*	*7*	*Using UART interrupt mode optimizes resource use since when the data comes in the Rx register, only then the data is read from RX buffer*	*4*	*84*							