T Y B Tech – Department of Computer Engineering

ODD SEMSTER (SEM- V)

Course: Processor Organization and Architecture **Course Code: PCCO5020T**

Term Test – I

Unit- 2-8 Hrs

15 Marks

Que No.	Questions (Statement)	Questions	CO	Blooms Level	PI
1	Explain different types of RAM	5	CO2	L2	1.4.1
2	Illustrate the concept of Interleaved memory with example	5	CO2	L3	1.4.1
3	Compare SRAM and DRAM	5	CO2	L3	2.2.5
4	Explain Cache Coherence and list different Cache Coherence protocols	5	CO2	L2	1.4.1
5	Illustrate Cache Mapping techniques with neat Sketch.	10	CO2	L4	1.4.1
6	Outline the concept Memory Hierarchy and its characteristics	10	CO2	L4	2.2.2
7	Explain Rom and its Types	10	CO2	L2	2.2.2
8	Apply FIFO and LRU page replacement policy for the following reference string and list the page faults occurred. Consider frame size as 3 Reference string = 7,0,1,2,0,3,0,4,2,3,0,3,2.	10	CO2	L3	2.2.3

Subject Teachers **Module Coordinator** **Program Coordinator** **HOD**