

# Lab Report: 8

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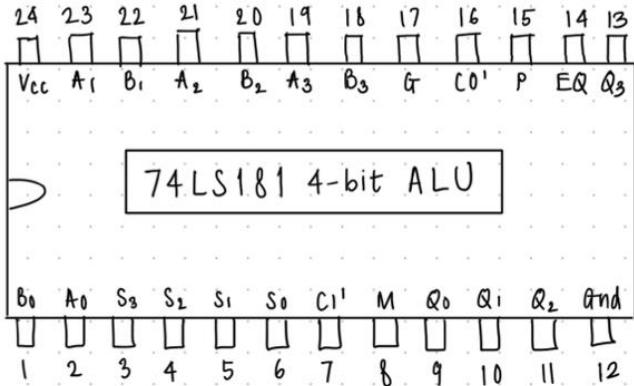
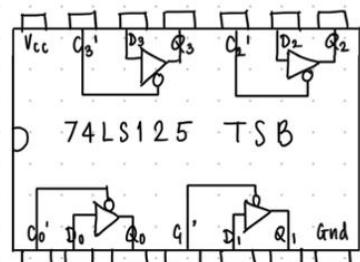
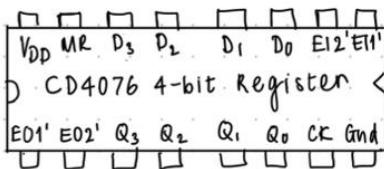
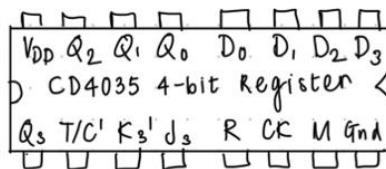
## Experiment 8: Bus-based ALU-Register Data Transaction

**Aim/Objective:** To build and study data transactions through a BUS-based system using a 74LS181 ALU, two Registers (CD4035 and CD4076), and a Tri-State Buffer (74LS125).

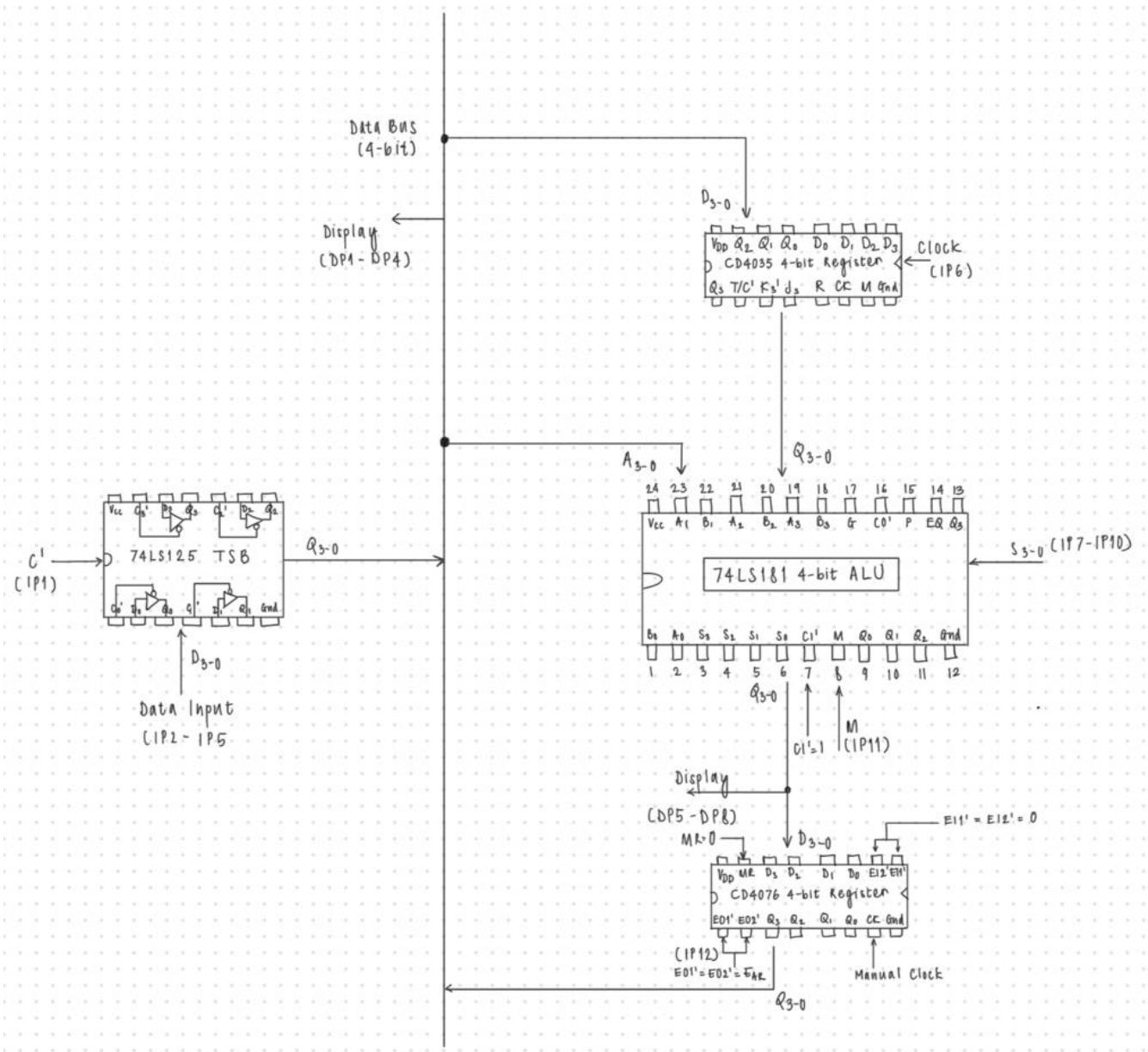
### Electronic Components Used:

1. 4-bit Arithmetic Logic Unit (74LS181)
2. Operand Register (CD4035)
3. Accumulator Register (CD4076)
4. Tri-State Buffer (74LS125)
5. Breadboard
6. Switches (Input Pins)
7. LEDs (Display Pins)
8. Power Supply

### Pin diagrams of the ICs used



## Reference Circuit



Programmable ALU with Registers on a Bus.

## **Connections to be made:**

### **1. Connections for Tri-State Buffer (74LS125):**

- Connect all C0, C1, C2, C3 to Input Pin 1.
- Connect D3, D2, D1, D0 to Input Pins 2, 3, 4, 5 respectively.
- Connect Q0, Q1, Q2, and Q3 to the lines above and below on the breadboard.
- Connect Q0, Q1, Q2, and Q3 to the Display Pins 1, 2, 3, 4 through data lines.

### **2. Connections for Operand Register (CD4035):**

- Connect M and T/C' to VCC.
- Connect R to Ground.
- Connect CK to Input Pin 6 (which will be used as a clock).
- Keep J3 and K3' open.
- Connect Q0, Q1, Q2, Q3 on Operand Register (CD4035) to B0, B1, B2, B3 on Arithmetic Logic Unit.
- Connect D0, D1, D2, D3 on Operand Register (CD4035) to Q0, Q1, Q2, Q3 on Tri-State Buffer using data lines.

### **3. Connections for 4-bit Arithmetic Logic Unit (74LS181):**

- Connect A0, A1, A2, A3 on Arithmetic Logic Unit (74LS181) to Q0, Q1, Q2, Q3 on Tri-State Buffer using data lines.
- Connect CI' to VCC.
- Connect S0, S1, S2, S3 to Input Pins 7, 8, 9, 10, respectively.
- Connect M to Input Pin 11.
- Connect Q0, Q1, Q2, Q3 Display Pins 8, 7, 6, 5.
- Connect Q0, Q1, Q2, Q3 to D0, D1, D2, D3 on Accumulator Register (CD4076).

### **4. Connections for Accumulator Register (CD4076):**

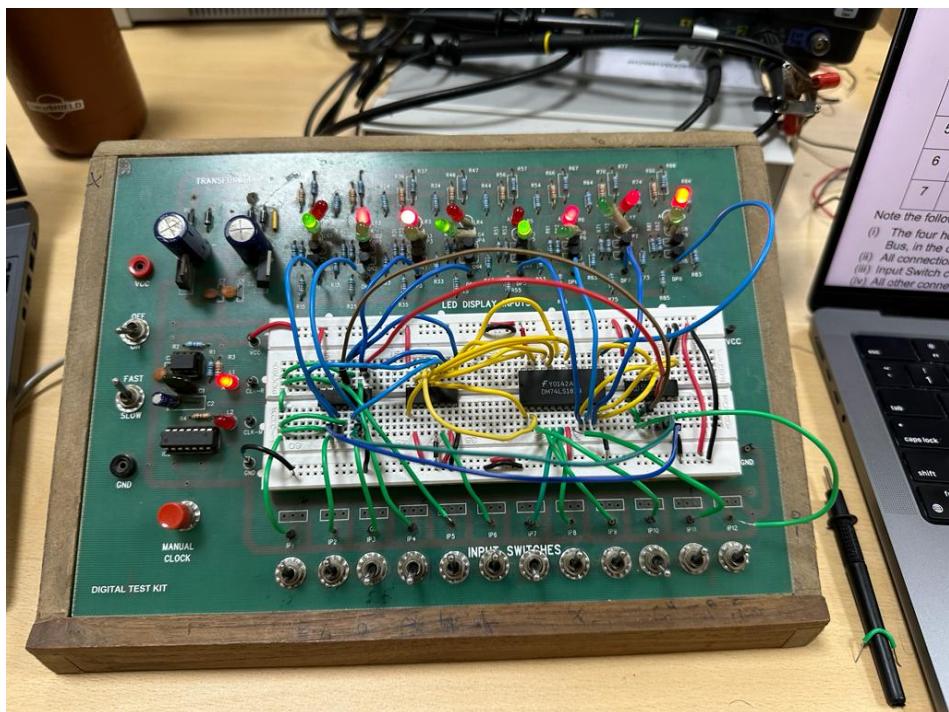
- Connect EI1', EI2', MR to Ground.
- Connect CK to Manual Clock.
- Connect both EO1' and EO2' together. It is named EA and connect it to Input Pin 12.
- Connect Q0, Q1, Q2, and Q3 to the data lines.

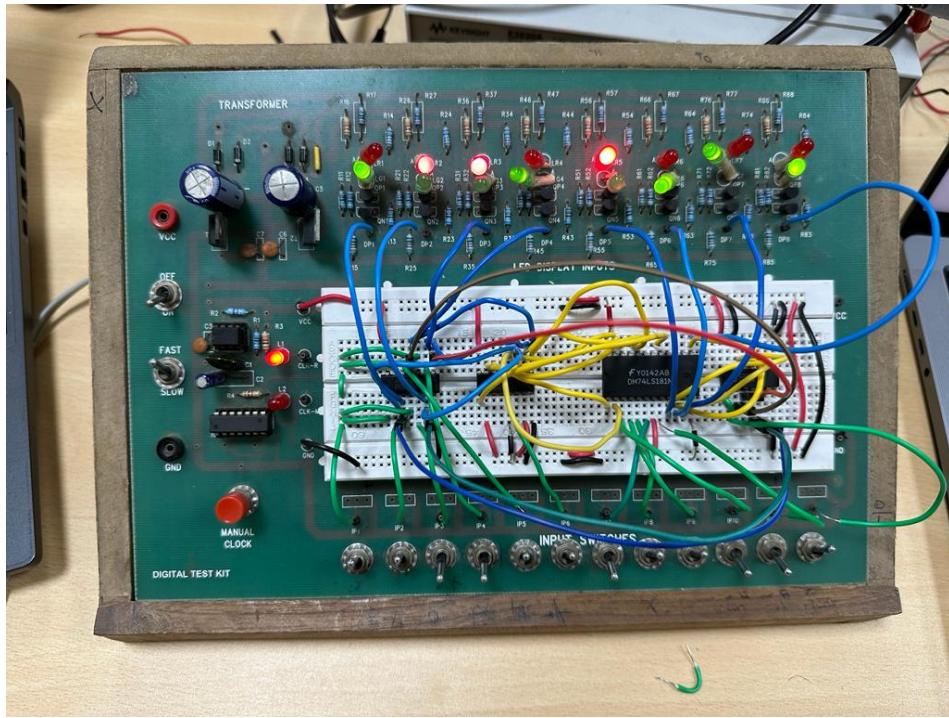
## **Procedure**

1. Power the breadboard using Ground and VCC.
2. Make the circuit connections described above.
3. Verify that when C' = 1, all the LEDs in DP1–DP4 are off, indicating the bus is "floating."

4. Avoid BUS CONFLICT while making the connections.
5. Ensure that C' (IP1) and EAR' (IP12) are not both LOW before turning the power back on.

## Images





## Observation:

When the Tri-State Buffer (TSB) is enabled by setting the control input (C') to LOW, and 4-bit data input is applied through Input Pins (IP2-IP5), the TSB loads this data into the ALU. Once this data is transferred to the ALU, depending on the selected function as specified by the control inputs (S3-0 and M), the ALU can perform the selected logical and arithmetic operations on the input data. The result is displayed in the output displayed on LEDs (DP5-DP8), showing the outcome of the ALU operation as per the observation table.

<b>S<sub>3-0</sub></b>	<b>M=HIGH (Logic)</b>	<b>M=LOW (Arithmetic)</b>	<b>S<sub>3-0</sub></b>	<b>M=HIGH (Logic)</b>	<b>M=LOW (Arithmetic)</b>
0	A'	A PLUS CI	8	A'+B	A PLUS (A•B) PLUS CI
1	(A+B)'	(A+B) PLUS CI	9	(A⊕B)'	A PLUS B PLUS CI
2	A'•B	(A+B') PLUS CI	10	B	(A+B') PLUS (A•B) PLUS CI
3	0000	Zero MINUS CI'	11	A•B	(A•B) MINUS CI'
4	(A•B)'	A PLUS (A•B') PLUS CI	12	1111	A PLUS A PLUS CI
5	B'	(A+B) PLUS (A•B') PLUS CI	13	A+B'	(A+B) PLUS A PLUS CI
6	A⊕B	A MINUS B MINUS CI'	14	A+B	(A+B') PLUS A PLUS CYI
7	A•B'	(A•B') MINUS CI'	15	A	A MINUS CI'

## Conclusion

In this experiment, we successfully implemented a bus-based digital system using components like a 4-bit Arithmetic Logic Unit, Operand Register, Accumulator Register, and a Tri-State Buffer. Using tristate buffers, we were able to successfully move data (the output of one register) from one register to another through the bus. The ALU operations were conducted and the results confirmed that the components could perform the required arithmetic and logic functions accurately.