Designing a JK flip-flop and determining its delay, power and area

A PROJECT

Submitted in fulfillment of the requirements for the practical coursework

of

Master of Technology

VLSI Design and Nanoelectronics (VDN)

by

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DISCIPLINE OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY INDORE

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INDIAN INSTITUTE OF TECHNOLOGY INDORE

We hereby certify that the work which is being presented in the report entitled **Determining results of 1-bit JK flip-flop using Cadence Virtuoso** submitted for requirements of the practical coursework of **M Tech (VDN)** and submitted in the Discipline of Electrical Engineering**, Indian Institute of Technology Indore**, is an authentic record of our own work carried out during the time period from July 2023 to Nov 2023 under the supervision of **Prof. Santosh Kumar Vishvakarma**. The matter presented in this report has been cited properly wherever necessary.

(Atharv Limaye)

This is to certify that the above statement made by the candidates is correct to the best of my knowledge.

(Prof. Santosh Kumar Vishvakarma)

ACKNOWLEDGEMENTS

First of all, We would like to thank our Supervisor Prof. Santosh Kumar Vishvakarma whose constant motivation, guidance and suggestion helped us to accomplish the task. We would also like to thank him for providing us Cadence software resources associated with Nanoscale Devices, VLSI Circuit and System Design (NSDCS) Lab. We would like to Thank NSDCS PhD Scholar Mr. Shashank, Mr Vikash and Mr Narendra sir for their constant guidance and support and fellow project members along with MTech VDN students for motivation towards achieving the task.

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1. SYNOPSIS

A JK flip-flop, a fundamental building block in digital electronics, represents a bistable multivibrator capable of storing a single bit of information. The nomenclature "JK" is derived from its two principal inputs, J (set) and K (reset). This digital circuit, an enhancement over the SR (Set-Reset) flip-flop, serves a pivotal role in memory storage within digital systems, offering a versatile and essential component for sequential logic operations.

At its core, the JK flip-flop exhibits three primary states: Set, Reset, and the hold state. The set state is characterized by a logic 1 at the J input and a logic 0 at the K input, compelling the flip-flop to establish a state where the Q output is set to logic 1. Conversely, the reset state, prompted by a logic 0 at the J input and a logic 1 at the K input, results in the Q output being forced to logic 0.
The distinctive feature of the JK flip-flop is its ability to toggle between states. In the toggle state, achieved by setting both J and K inputs to logic 1 and applying a clock pulse, the flip-flop undergoes a transition—changing from the set state to the reset state or vice versa. This capacity for toggling provides a dynamic element to the JK flip-flop, enabling it to adapt to changing inputs and serve various functions in digital systems.

Furthermore, the JK flip-flop can remain in a hold state when both J and K inputs are set to logic 0. In this state, the flip-flop retains its current configuration, maintaining stability until new inputs are applied. The synchronous nature of the JK flip-flop, where changes in the J and K inputs only affect the output during a clock pulse, ensures predictable and reliable operation within the context of a digital system.
The inclusion of a clock input (often denoted as CLK or CP) is pivotal in governing the timing of state transitions. The presence of a clock pulse synchronizes the changes in the J and K inputs, preventing erratic behavior and contributing to the systematic functionality of the flip-flop.

JK flip-flops play a crucial role in digital circuitry, finding applications in various domains. One notable application is in memory cells, where the bistable nature of the flip-flop allows for the storage of binary information. Additionally, JK flip-flops are integral components in frequency dividers, where they aid in dividing the frequency of a clock signal. Their versatility extends to serving as fundamental building blocks for more complex sequential circuits, contributing to the design and implementation of sophisticated digital systems.

The widespread use of JK flip-flops underscores their significance in digital design. Their ability to toggle between states, coupled with the synchronous control provided by the clock input, makes them invaluable for realizing sequential logic operations. Designers leverage the JK flip-flop to create circuits that exhibit

memory, produce frequency-divided signals, and facilitate intricate digital processes.
In conclusion, the JK flip-flop stands as a cornerstone in digital electronics, embodying the principles of bistable multivibrators and offering a robust mechanism for storing binary information. Its distinctive set, reset, toggle, and hold states, coupled with the influence of the clock input, render it an indispensable component in the construction of digital systems. The ongoing evolution of digital technology ensures the continued relevance and application of JK flip-flops in diverse and complex electronic designs.

A JK flip-flop is a type of digital electronic circuit that serves as a basic memory element in digital systems. It belongs to the family of flip-flops, which are bistable multivibrators capable of storing one bit of information. The JK flip-flop is an improvement over the simpler SR (Set-Reset) flip-flop, addressing some of its limitations.

The name "JK flip-flop" is derived from its two inputs: J (set) and K (reset). These inputs, along with a clock input (usually denoted as CLK or CP), enable the JK flip-flop to transition between two states: SET, RESET, and the hold state.

The fundamental operation of a JK flip-flop is as follows:

1. **Set State (J=1, K=0)**: When the J input is set to 1 and the K input is set to 0, the flip-flop enters the SET state. This means that the Q output is forced to logic 1.

2. **Reset State (J=0, K=1)**: Conversely, when the J input is set to 0 and the K input is set to 1, the flip-flop enters the RESET state. This forces the Q output to logic 0.

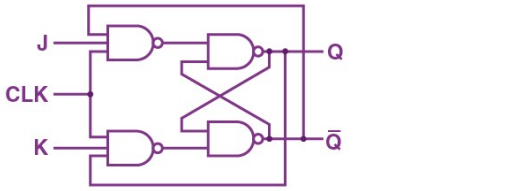
3. **Toggle State (J=1, K=1)**: The unique feature of the JK flip-flop is its ability to toggle between states. When both J and K inputs are set to 1 and a clock pulse is applied, the flip-flop toggles its state. If it was in the SET state, it transitions to RESET, and vice versa.

4. **Hold State (J=0, K=0)**: If both J and K inputs are set to 0, the flip-flop remains in its current state, effectively holding its output.

The clock input is crucial in controlling the timing of state transitions. The flip-flop responds to changes in the J and K inputs only when a clock pulse occurs. This synchronous behavior ensures stable and

predictable operation within a digital system.

JK flip-flops find widespread use in digital circuits, such as memory cells, frequency dividers, and as building blocks for more complex sequential circuits. Their versatility and ability to toggle between states make them valuable components in digital design.



Truth Table

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table1: JK flip-flop truth table

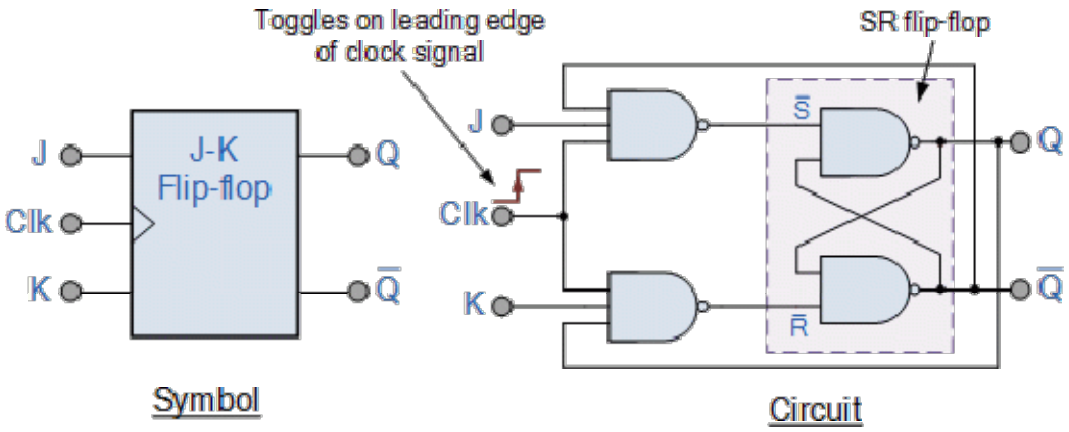


Fig1: JK Latch circuit and symbol

2. INTRODUCTION

A JK flip-flop is a type of digital circuit that serves as a memory element in digital systems. It's a bistable multivibrator, meaning it has two stable states. The theory and working principle of a JK flip-flop can be explained as follows:

1. Theory:

The JK flip-flop is an extension of the simpler SR (Set-Reset) flip-flop. The J and K inputs of a JK flip-flop stand for "Jump" and "Kill," respectively, which are used to set or reset the flip-flop. The key advantage of a JK flip-flop over an SR flip-flop is that it eliminates the invalid state where both the S and R inputs are high.

2. Working Principle:

A JK flip-flop has two inputs, J (set) and K (reset), along with a clock input (usually denoted as CLK or CP) and two outputs, Q and Q' (complement of Q).

The flip-flop changes its state (Q and Q' outputs) based on the inputs (J and K) and the clock signal. The clock signal is used to control when the inputs are considered for a state change.

The following are the fundamental operating rules of a JK flip-flop:

- If J and K are both low, the flip-flop maintains its current state.
- If J is high and K is low when the clock signal transitions (e.g., from low to high), the flip-flop sets (Q becomes high).
- If K is high and J is low when the clock signal transitions, the flip-flop resets (Q becomes low).
- If both J and K are high when the clock transitions, the flip-flop toggles: if Q is high, it becomes low, and if Q is low, it becomes high.

The behavior of a JK flip-flop can be summarized using a truth table:

J	K	CLK	Q	Q’
0	0	↑	Q	Q’
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	~Q	~Q’ (toggle)

Table2: Working of JK flip-flop on positive edge

Here, ↑ indicates the rising edge of the clock signal, and ~Q represents the complement of Q.

The JK flip-flop is a versatile component widely used in digital circuits and sequential logic systems due to its ability to toggle states and avoid the invalid state found in the SR flip-flop.

3. THEORY AND WORKING PRINCIPLE

The behavior of a JK flip-flop can be expressed using the following equations:

1. Next State Equations:

- $Q_{next} = J \cdot Q' + K' \cdot Q$
- $Q_{next}' = J' \cdot Q + K \cdot Q'$

Where:

- Q_{next} is the next state of the Q output.
- Q_{next}' is the next state of the complement of Q output.
- Q is the current state of the Q output.
- Q' is the complement of the current state of the Q output.

2. Output Equations:

- $Q = Q_{next}$
- $Q' = Q_{next}'$

These equations describe the relationship between the current state, inputs, and the next state of the JK flip-flop. The JK flip-flop's behavior is determined by the combination of J, K inputs, and the current state, as well as the clock signal.

It's important to note that these equations are specific to positive-edge-triggered JK flip-flops, where the state changes occur on the rising edge of the clock signal. If you are working with a negative-edge-triggered flip-flop or asynchronous inputs, the equations may differ. Always refer to the datasheet or specific implementation details for accurate equations based on the flip-flop model you are using.

4. MASTER - SLAVE JK FLIP-FLOP

The master-slave JK flip-flop is a sequential digital circuit that consists of two JK flip-flops, often referred to as the master and slave stages. The principle of a master-slave JK flip-flop involves using these two stages in a specific sequence to prevent the occurrence of an invalid state that can happen in a single JK flip-flop. The master-slave configuration helps to improve the reliability of the output and ensures proper operation, especially in synchronous digital systems. In digital systems, the clock edge triggering mechanism is crucial for proper synchronization and reliable operation. Master-slave flip-flops are often used to implement edge-triggered behavior.

Here's a detailed explanation of the principle of a master-slave JK flip-flop:

1. Master Stage:

- The master stage is sensitive to the clock signal (CLK) and changes in the input signals (J and K).
- During the active edge of the clock signal (e.g., rising edge or falling edge, depending on the design), the master stage captures the input signals and computes its output.
- However, the output of the master stage does not immediately affect the overall output of the flip-flop.

2. Holding State:

- The output of the master stage is held constant until the next clock transition. This holding state ensures that any changes in the input during the active clock edge do not immediately propagate to the overall output.

3. Slave Stage:

- The slave stage is activated on the opposite edge of the clock signal compared to the master stage. For example, if the master stage is triggered on the rising edge, the slave stage is triggered on the falling edge, and vice versa.
- The output of the master stage is transferred to the slave stage during the active edge of the clock signal.

4. Output Stability:

- The output of the slave stage becomes the overall output of the master-slave JK flip-flop.

- The master-slave configuration ensures that the output is stable and unaffected by changes in the input during the clock transition.

5. Sequential Operation:

- The master and slave stages work in a sequential manner, and this sequential operation helps prevent glitches or invalid states that might occur in a single-stage flip-flop.

6. Clocking Strategy:

- The clocking strategy is crucial in master-slave flip-flop design. The master and slave stages are often triggered on opposite edges of the clock signal to avoid conflicts and ensure proper sequencing.

By controlling the clock edge triggering mechanism, digital designers can ensure proper sequencing and synchronization of the flip-flop within the larger digital system. Choosing between rising-edge or falling-edge triggering depends on the specific requirements and timing considerations of the system being designed. The choice of clocking strategy helps prevent glitches and ensures reliable operation in the presence of complex digital signals.

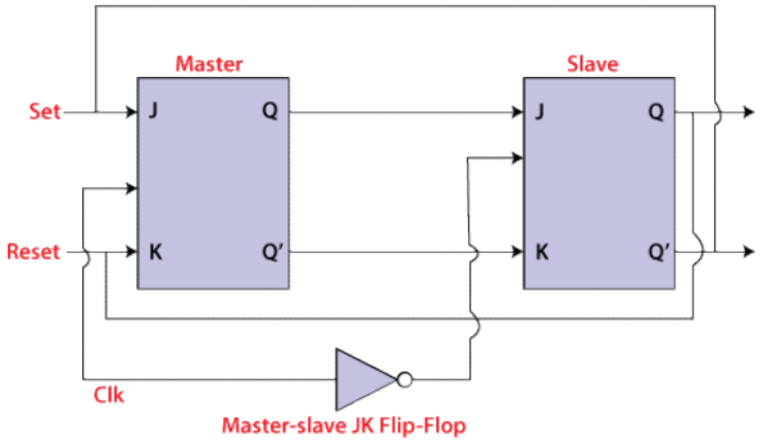


Fig2: Master-Slave JK flip-flop

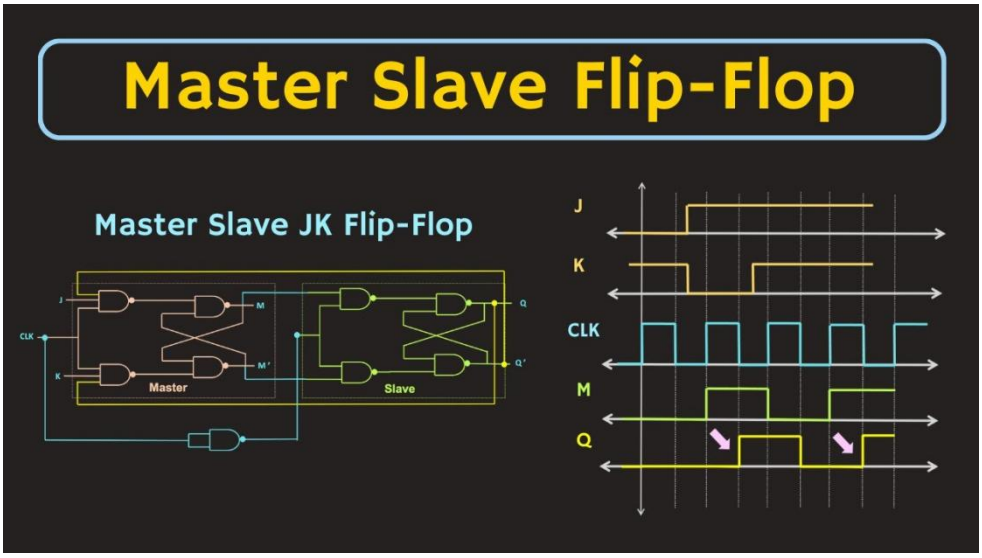
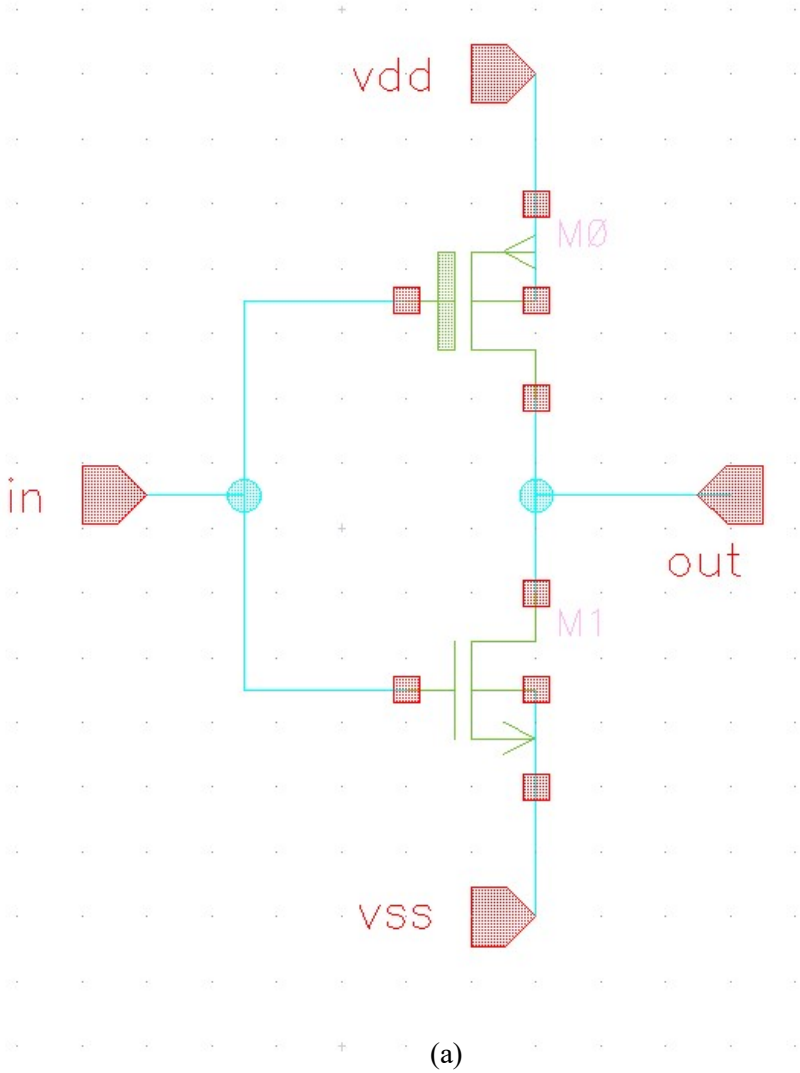
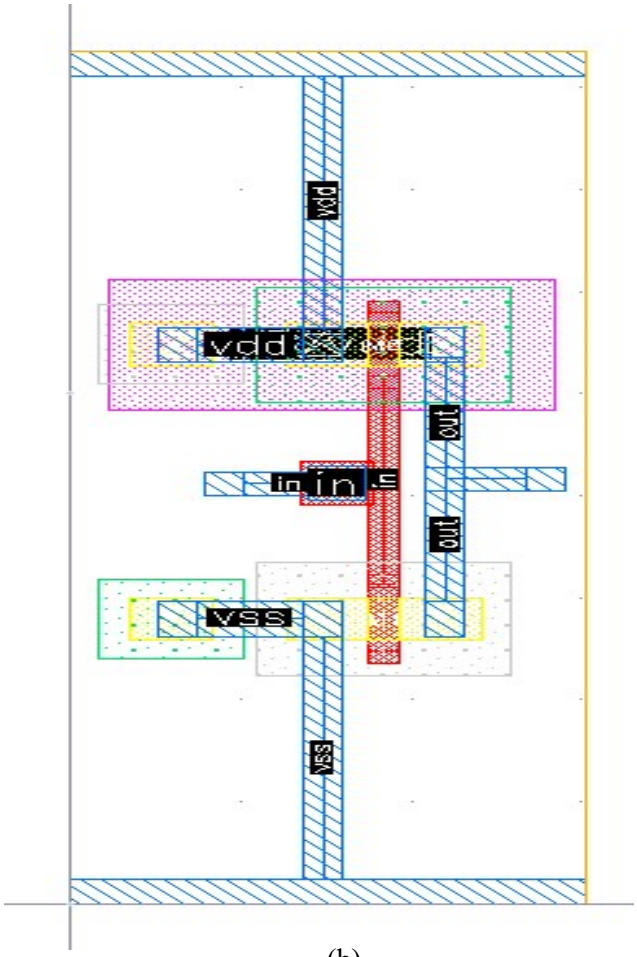


Fig3: Timing diagram for JK flip-flop

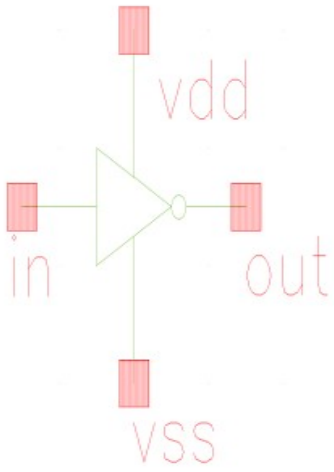
5. Results



(a)

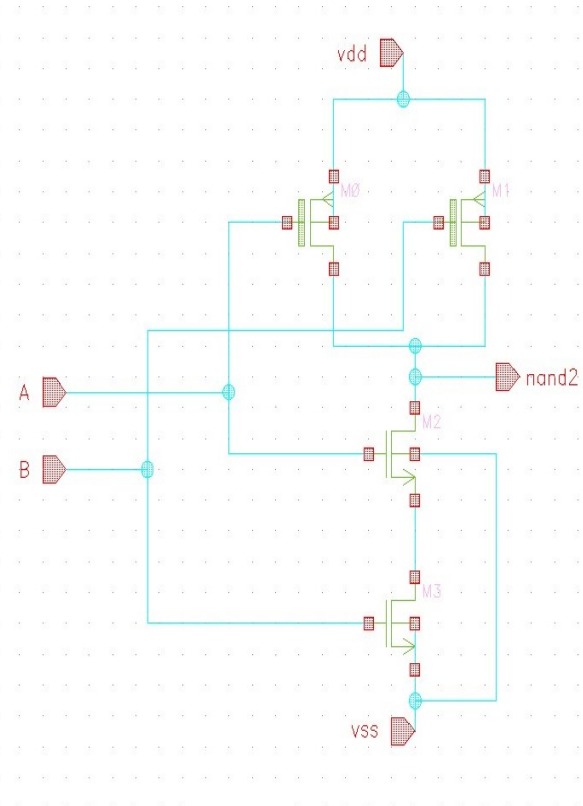


(b)

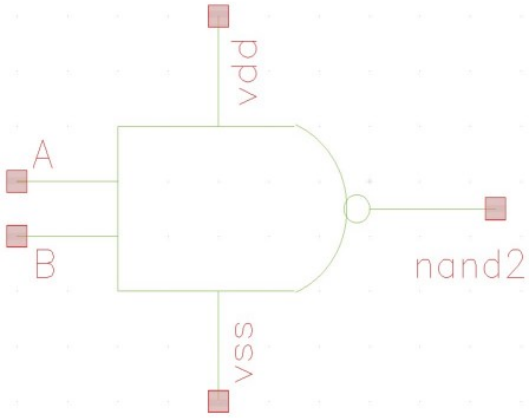


(c)

Fig4: Inverter (a) Schematic, (b) Layout, (c) Symbol



(a)



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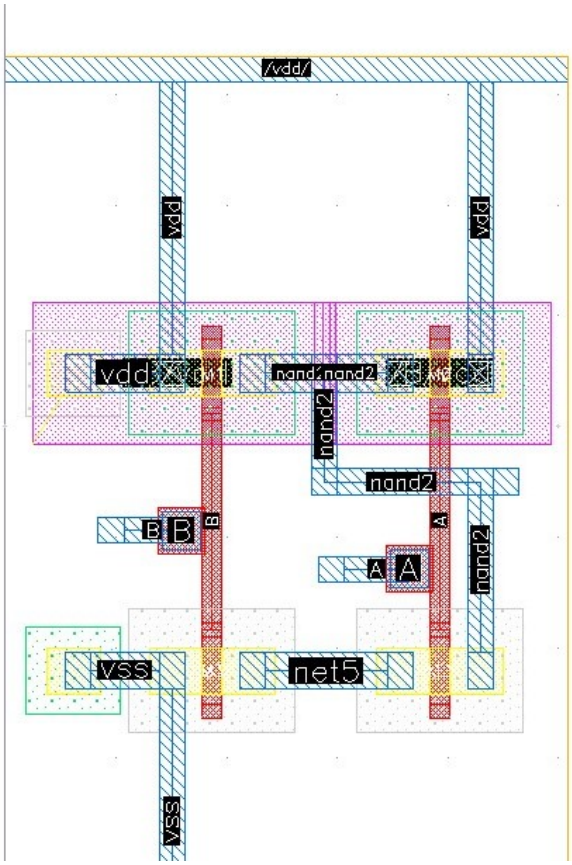
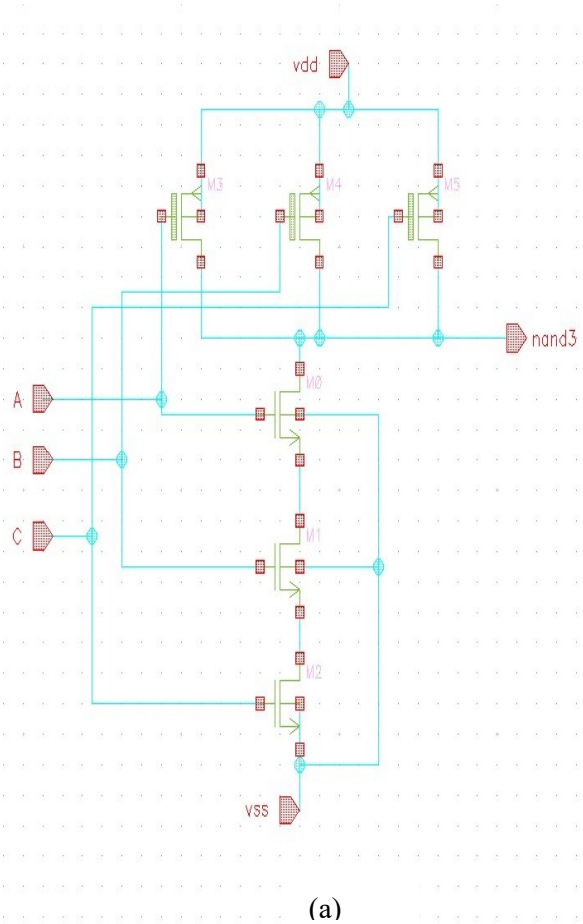
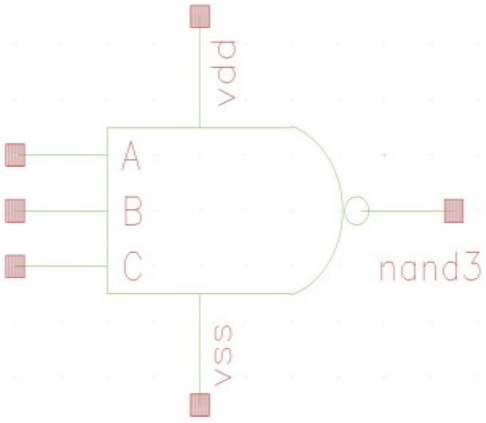


(b)

Fig5: 2 input NAND gate (a) schematic, (b) layout, (c) symbol



(a)



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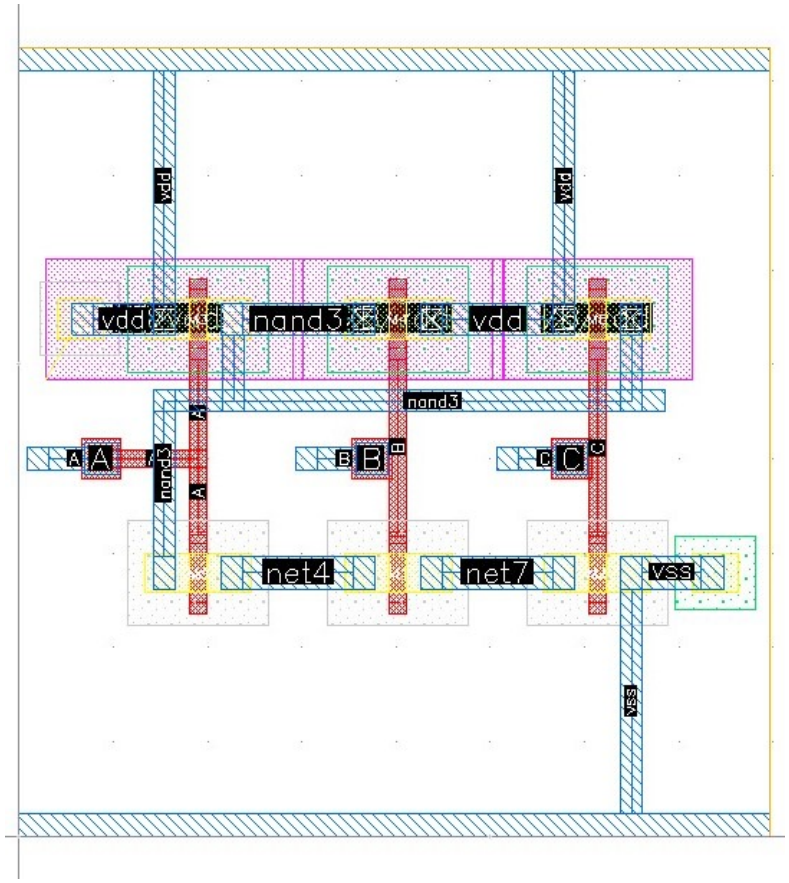

(b)

Fig6: 3 input NAND gate (a) schematic, (b) layout, (c) symbol

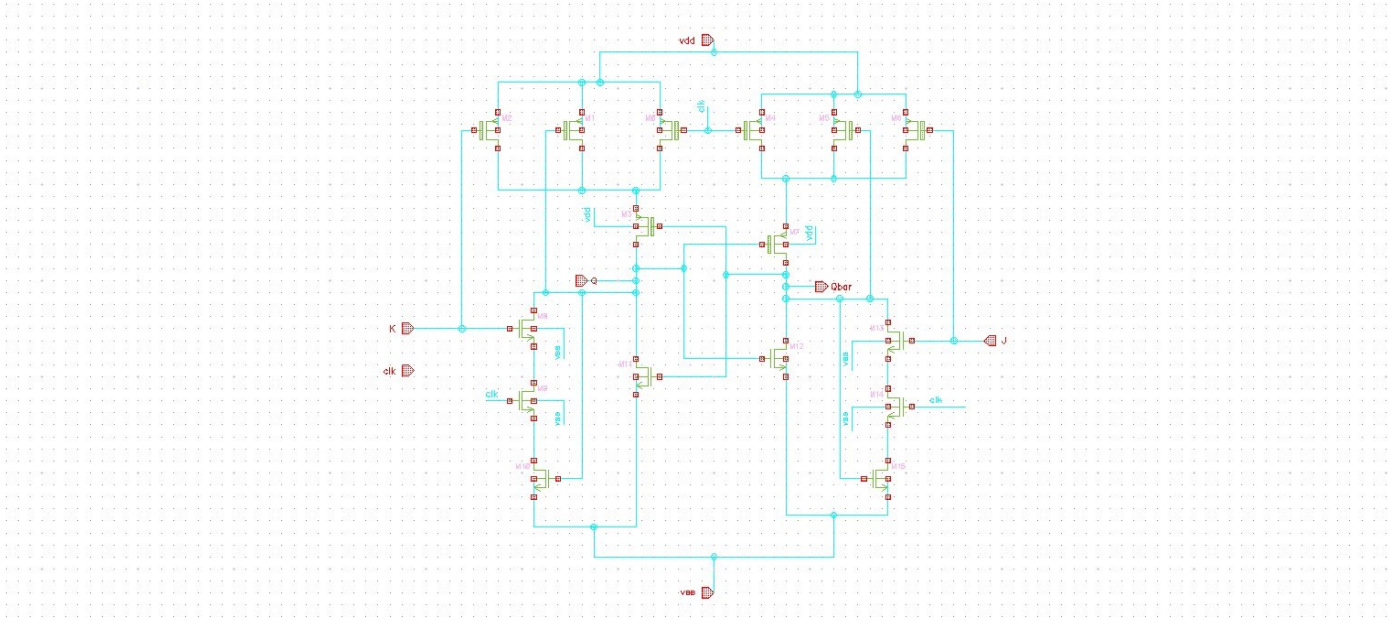

Fig7: JK Latch schematic using transistor only

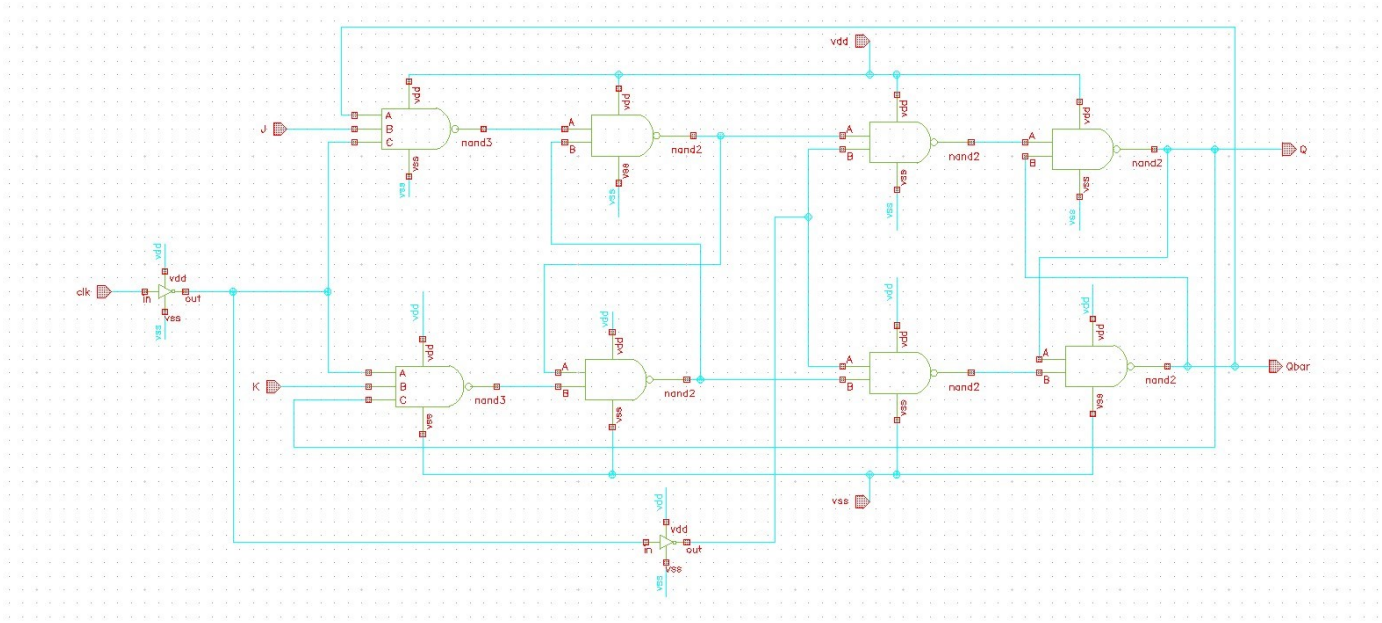

Fig8: Master Slave based edge triggered JK flip-flop using only Nand gates

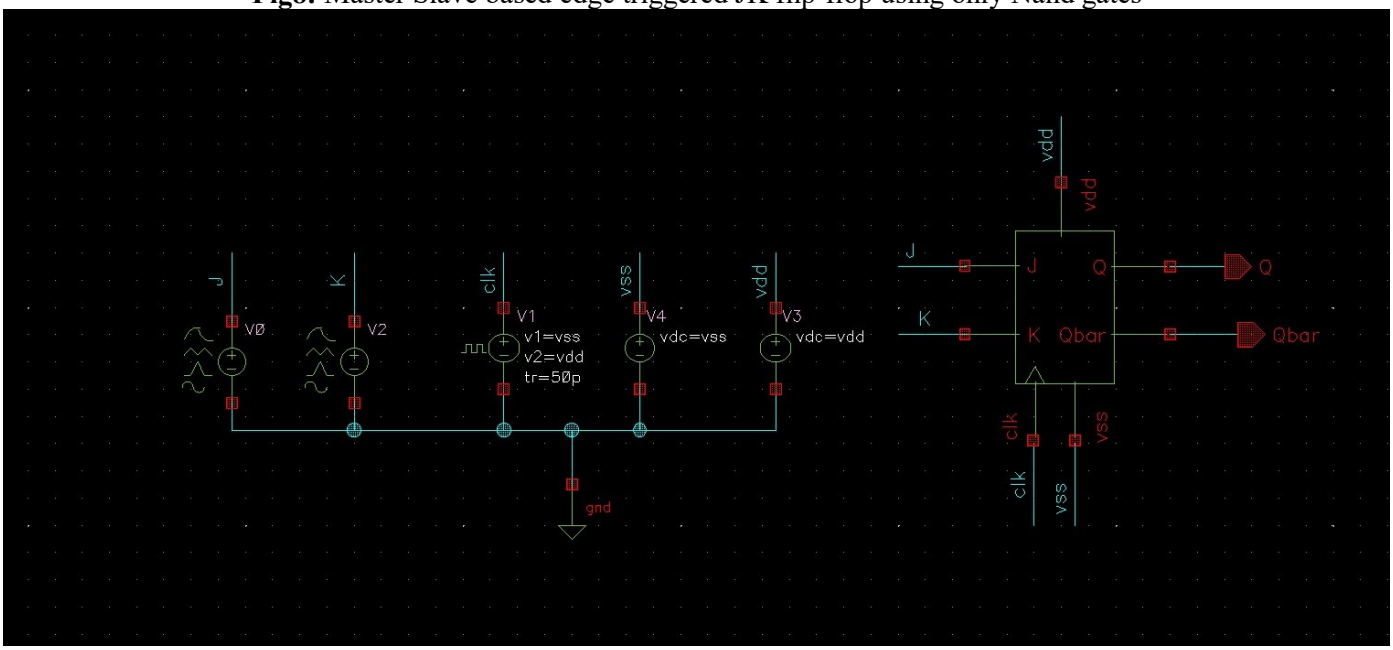

Fig9: JK flip-flop test-bench with specified inputs

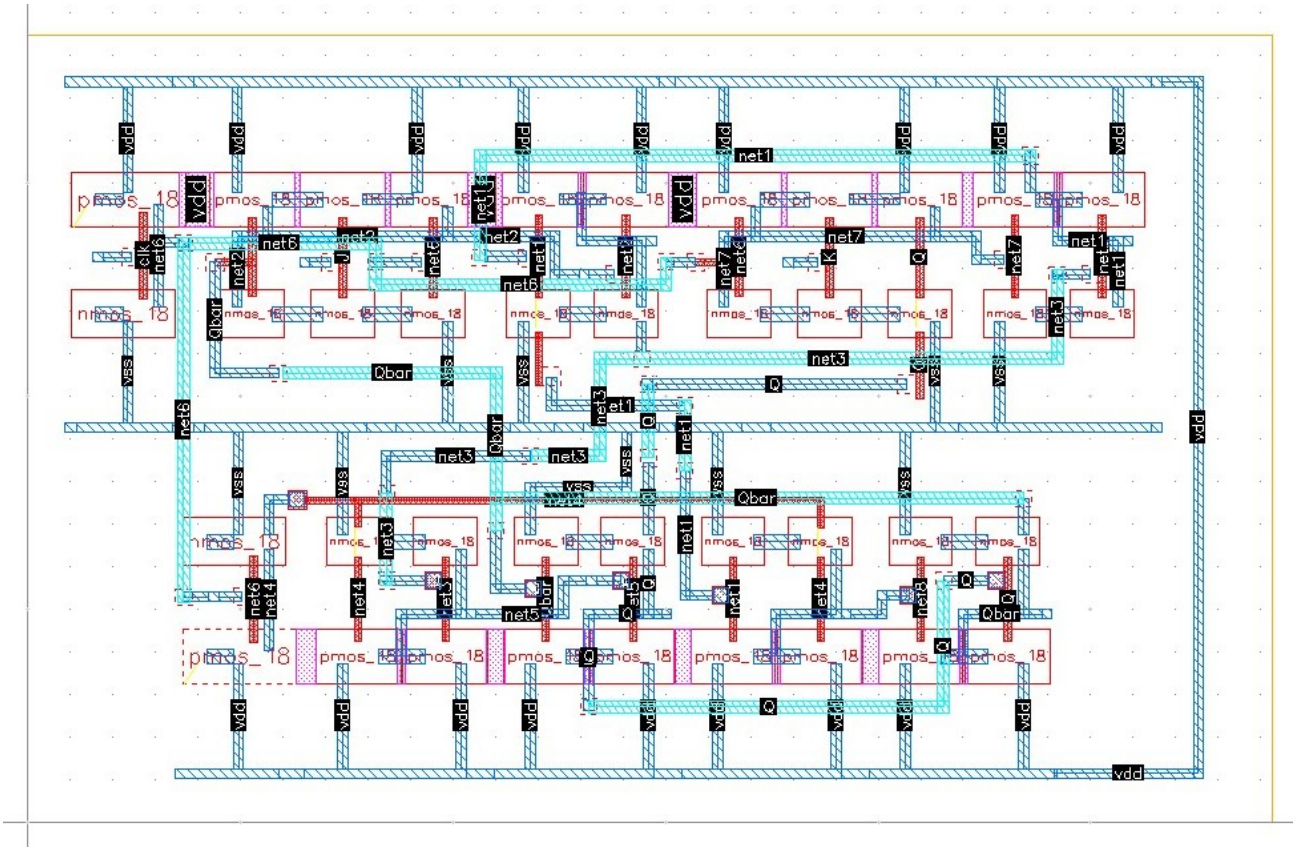

Fig10: JK master-slave layout

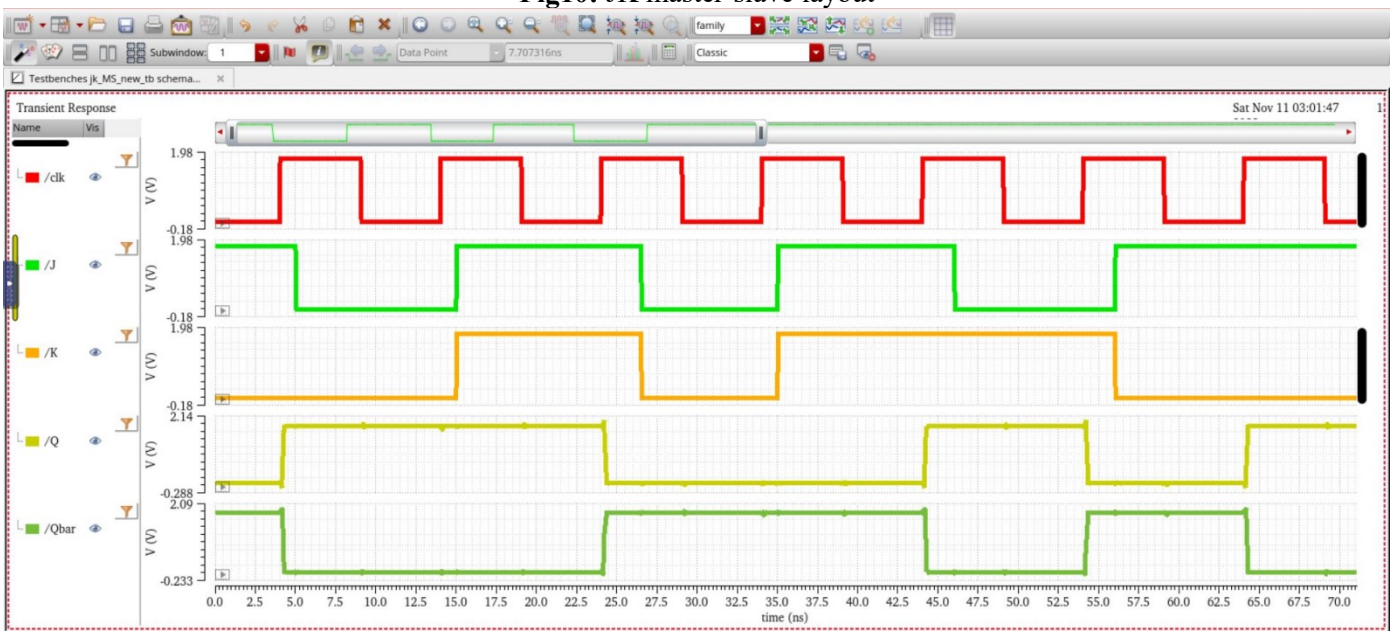

Fig11: Positive edge triggered clock JK flip flop with inputs as clk, J, and K giving outputs as Q and Q'

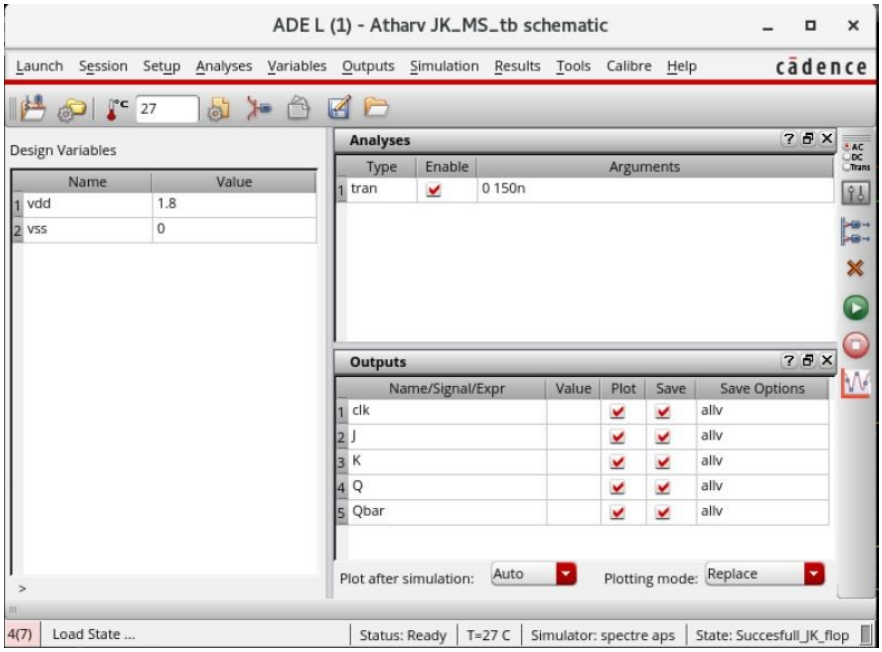

Fig12: ADE L WINDOW

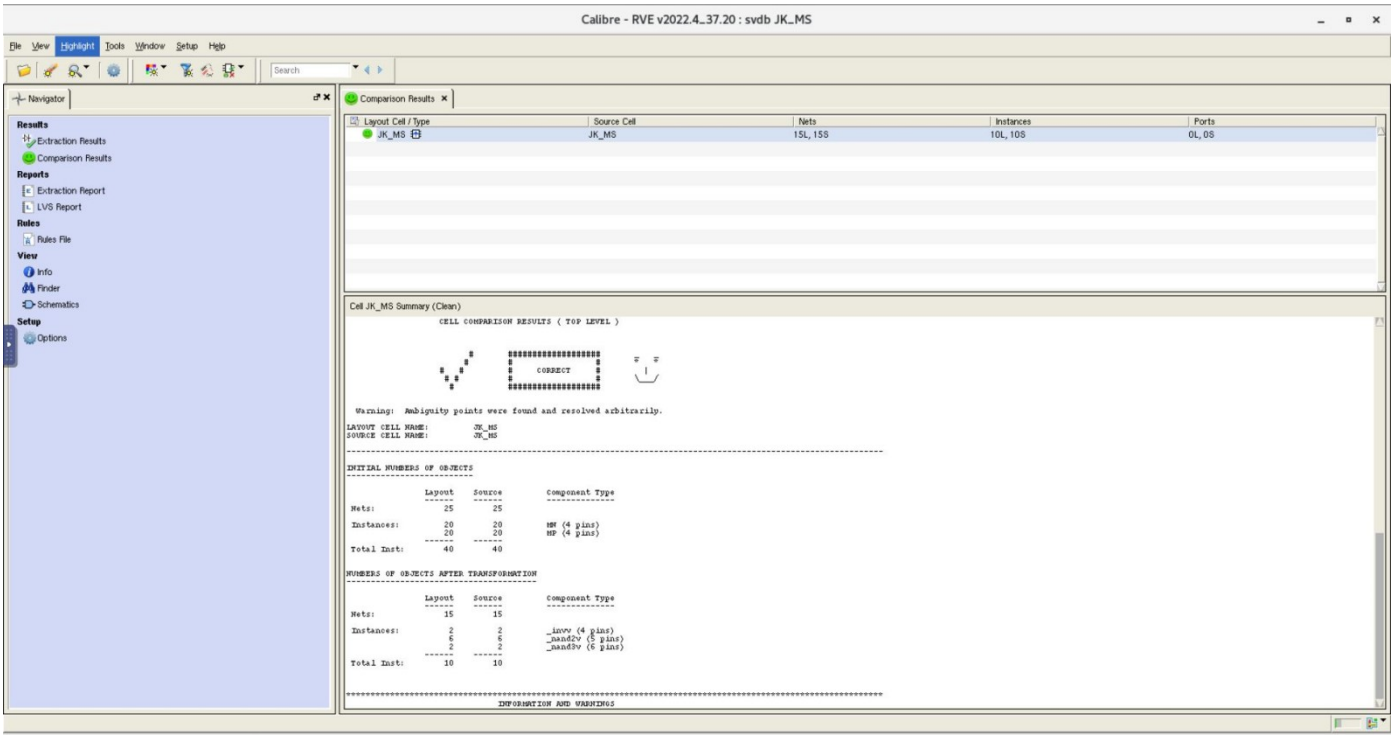

Fig13: LVS Report

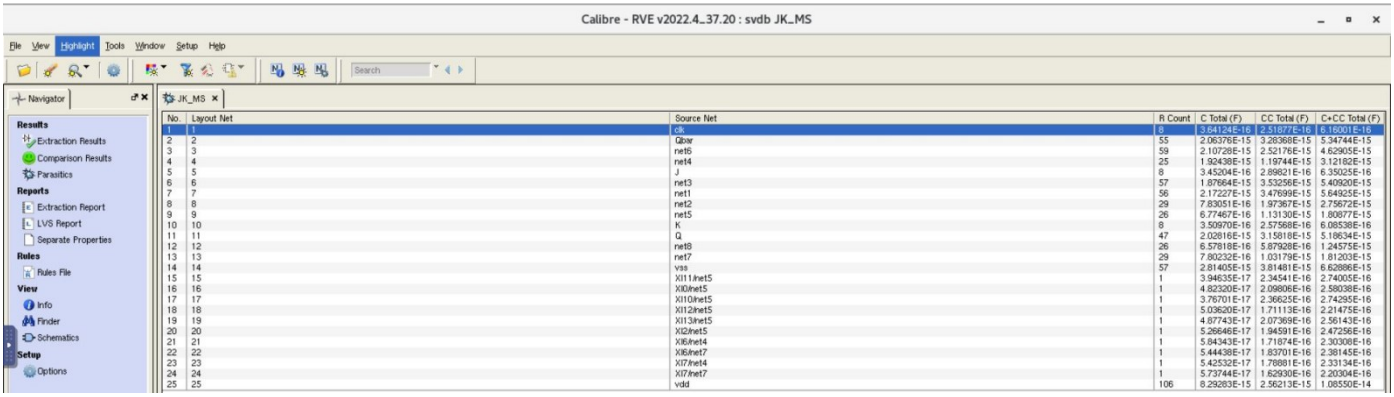

Fig14: PEX Report

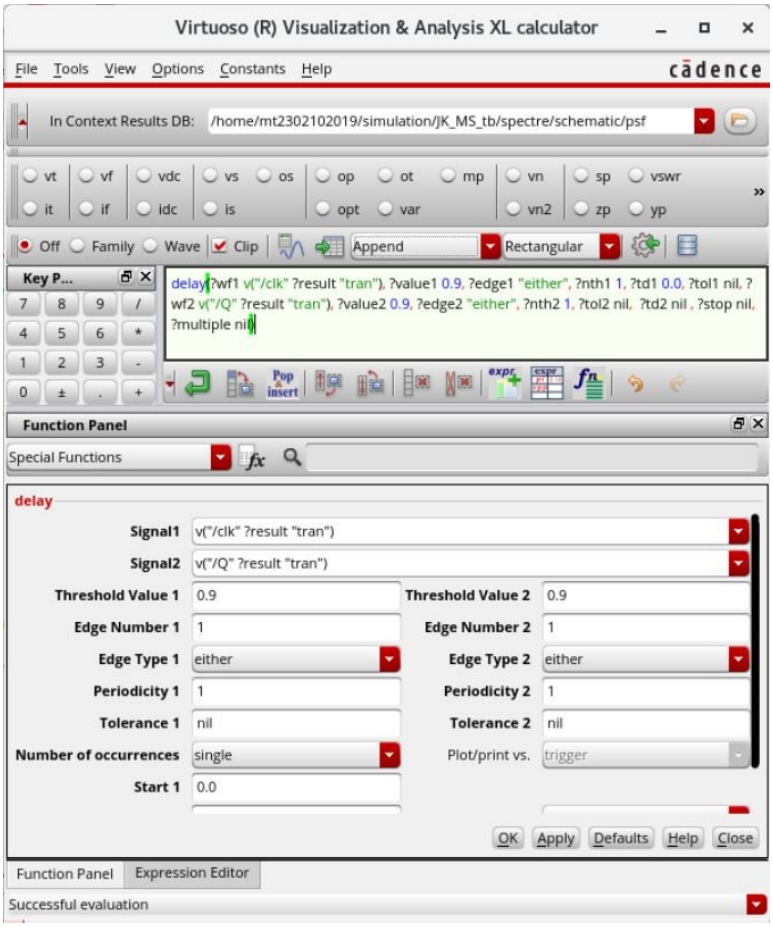

Fig15: Calculation representing delay of clk-q delay

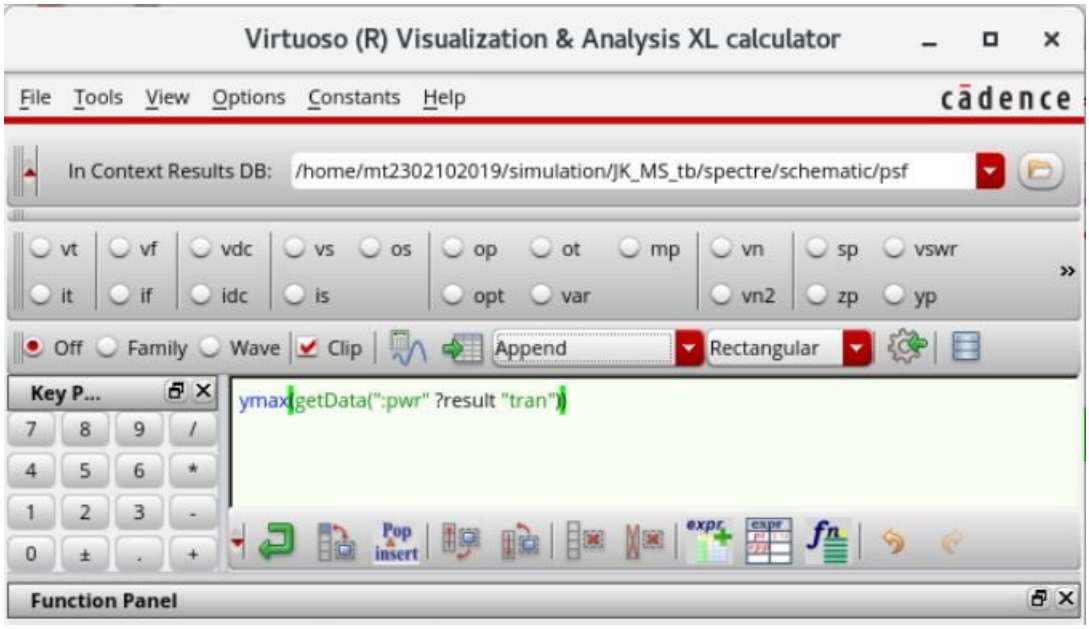

Fig16: Calculation representing power of the circuit

Outputs

	Name/Signal/Expr	Value	Plot	Save
1	clk		☑	☑
2	J		☑	☑
3	K		☑	☑
4	Q		☑	☑
5	Qbar		☑	☑
6	Clk-Q_delay	312.291p	☑	☑
7	Power(maximum)	331.526u	☑	☑

Fig17: Numerical values representing power and CLK-Q delay

Area = 27 x 16.8 um^2

Fig6, 7 and 8 represents the inverter 2 input nand and 3 input nand gates along with their symbols and layouts.
These gates are to be used in the main JK latch and further be used in JK master slave flip flop circuit.

These layouts helps us to instantiate more than 2 gates in their layout form and then convert them into transistor level schematic and easily form same substrate material.

Fig 9 represents JK latch whose inputs are J, K, clk with power supply as Vdd and Vss. The outputs obtained are Q and Qbar. The latch works on the high value of clock i.e. level triggered clock.

Fig 10 represents JK master slave using all the gates made above.

6. Conclusion

This project which has been designed is operating accurately as per our requirement. As we have mentioned above, the JK flip flop is the basic unit of memory and used everywhere, with the constraints of input the output can be found as accurately possible. The features of this project include the power consumption, area requirement and Clk-Q delay are in the sufficient values.

Parameter	Value
Power	331.526 uW
CLK - Q delay	312.291 ps
Tplh	317.47ps
Tphl	307.112 ps
Area used of PR boundary	27 x 16.8 um^2

Table3: Parametric values

The flip flop is working at the positive edge of the clock.
The static time analysis required is such that the data should be stable for at least 1/2 period and should be stable before negative edge of clock.
The layout is made by converting whole structure in two parts and then adding them using same Vss and 2 Vdd lines as can be seen from layout.

Performance of JK Flip-Flop as compared to JK Latch:

- Speed and Timing: Edge-triggered flip-flops are often faster and have more predictable timing characteristics than latches, especially in synchronous designs where timing is critical.

- Complexity: Flip-flops are generally more complex than latches, but this complexity is often justified by the advantages they offer in terms of synchronization and performance.

- Power Consumption: Latches may consume less power than flip-flops since they are continuously active, while flip-flops only consume significant power during clock transitions.

- Design Complexity: Latches might be simpler to design and understand, making them suitable for certain applications with less stringent performance requirements.

Performance	JK Latch	JK Flip Flop
Timing and Synchronization	Timing in a JK latch is continuous, as it responds to changes in the input levels immediately. Latches are not synchronized with a clock signal, making their behavior harder to predict in complex systems.	Edge-triggered flip-flops synchronize their operations with a clock signal. Timing is well-defined, and the flip-flop responds to changes at the clock edge, making it easier to analyze and design in synchronous systems.
Propagation Delay	The propagation delay in a JK latch is typically shorter than in a flip-flop because the latch responds immediately to input changes.	Edge-triggered flip-flops have a longer propagation delay due to the synchronization with the clock signal. However, this delay is predictable and can be optimized in synchronous designs.
Power Consumption	Latches may consume less power than flip-flops because they are continuously active and respond to input changes at all times.	Flip-flops consume power primarily during clock transitions, resulting in potential power savings during periods of inactivity.
Design Complexity:	Latches are generally simpler to design and understand, making them suitable for certain applications where simplicity is prioritized over performance.	Flip-flops are more complex due to the additional clock input and synchronization circuitry. However, this complexity is often justified by the advantages they offer in terms of predictability and ease of integration into larger synchronous designs.
Ease of Integration	Latches may be easier to integrate into certain designs due to their simpler structure and continuous operation.	Flip-flops might be more challenging to integrate, but their synchronization with a clock signal facilitates overall system design and analysis.

Table4: Comparison Table for JK Latch and JK Flip-Flop

7. References

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