FULL ADDER USING CMOS

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***Abstract*—This paper proposes the design of a Full adder using 28 conventional cmos transistors , presents a full adder cell having reduced power and delay.This adder uses regular cmos structures (pull up and pull down networks) with pmos and nmos as a part of a complementary network.The full adder is designed in 0.28um technology and the advantage of this design is its high noise margin and thus reliable operation at low voltage.The layout of the cmos gate was also simplified due to the complementary transistor pairs.It's advantages include robustness and scalability at low supply voltages.**

***Index Terms*—Full adder, sum , carry**

I. Reference circuit details

Circuit realization for low power and low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. A basic full adder system in digital computing system is 1 bit full adder having three 1 bits A ,B, C as inputs and the single outputs obtained are SUM and CARRY .This circuit is a combination of PMOS pull up transistors and NMOS pull down transistors. [1]The relation between the inputs and outputs are given as

$$sum = A \oplus B \oplus C \tag{1}$$

$$carry = C_{out} = AB + BC + AC \tag{2}$$

Full Adder performs the addition bit by bit with carry input and provides output with carry output. The carry output becomes the carry input for next input combination.The normal full adder operation will give the above mentioned equations.But it requires more number of transistors and area to realise.So the inverted form of carry output obtained is considering as an input component thereby obtaining the sum output equation that depends on four different varioble inputs. [2] Then the above equations can be altered as

$$sum = ABC + (A + B + C)\bar{C_{out}} \tag{3}$$

$$C_{out} = AB + C(A + B) \tag{4}$$

These outputs can be implemented using the 0.28um cmos technology which is cost effective and used for low power applications. Here the primary concern to design Full adder is to obtain low power consumption and delay in critical path and full output swing with low number of transistors to implement it.

II. Reference circuit design

The design consist of 28 cmos transistors among which four are part of inverters , 10 transistors will conribute for the$\bar{C_{out}}$ and remaining 14 for the inverted sum output.

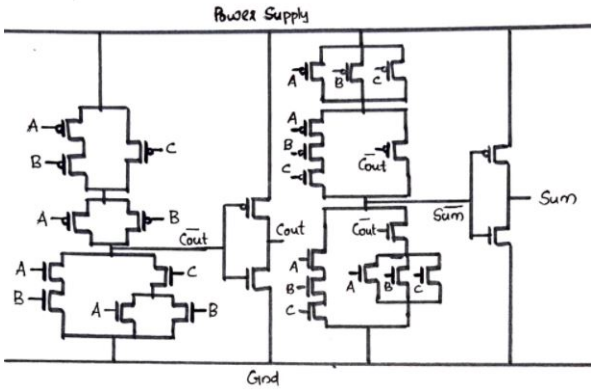

Fig. 1. CMOS circuit design

III. Reference waveforms and area estimate

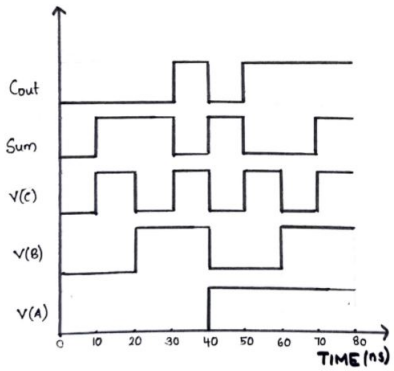

Fig. 2. Waveforms

IV. References

The references [1] and [2] are cited in this paper.

References

[1] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. Addison Wesley, 2011. [Online]. Available: https://books.google.co.in/books?id=sv8OQgAACAAJ

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