Digital Design & Verilog – Beginner Assignment

Goal: Make digital design intuitive, confidence building, and fun for absolute beginners.

PART A: Digital Logic Warm-Up (No HDL)

1. Number Systems Challenge: Convert 255.375 (base 10) into Binary, Octal, and Hexadecimal.
2. Reverse Thinking: Given 110101.101 (base 2), find its decimal value.
3. Binary Detective: Without converting to decimal, identify whether 100111 (base 2) is divisible by 3. Explain why.
4. Complement Puzzle: Represent −23 (base 10) using 8 bit 2's complement.
5. Boolean Logic Mini Game: Simplify F = (A + B)(A' + C)(B + C') and explain each step in plain English.
6. K Map Visual Thinking: Minimize F(A,B,C) = Σm(1,3,5,7). What pattern do you observe?

PART B: First Steps into Verilog

1. Explore HDLBits: Complete the sections – Getting Started, Wire vs Reg, Simple Combinational Logic.
2. Write your first module: Implement a 2 input AND gate in Verilog.
3. Upgrade it: Modify the module to behave like an OR gate using assign statements.
4. Truth Table to Code: Given the truth table of a XOR gate, write the Verilog module.
5. Simulation (Optional): Simulate your design using Vivado or EDA Playground and verify outputs.

PART C: Think Like a Designer

Design a Majority Voter: Output is 1 if at least two of the three inputs are 1.

Submission Guidelines

- Handwritten or typed solutions are allowed.
- Verilog code must be properly commented.
- Focus on understanding, not perfection.