COMPUTER ORGANIZATION AND ARCHITECTURE LAB

INTRODUCTION TO VERILOG PROGRAMMING

VERILOG ASSIGNMENT-2

GROUP 09

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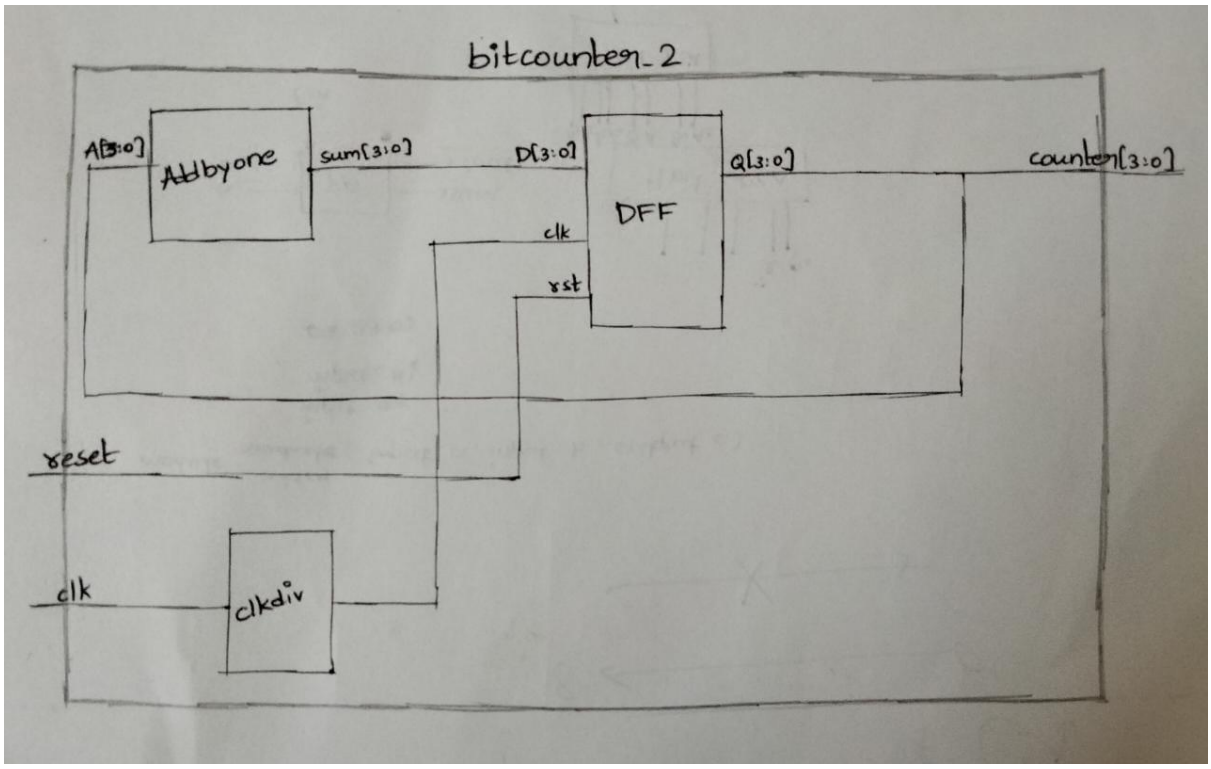
Designing Counters and Displaying the output on the LEDs of the FPGA Board

In this assignment we have designed a Binary counter (a sequential circuit) with an asynchronous reset in two ways, behavioural and structural.

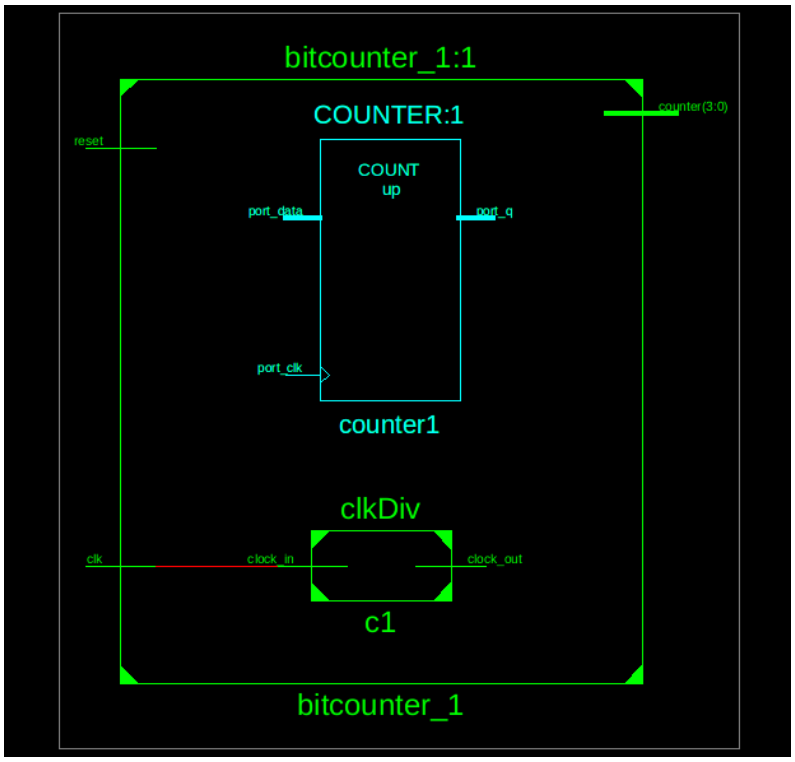
For behavioural design, we have created a verilog module - bitcounter1 and a UCF file with appropriate locations to the FPGA board i.e., SPARTAN3 board. We have also added a clock divider so that the output on the LEDs is properly visible. The frequency of the internal clock of the device is 4MHz and hence the state of the counter changes at the rate of 250 ns. So, in the clock divider, we have divided with 4,00,000 which makes it to 100 ms so that the result of the counter is clearly noticed. We have also created a testbench and checked the simulations.

For structural design, we have created a verilog module – bitcounter2 which has an add by one adder, clock divider and DFF as its submodules. For the add-by-one block, we have modified our RCA 4-bit adder which was done in the previous Verilog assignment as mentioned in the question. The clock divider functions in the same way as the one used in the first part. Similarly, we have created a UCF file with appropriate locations and a testbench to check the simulation.

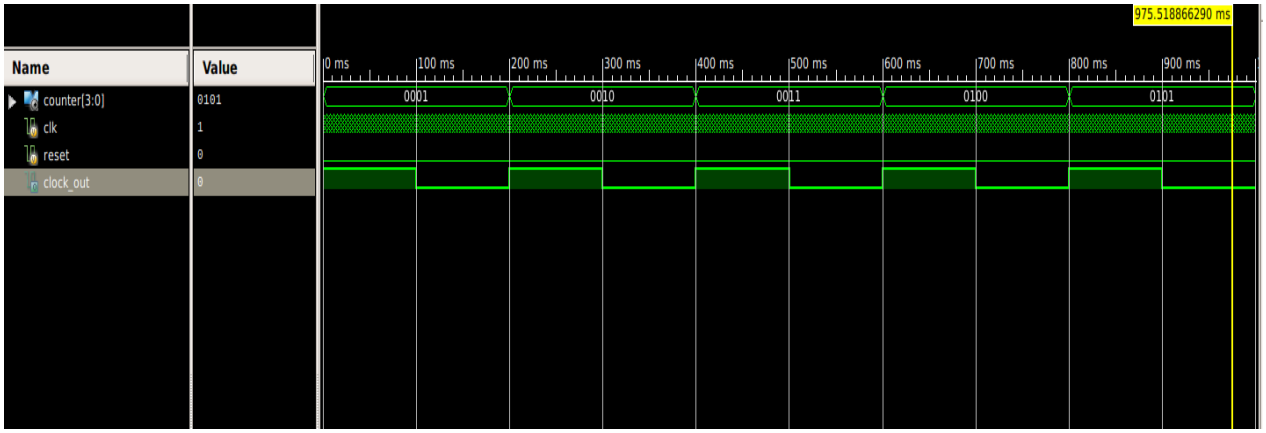


Part-1: Behavioural design

Schematic view:

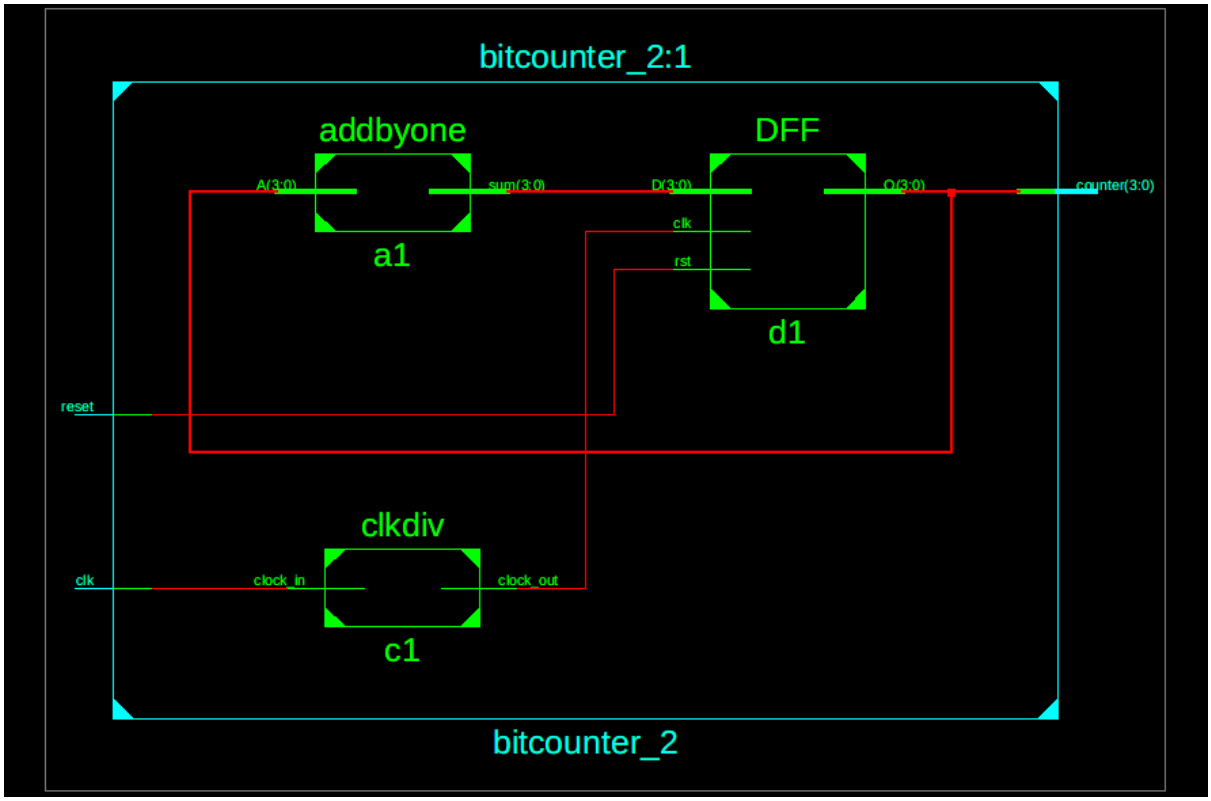


Simulation:

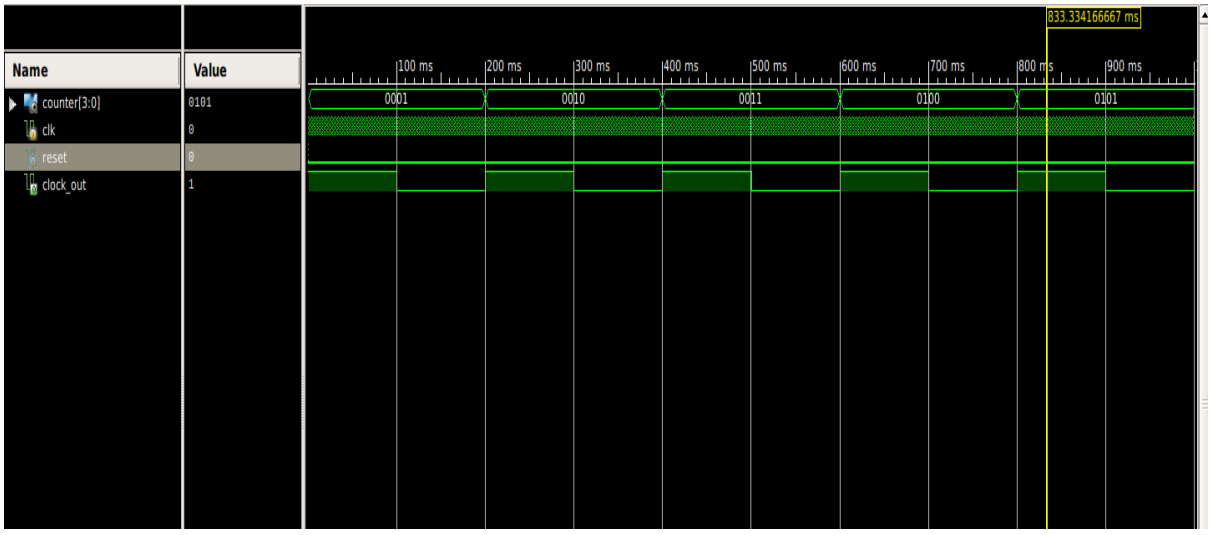


Part-1: Structural design

Schematic view:



Simulation:



OUTPUTS ON THE LEDs OF FPGA BOARD: