Computer organisation and architecture (CS31007)

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Programmed I/O

- CPU requests I/O operation
- I/O module performs operation
- I/O module sets status bits
- CPU checks status bits periodically
- I/O module does not inform CPU directly
- I/O module does not interrupt CPU
- CPU may wait or come back later
- Data transfers between i/o device and memory go through CPU

Interrupt driven

- CPU issues commands to the I/O module
- CPU may HLT (wait for interrupt)
- Current processed may be moved to i/o wait because i/o was originally invoked by s/w interrupt
- Input device interrupts CPU when new data has arrived
- Output device interrupts CPU when given data is output
- Data transfers between i/o device and memory still go through CPU

Direct memory access

- Direct Memory Access (DMA) supports direct transfer of data between i/o device and memory
- CPU is only involved at the beginning and end of the transfer
- End of transfer event is triggered by an interrupt from the DMA enabled i/o device
- Direct Memory Access needs a special hardware called DMA controller (DMAC)
- DMAC has the following:
  - register for source and destination addresses (where to read/write the data)
  - counter counters to track the number of transferred bytes
  - logic and h/w to access system bus (BUSREQ, BUSGRANT)
  - logic and h/w to interrupt the CUP on completion

Burst vs cycle stealing

Burst mode

- A number of data words are transferred continiously until completion
- Suitable for fast devices
- CPU may remain idle unless kept busy via cache

Cycle stealing mode

- One word transferred at a time
- CPU operation largely unaffected, high CPU utilisation