Lecture - 1
13.01.2026

Ram, Rom, storage

Hardware lab :-

Counter, register দিয়ে Design

ALU → Arithmatic Logic Unit] Final

register দিয়ে CPU তৈরী

Theory ...

Ram, Rom – Primary

Hardisk → Secondary

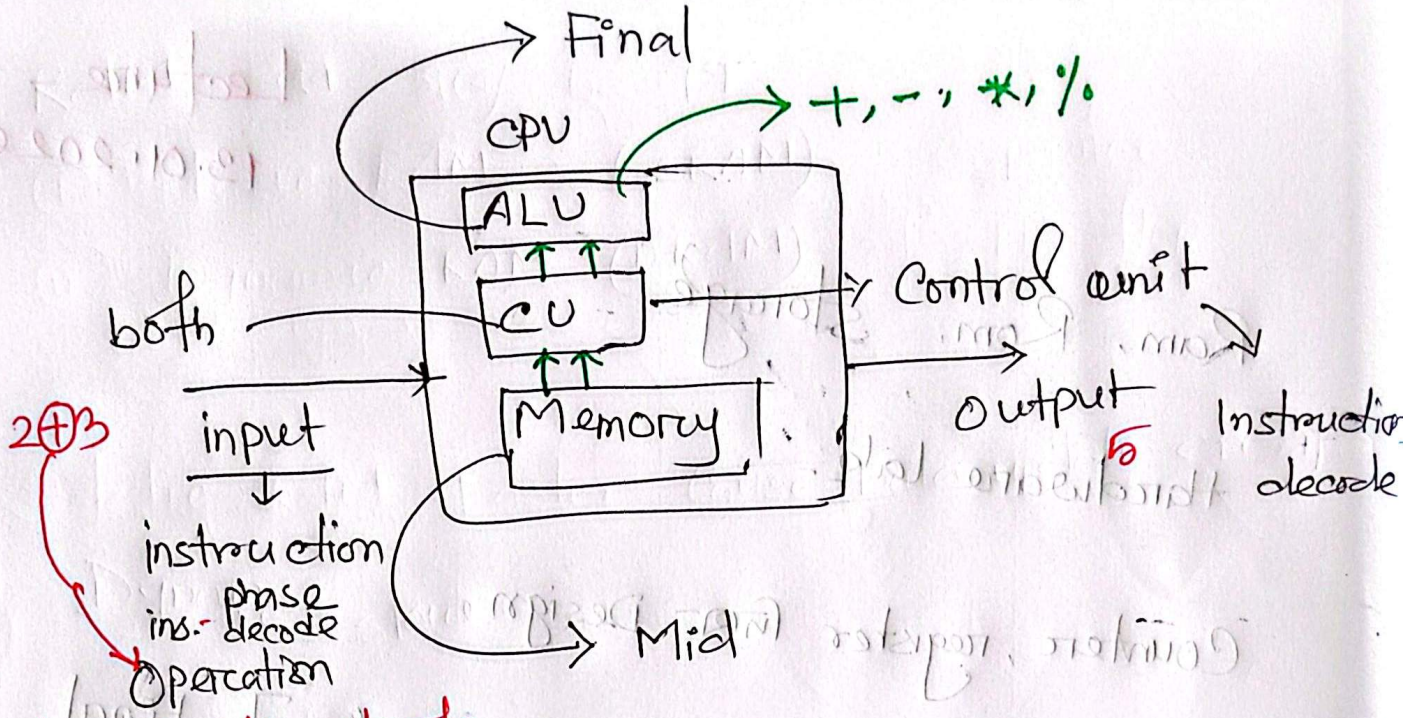
Memory – সাজানো

→ Computer Architecture কয় তিনটা basic

→ Com. Arc. কি ? → Mechanism [ভিতরের functionality]

→ Com. design [কি কি hardware গুলোকে design করা

→ Comp. Organization [কিভাবে org. করা যায়]
|| Connect করবে Hardware]



two variable decode

CU → মানুষের ব্রেইন

Processing → যোগ করবে

storing → Output বা Reset

→ এই সবগুলো করে CU

ALU → +, −, *, ÷ করবে

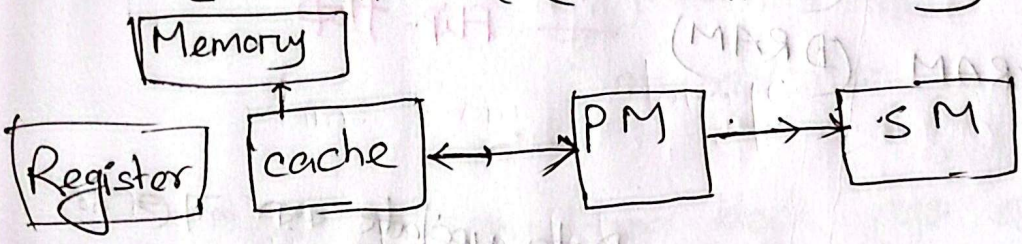
Memory → store করবে

বাকি সব → CU

Memory → RAM, ROM, SSD, HDD, ~~cash~~ cache

→ যা গের টাকে Register বলে

CPU এর সবথেকে কাছের Memory হচ্ছে Cache



Temp. ভ্যালু রাখতে হলে Register ব্যবহৃত হয়।

Cache → যেটা frequently use হয়।

PM → RAM, ROM

CPU কখনো directly SM-কে Access করতে পারে না। PM হয়ে যাবে।

Cache — সবথেকে বেশী Faster

তারপর PM

then — SM

Faster:

Cache > PM > SM

Capacity: Cache < PM < SM

RAM - এর মধ্যে দুই ভাগ

(i) Static RAM (SRAM) — Capacitor

(ii) Dynamic RAM (DRAM) — Flip-flop

Static RAM faster Cause Data update করার লাগে না

Dynamic store

Refresh

১ সেট

কোনো

কমেন্ট

Lecture-2
20.1.2026

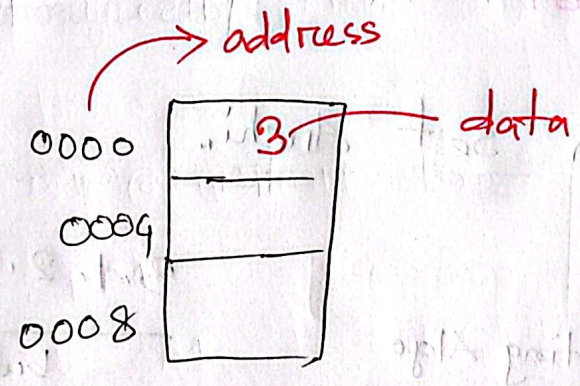
Introduction

ছোট ছোট building block থেকে বড় building – Com. Organi-zation, CPU and Memory,

তিনটা bus -এর মাধ্যমে connect থাকে

(i) control bus – instruction অনুযায়ী কাজ পাবে কে করবে (ALU কে করবে) [রেইনকোড]

(ii) Address bus → Address কোন করার



শুধু Output

(iii) Data bus – Address থেকে provide করে।

Comp. Design — Hardware design

Design → organization → Archi.

Comp. Archi.

overcall functionality and capabilities of the comp. system.

performance, size, Cost, Energy → Trade off

এগুলোর উপর ভিত্তি করে comp. arch. design করে।

C.A. Level of Transformation

Instruction Set Archi.

7 Segment

→ Sorting Algo

3, 1, 2, 5, 7, 6, 4

bubble

Problem

Algorithm

Program/Language

Runtime system

ISA

Microarch -

Logic

Devic

Electrons

Organization vs Archi. → এখান থেকে শুরু —

চুয়াল figure-থেকে বুঝা যাবে।

Data Movement — কোথা থেকে data যাবে এবং কোথায় যাবে

→ Source and destination device connected থাকে Peripheral

→ অনেক দূরে (remote device) হলে data communication

→ Control unit সব control করে।

Data Movement device —

No data stored or processed

— Source থেকে destination এ পাঠানো।

→ Forward data

Data Storage device

শুধু store করতে হবে।

→ File থেকে একের জায়গায় পাঠ করলে Read

→ File Save করলে Write (বাইরে থেকে data Save)

external → Input and Output

→ No processing Performed

Data Processing on Stored Data

Storage → processing → control → storage

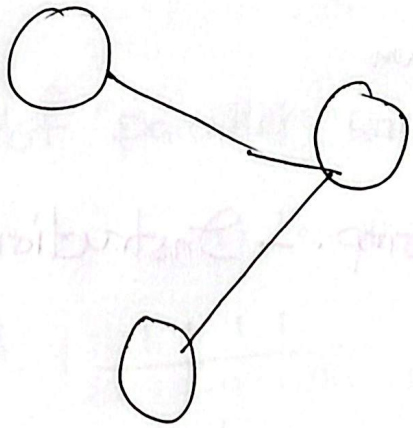
Data processing on En Route Data

Movement → control processing → control → storage

Lecture - 3

21.1.2026

Memory - কে Register বলা হয়



PC - Prog. Counter

CR - Register clear [Loop এর কাজ করে]

AC - Accumulator

Register - সবচেয়ে Fastest - Cache Memory এর আগে থাকে।
↳ সবচেয়ে ছোট সাইজ

Functional Unit

Set of instructions and data is called program or Instruction set

```
a=2; b=3;
a=a+b
b=b*a
```

→ Instruction set

program

Information in a Comp. – Instruction.

ins 1	0004
ins 2	0008
ins 3	0042
data 1	0016

→ opercands

a + b

|

opcode

SRAM → Flipflop

DRAM → Capacitor

Cache-Memory Static Ram দ্বারা তৈরী

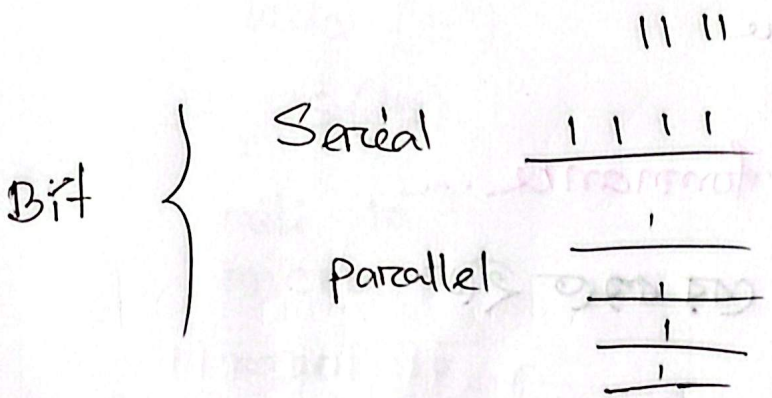
Flipflop -

Arithmetic : +, −, *, /

Logical : AND, OR, NOT

Manipulate → update, insert

→ Group of parallel wires is called bus.



Bus Structure

Performance Metrics.

→ Latency : time to completely execute a certain task. (→ এক্সিকিউট হতে কত সময় লাগে)

End − Start

5*

→ Throughput : amount of work that can be done over a period of time

A: 5s → 10^6 instructions

B: 10s → 10^{12} instruction

10s → 10^9 instruction

power : execution of program

Energy : Energy consume

Reliability : Failure rate

CPI → Clock cycle Per instruction

MIPS → Million instruction per seconds

Transaction per Minute

Measure of Performance...

CPI, MIPS → এগুলো বের করতে হবে

cycle Time: (T)

Clock Rate : f

$$f = \frac{1}{T}$$

Hz ← f, T → s (unit)

Math-1 :

A 200 MHz clock has a cycle time

$$\frac{1}{200 \times 10^6} \times 10^9 = 5\,ns$$

→ Nano তে রাখার জন্য 10^9 দ্বারা গুণ

Exa (10^{18})

Peta (10^{15})

Tera (10^{12})

Giga (10^{9})

Mega (10^{6})

Kilo (10^{3})

S (Hz)

উপর থেকে নিচে গেলে (−) দিতে হবে না।

উল্টো হলে (+)

mili 10^{-3}

micro 10^{-6}

nano 10^{-9}

Pico 10^{-12}

famto 10^{-15}

auto 10^{-18}

$$1\,Hz = 10^{-9}\,GHz$$

Execution time · Formula

$$T = \frac{N * CPI}{f}$$

N = Number of Instruction

CPI = Cycle per Instruction

f = frequency.

CamScanner

$N = 5 \times 10^6$

$CPI = 3$

$f = 1.5 \times 10^9$

$$= \frac{5 \times 10^6 \times 3}{1.5 \times 10^9}$$

MIPS

$$MIPS = \frac{f \text{ in } MHz}{CPI}$$

effective CPI

$$= \frac{\sum N * CPI}{\sum N}$$

Instruction	CPI
5	1
2	3
3	2
1	1

$$\text{effective CPI} = \frac{5*1 + 2*3 + 3*2 + 1*1}{5+2+3+1}$$

$f = 2\ GHz$; $CPI = 4$

$= 2 \times 10^9\ Hz$

$= 2 \times 10^9 \times 10^{-6}\ MHz$

$= 2 \times 10^3\ MHz$

$$MIPS = \frac{2 \times 10^3}{4}$$

Example-3:

Machine A → T = 10ns , CPI = 2

Machine B → T = 20ns , CPI = 1.2

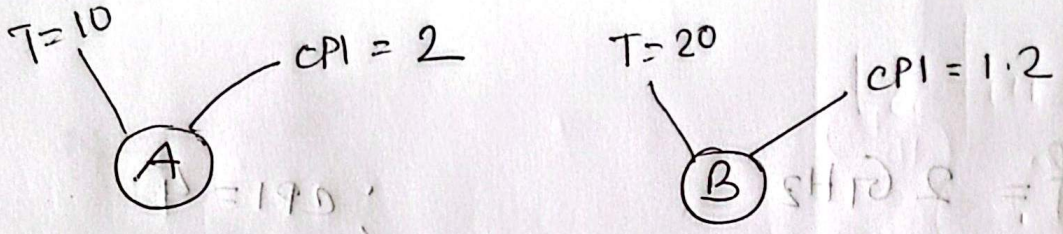
Machine কে দুইভাবে compare করা

→ Execution T (Time) < (কম হলে ভালো)

→ MIPS (বেশী হলে ভালো)

For execution Time

$$\frac{N * CPI}{f \rightarrow \frac{1}{T}}$$



$A \rightarrow \quad f = \frac{1}{T} = \frac{1}{10\,ns}$

$= \frac{1}{10 \times 10^{-9}}$

$= 0.1 \times 10^{9}$

$= 1 \times 10^{8}$

$B \rightarrow$

$= \frac{1}{20}$

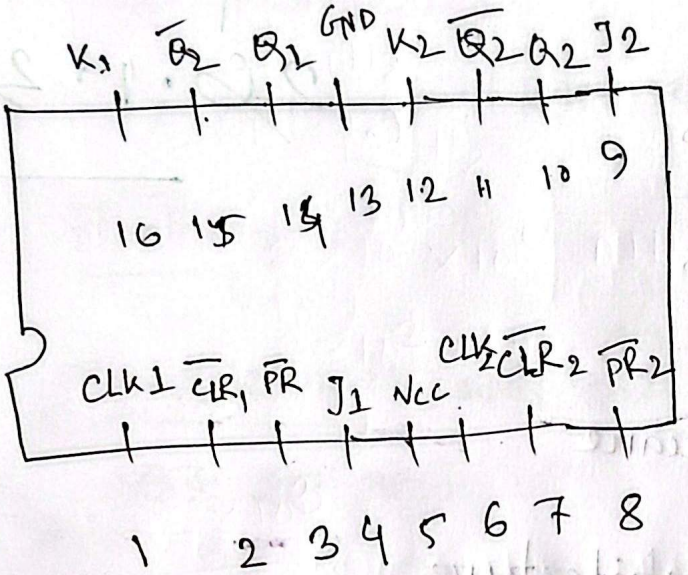
$= \frac{1}{20 \times 10^{-9}}$

$= 0.05 \times 10^{9}$

$= 5 \times 10^{7}$

Lab -2

25.1.2025



Q, $\overline{Q}$ = Output

CLR = Reset button

PR = Preset

একটা (প্রথম CLK Pulse one) One না হলে পরের গুলো On হবে না।

Experiment: Design an asynchronus counter using 74.73

Lecture-4

26.1.26

$$T = \frac{N * CPI}{f}$$

f = hardware

CPI = Architecture

N = Software

Arch (CPI) এর সাথে T সম্পর্কিত

T বেশলে CPI বেশবে।

$T \propto CPI$

$(\uparrow)\ T \propto N(\uparrow)$

$(\uparrow)\ T \propto \frac{1}{f}\ (\uparrow)$

Soft, Archi, hardware,

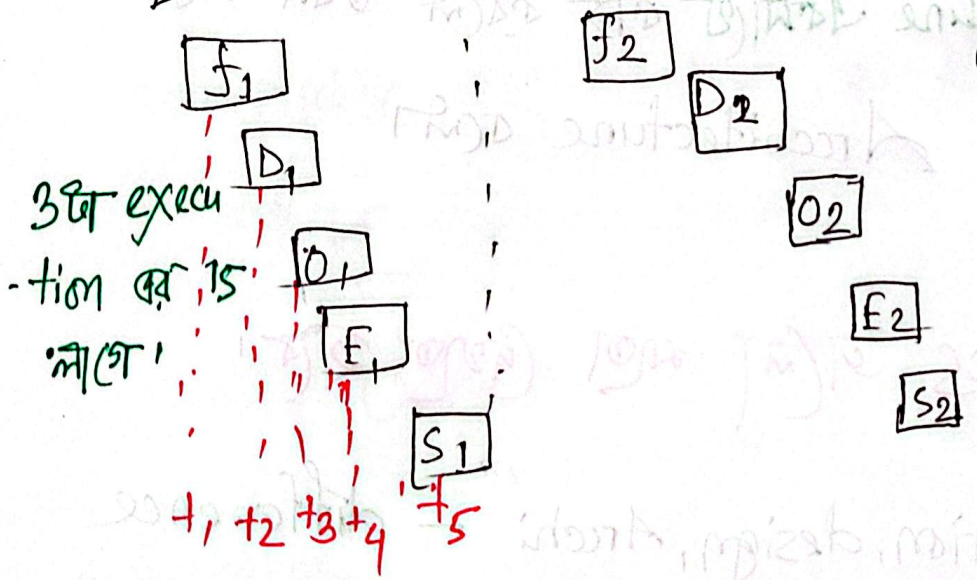
$\boxed{\text{Factors affecting performance}}$

Speedup techniques.

- Cache Memory : RAM এর সবচেয়ে কাছের অংশ।

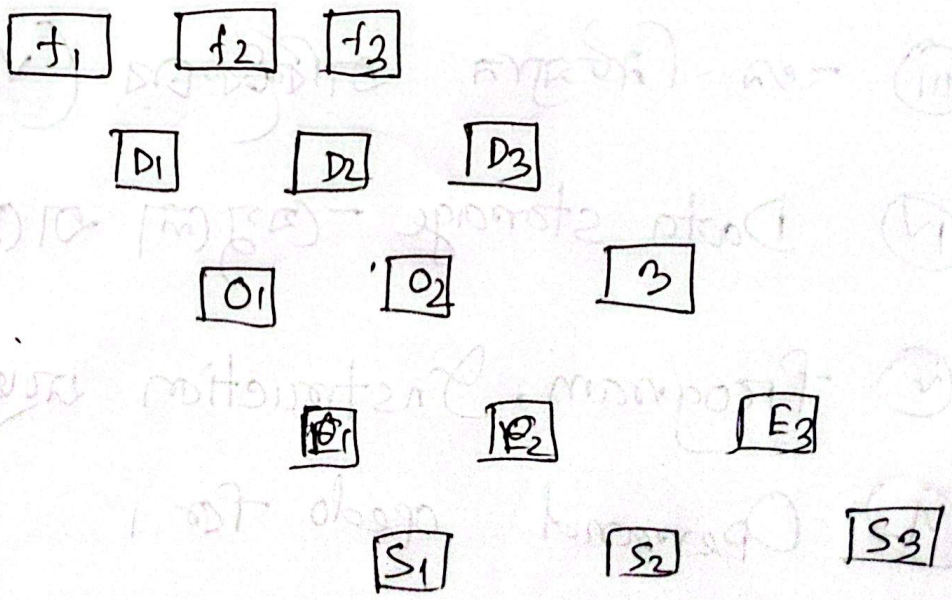
- Pipelining :

Non-pipelined: একটা শেষ না হওয়া পর্যন্ত আরেকটা শুরু হবে না।



(i) fetch
(ii) Decode
(iii) Operation
(iv) Execution
(v) Store

Pipelined :



Pipelining in Details

Row + instruction − 1 → formula

↓

Frame

Multiple pipeline একসাথে কাজ করলে তখন তাকে Superscalar Architecture বলে।

যেসব Topics ভালো মতো দেখতে হবে।

(i) Organization, design, Archi — difference

(ii) কেনো — এ সবার Archi. পড়বো

(iii) ভন-নিউম্যান আর্কিটেকচার (Van-Neuman)

(iv) Data storage — যেগুলো আছে।

(v) Program, Instruction সংগ্রহ

(vi) Operand পেতে কি।

(VI) Performance Metrice (সংজ্ঞা ব্যাখ্যা)

(VII) Measure

(VIII) Factors Affecting performance

(IX) Speed Techniques কিভাবে speed বাড়ানো,

(X) Pipeline, details

non-pipeline এবং Pipeline এর মধ্যে difference কে কতগুণ faster. বলেকিনু।

Processing Unit

$t_p \rightarrow$ pipeline

$t_n \rightarrow$ non-pipeline

$$S = \frac{n\, t_n}{(k+n-1)\, t_p}$$

K = Segment number (Phase সংখ্যা)

n = task numbers (কাজসংখ্যা)

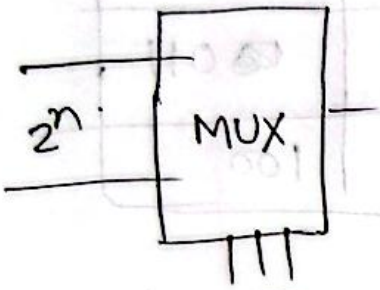
Non-Pipeline: এর ক্ষেত্রে যতগুলা segment Number
আছে এবং task number এর গুণফল -ই হবে
মোট times (t)

Pipeline:

Lecture - 5

02.02.2026

Processing Unit



(n) Selection line

Example

$R_1 \leftarrow R_2 + R_3$

$R_2 \leftarrow R_3 - R_1$

$R_3 \leftarrow R_2 * R_3$

$R_4 \leftarrow R_1 / 3$

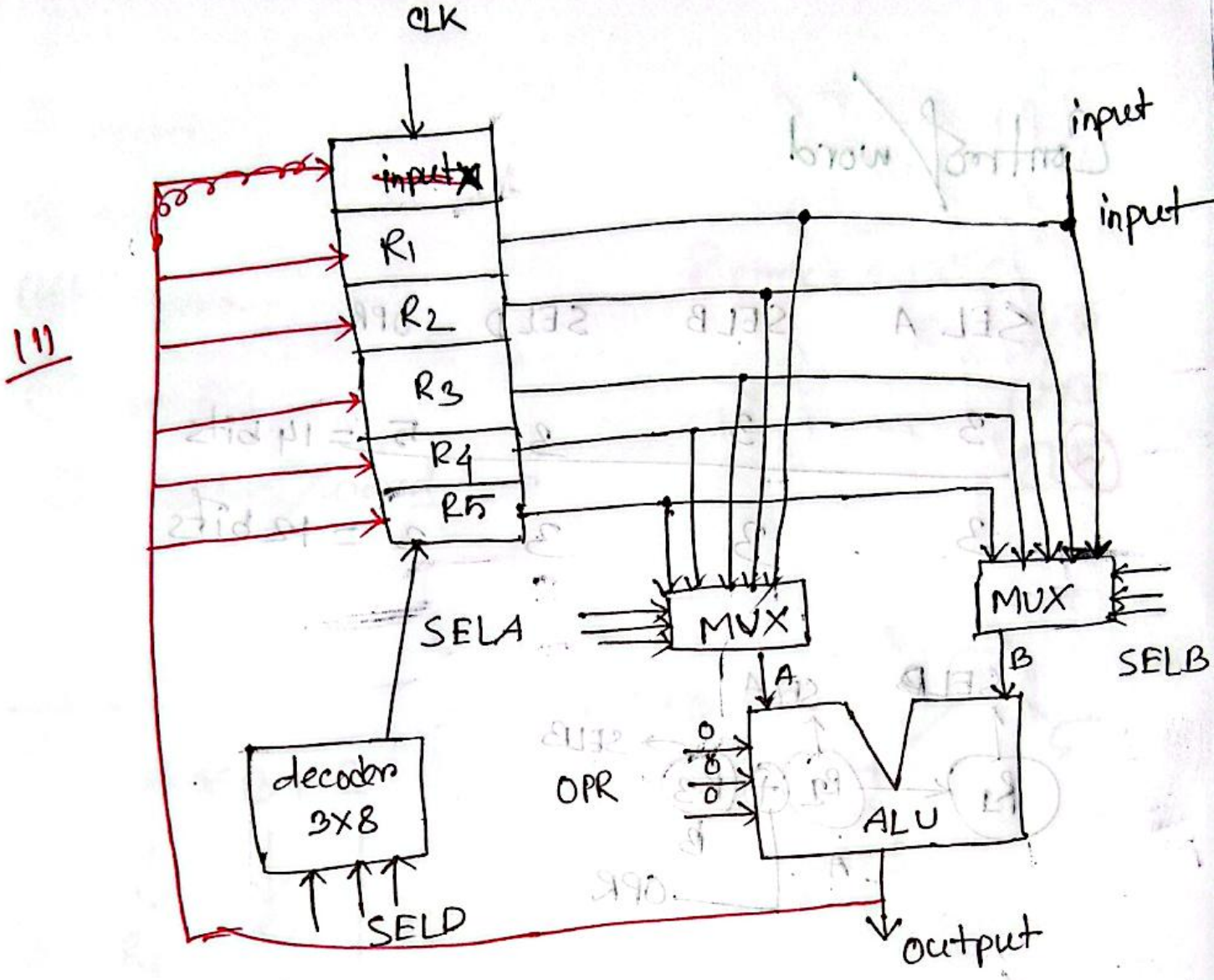
$R_5 \leftarrow R_1 \wedge R_3$

1

Reg	Address
input	000
R_1	0001
R_2	010
R_3	011
R_4	100
R_5	101

11

OPR	Address
+	000
−	001
×	010
/	011
^	100



Calculator

$\log_2 6 = 2.$ - -

$= 3$

Processing unit কিভাবে

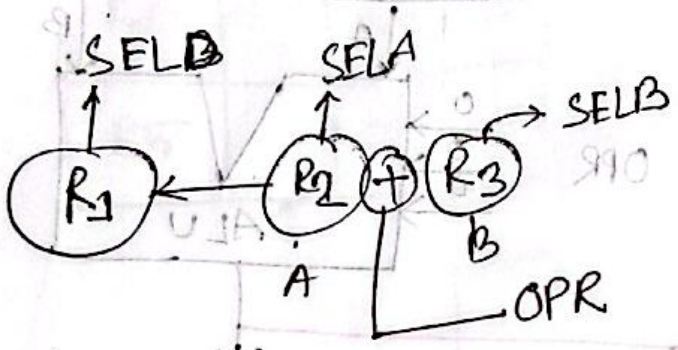
Process করে।

instruction অনুযায়ী

Control word

SEL A	SEL B	SEL D	OPR
3	3	3	5 = 14 bits
3	3	3	3 = 12 bits

(W)



$R_1 \leftarrow R_2 + R_3$ ~~010~~ 011

010	011	001	000

$R_2 \leftarrow R_3 - R_1$

011	001	010	001

$R_4 \leftarrow R_3 / 3$

011	000	100	011

(i) Register

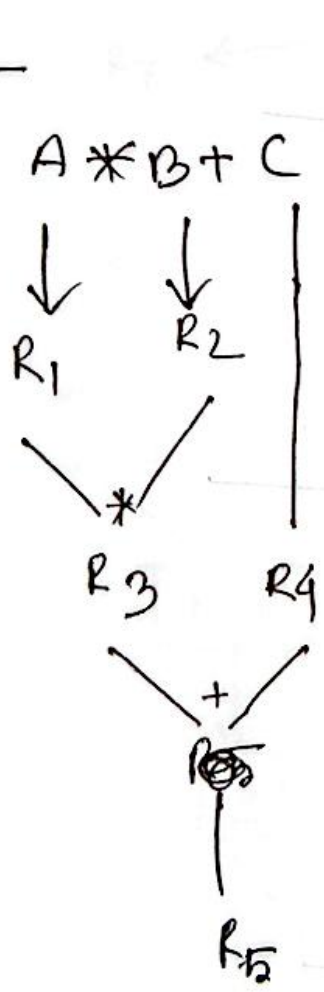
(ii) DPR

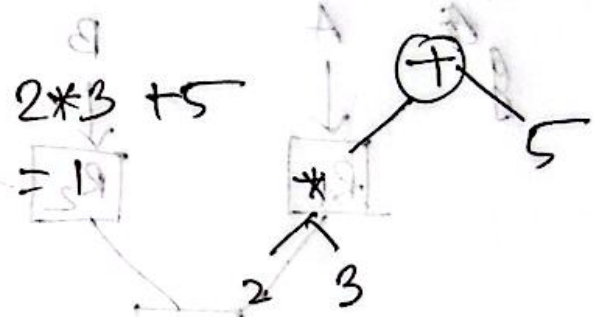
(iii) Figure

(iv) কাজ চিত্র

(v) Control/word

R++ থাকলে R+1 বুঝে নিতে হবে





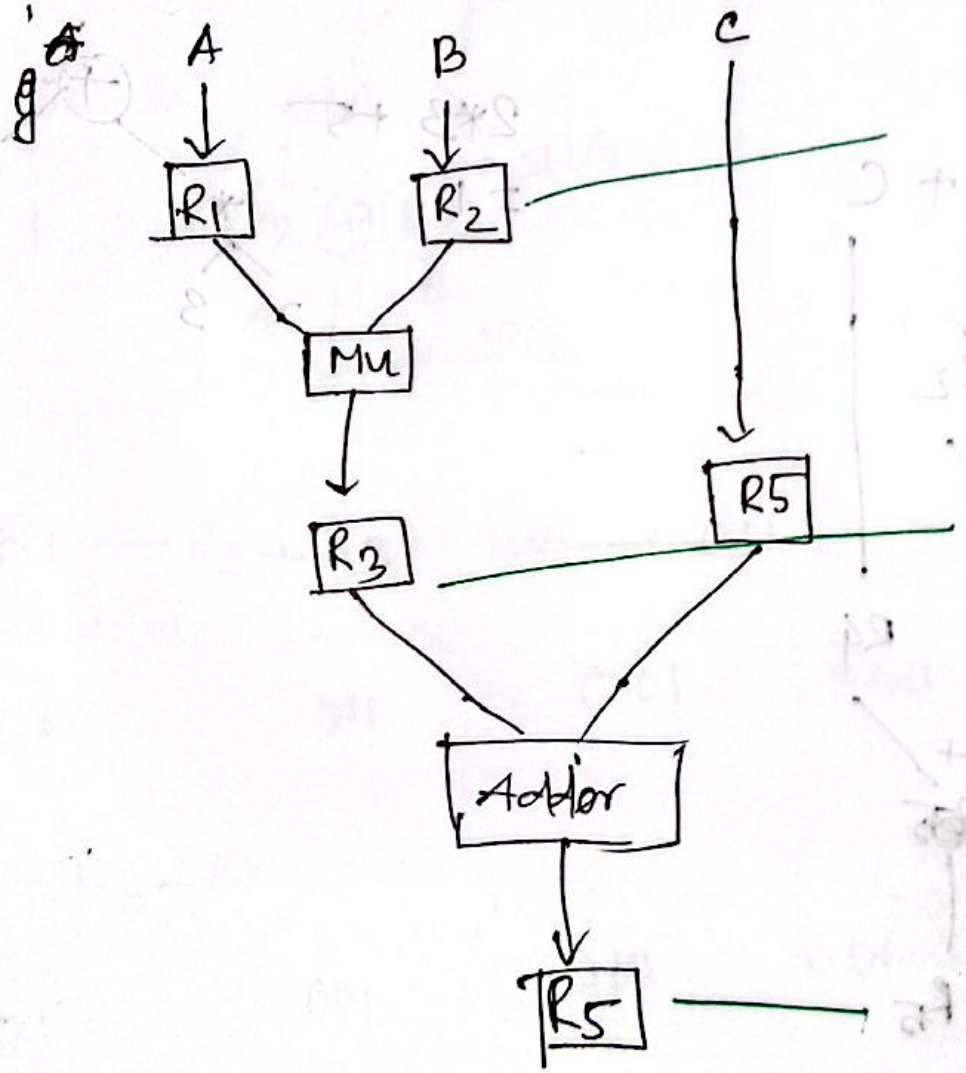
$R_1 \leftarrow A$

$R_2 \leftarrow B$

$R_3 \leftarrow R_1 * R_2$

$R_4 \leftarrow C$

$R_5 \leftarrow R_3 + R_4$



A * B + C * D

$R_1 \leftarrow A$

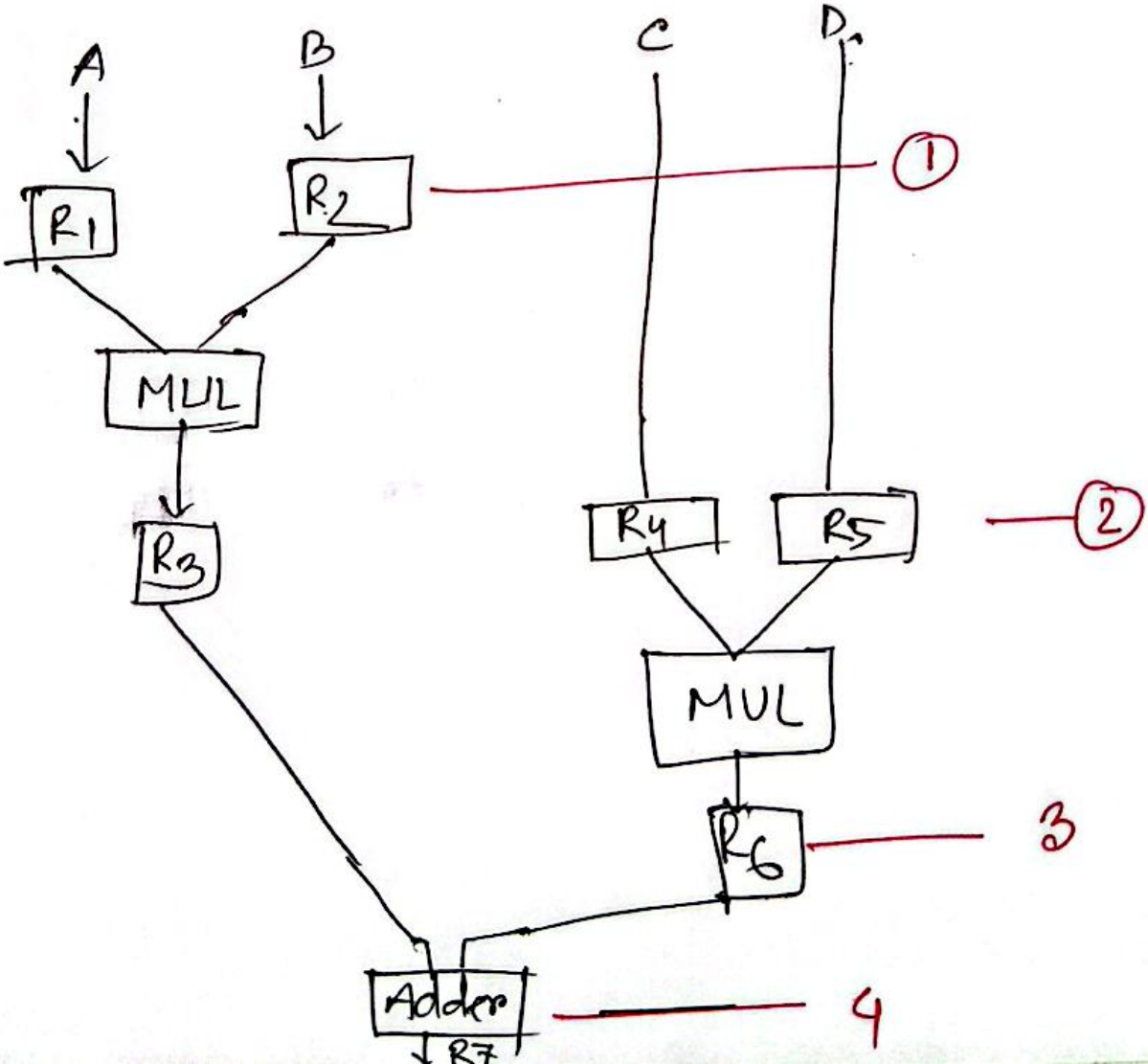
$R_2 \leftarrow B$

$R_3 \leftarrow$ ~~A*B~~ $R_1 * R_2$

$R_4 \leftarrow C$

$R_5 \leftarrow D$

$R_6 \leftarrow R_4 * R_5$

$R_7 \leftarrow R_3 + R_6$

4 step