

Lecture - 1

Semi-conductor (অর্পণবিদ্যী)

insulator - অগ্রিবাহী

conductor - পরিবাহী

এইচু মাঝে semi-conductor
মাজের সংজ্ঞা

single crystal

negative temperature co-efficient - (inverse)

doping বেকুর semi-conductor এর conductivity
বৃদ্ধি বা কমানো যাব।

most used semiconductor material - Silicon, Germanium

Energy Level: (imp) v.v.

conduction level: current flow কৃত হয়,

পরম্পরা অমান্য বলুন semi-conductor insulator হয় শব্দ।
(ক্ষেত্রের ক্ষেত্র ক্ষেত্রের দ্রুতি, energy level দিয়ে explain)# movement এক ইল নিচে যাব খেক পেতে পেতে গোড়া
খেতে পাবে না।

room temperature - 25°C

0 kelvin / -273.15° සිලිකෝන් ක්‍රිස්ටලය මැඟි

e⁻ pass තහවුරු room temp. - අ පිළි දෙනු

energy gain



breaking covalent band (මගුදාලු තුළුව)



Free electron



moveable electron

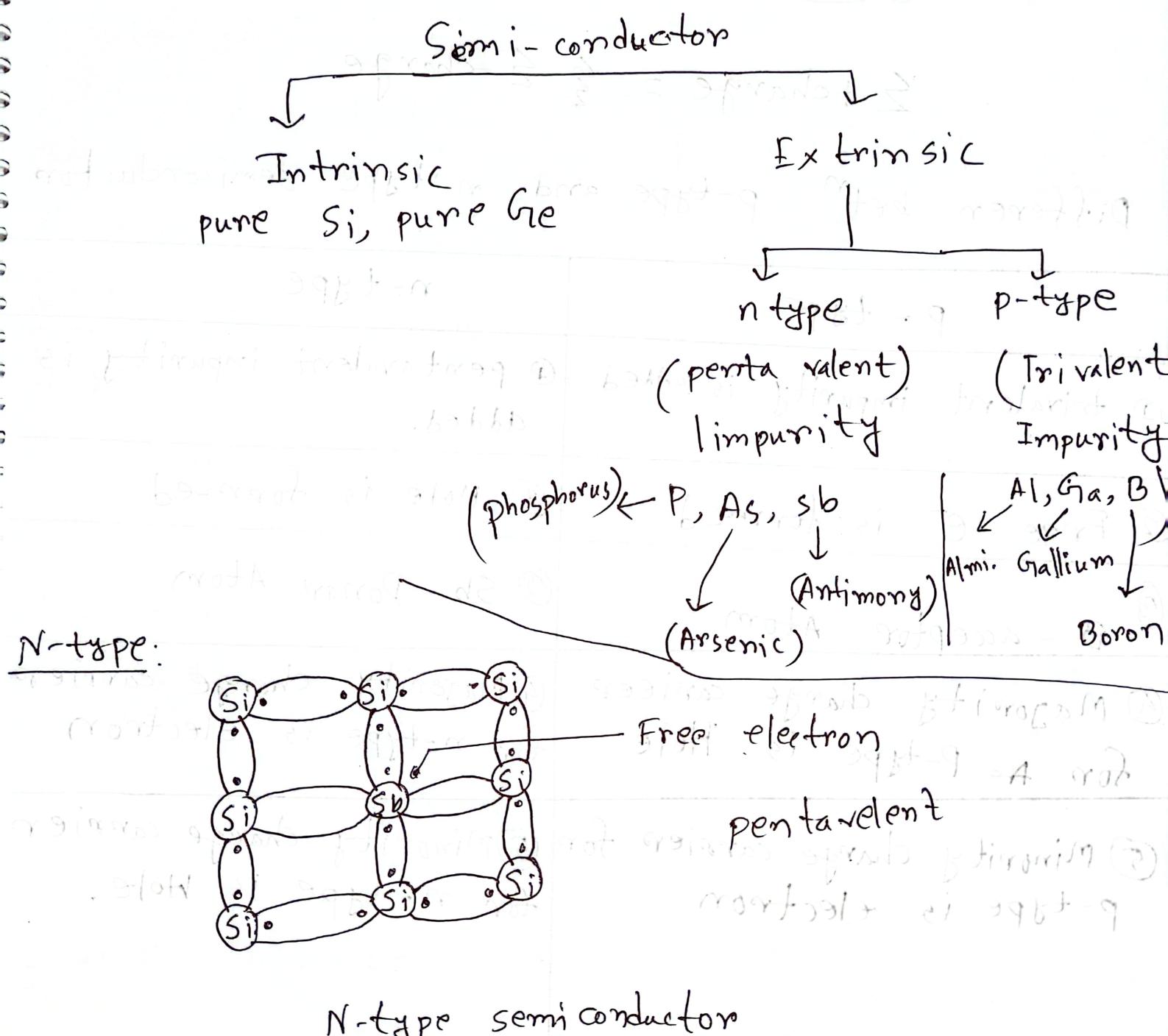
pentavalent - මෙය තුළුදාලු ප්‍රති තුළුවන - ප්‍රතිග්‍රීහ ප්‍රතිඵලි

anion (N-type)

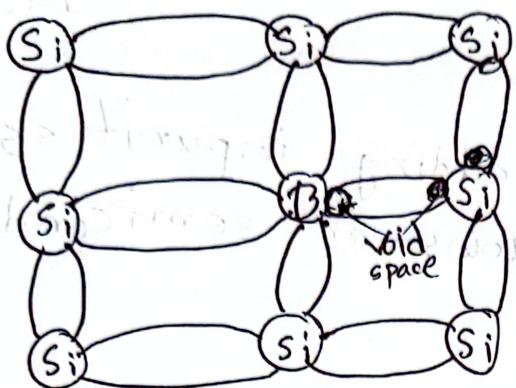
trivalent - ප්‍රතියාංශ (P-type)

Valence Band, Conduction Band, Forbidden Energy Gap.

Doping: The process of adding impurities to intrinsic semiconductors known as semiconductors.



P-type



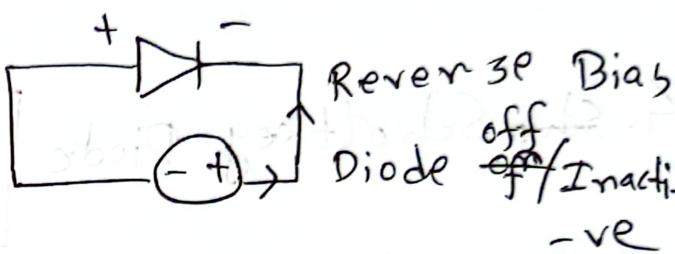
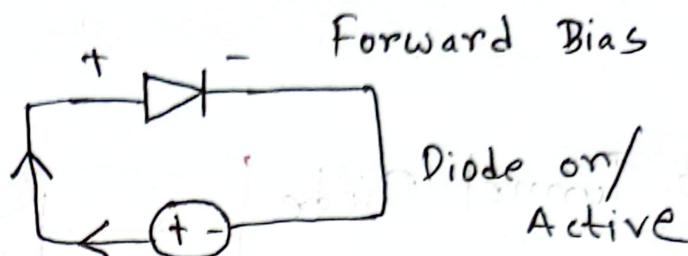
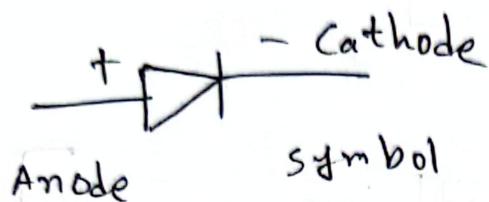
Al
Hole (state)

$$\Sigma +\text{charge} = \frac{1}{2} \Sigma -\text{charge}$$

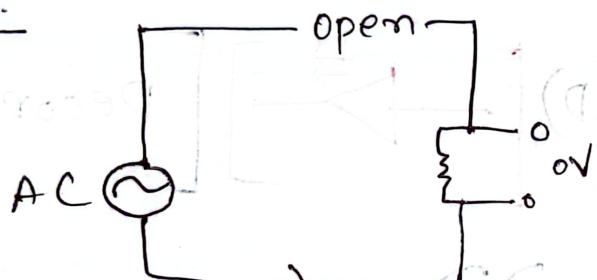
Difference betⁿ p-type and n-type semiconductor

p-type	n-type
① trivalent impurity is added	① pentavalent impurity is added.
② Free e^- is formed	② Hole is formed
③ B - acceptor Atom	③ Sb - Donor Atom
④ Majority charge carrier for P-type is Hole	④ Majority charge carriers for n-type is electron
⑤ Minority charge carriers for p-type is electron	⑤ Minority charge carriers for n-type is hole.

Diode: Diode is a two terminal device that allows current to flow in only one direction and blocks current coming from opposite direction.



Rectifier:



EEE1231

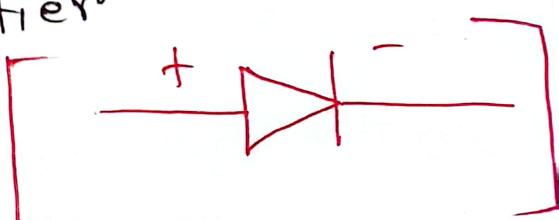
Lecture - 3, 4

25. 08. 2024

25. 07. 2024

Classification of Diode

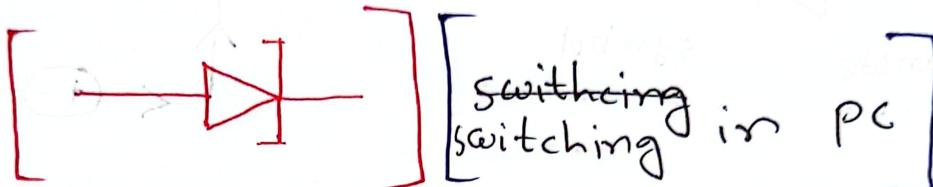
1. p-n Junction diode/ rectifier



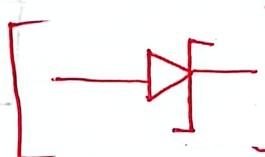
2. Zener Diode [stabilizer & voltage regulator স্টেবিলাইজার এবং ভৱেজার]



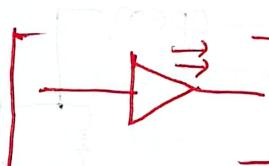
3. Tunnel Diode [switching in PC]



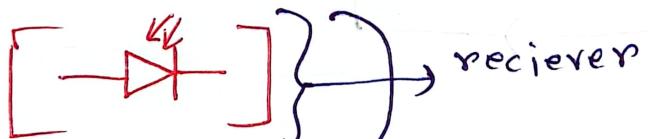
4. Schottky Diode [high frequency and high speed operation]



5. Light Emitting Diode (LED) [Decoration]



6. photo Diode



reciever

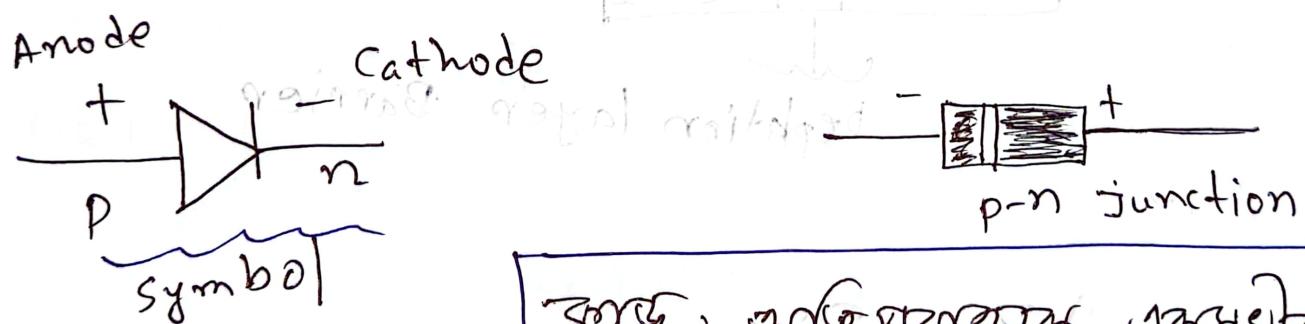
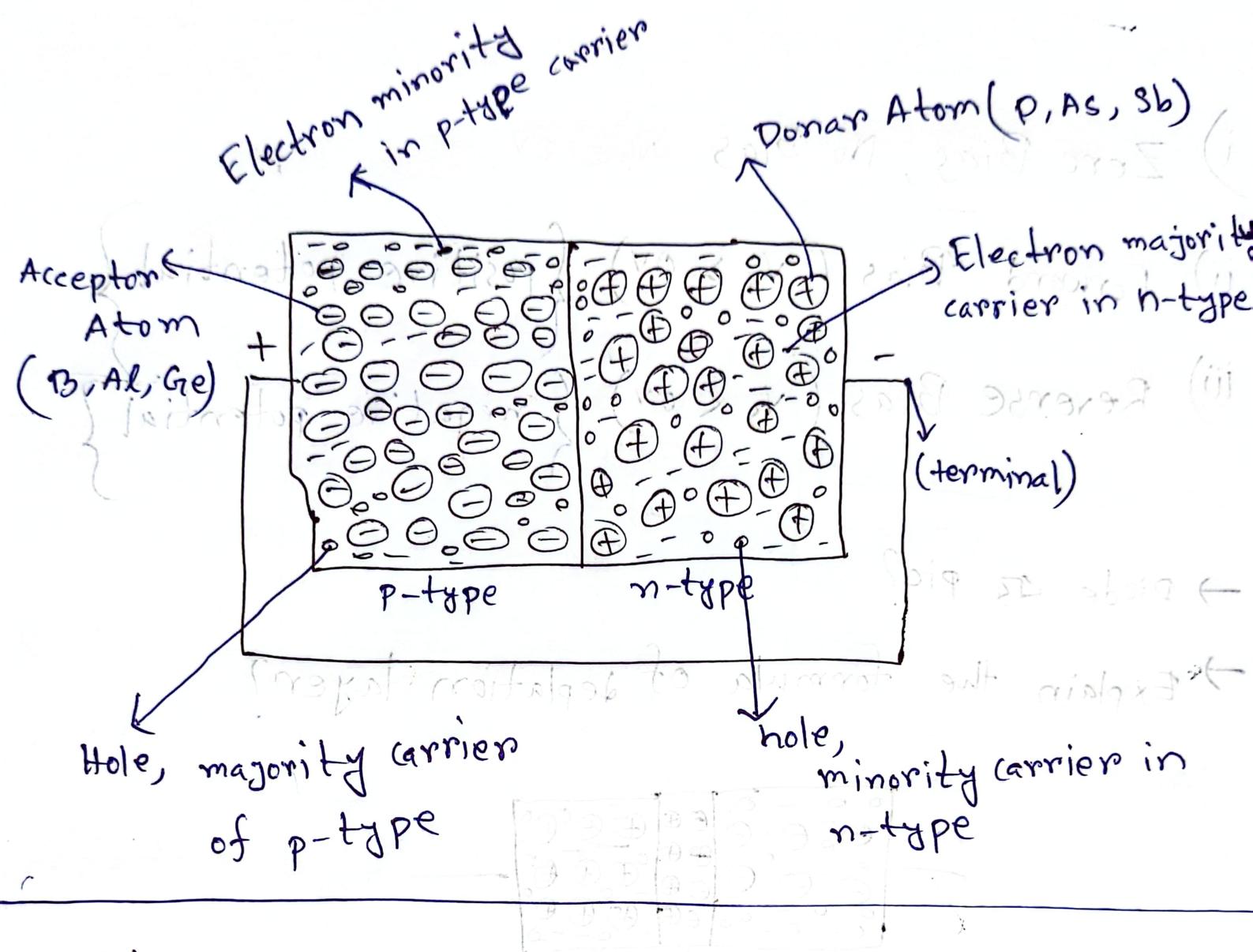
7. IR8 Diodes



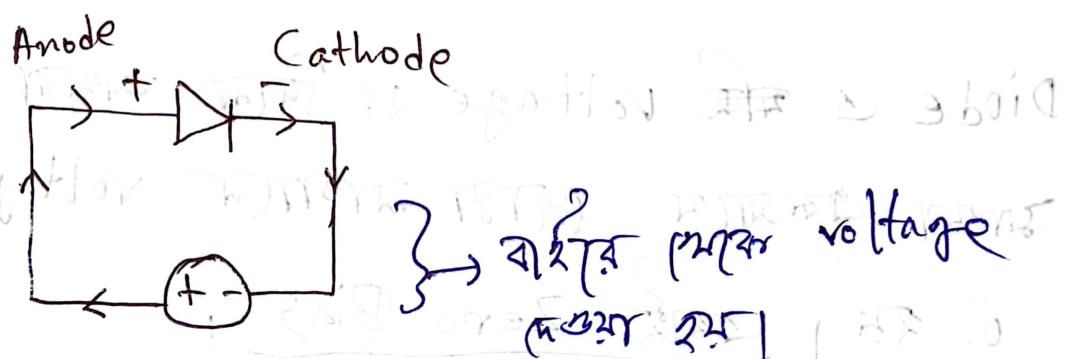
used as a pair in pulse oximeter

transmitter

Internal Structure of Diode



বাই: অতিপ্রযোগ্য একক্ষণীয়তা



Biassing in Diode

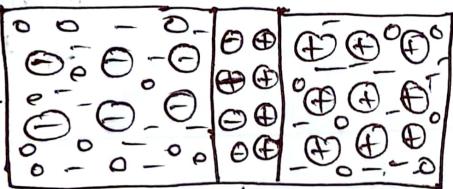
i) Zero Bias, No Bias $V_s = 0V$

ii) Forward Bias ($V_s > 0V$) {positive potential}

iii) Reverse Bias ($V_s < 0V$) {negative potential}

→ Diode ഏ പി?

→ Explain the formula of depletion layer?



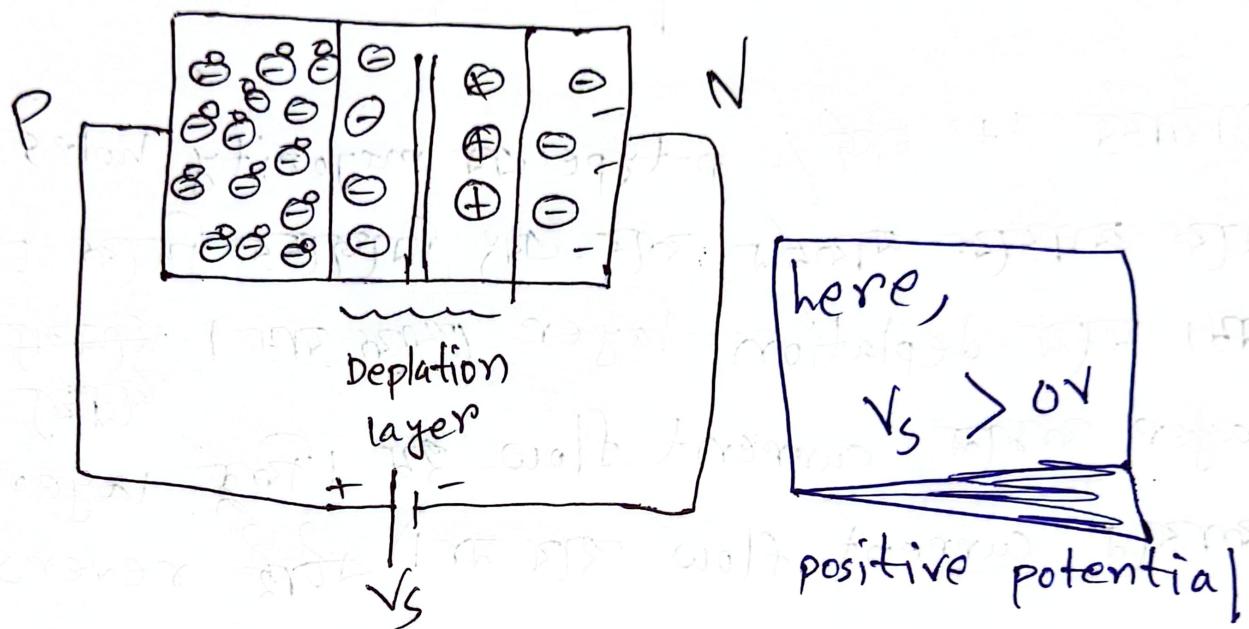
Depletion layer Barrier

i) Zero Bias

Diode എ വോല്ടേജ് നു തിരികെടുത്ത് അഥവാ കൂടിപ്പിക്കുന്ന ഒരു വായ്യേരം മാറ്റുള്ള പ്രസ്താവനാണ് വോല്ടേജ് 0 എംബ് current 0 എംബ് ചുരുക്കം എന്നും പറയുന്നു.

ii) Forward Bias:

Diode - এব় (+) প্লাটের মাধ্যমে কার্ডিভিং (+) প্লাট ও Diode
 এব় (-) প্লাটের মাধ্যমে কার্ডিভিং (-) প্লাট মুক্ত হয়ে।



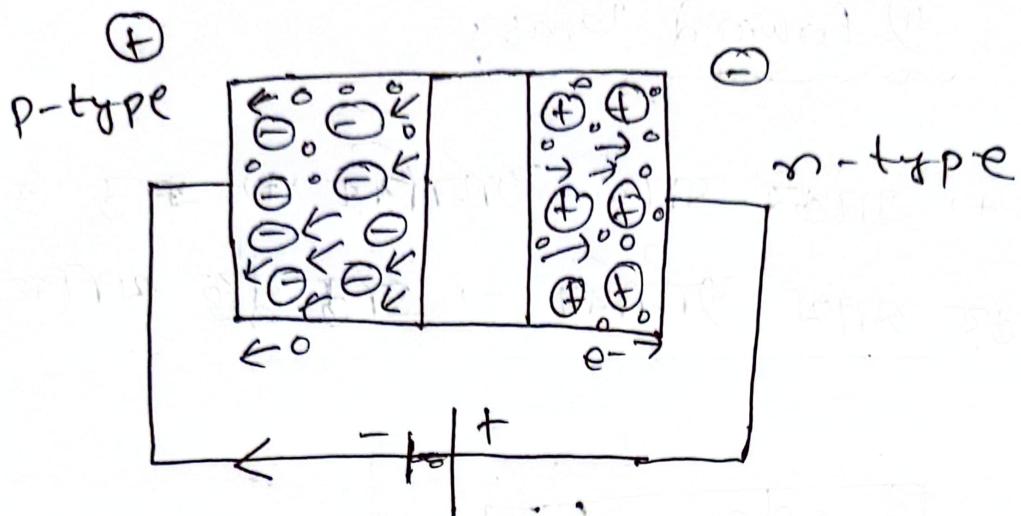
Depletion layer মধ্যে প্রবাহিত current flow

p-n junction \rightarrow forward Bias \rightarrow সুষ্ঠি current flow

ব্যবহা

iii) Reverse Bias:

এখন, $V_s < 0V$



বাটারির '+' চৰ্দ / - p-type এৰ majority holes পুলোৱা (+)
একে আপৰকে আকস্মাৎ কৰে এখন নিষ্ঠায়ের দ্বিতীয় চৰ্দ হৈন
মেয়। ফলত depletion layer থাকিব। কৃত্য deplation
layer অমূল current flow হৈব। ফিল্ট layer গড়া
কৰিব। current flow থাকিব। এটুই reverse bias.

p-n junction কৰি : forward bias-এ কোণ কৰিব।

Graph of p-n junction diode with forward bias

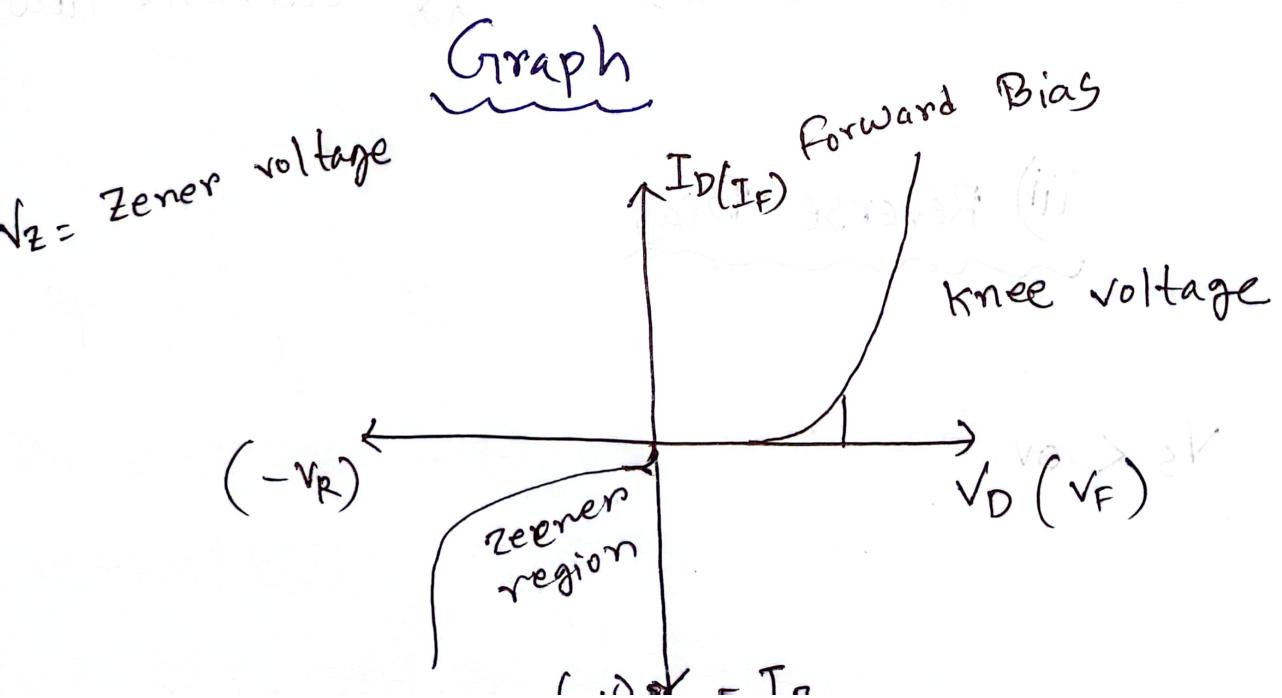


Fig: VI characteristic curve of a p-n junction knee voltage. The minimum amount of voltage for which current through a diode starts rising rapidly.

minority charge carrier depends on temperature
that's why ^{through} reverse bias, minority current does flow.

Zener reverse diode (मात्र बिट्टा)

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Semiconductors

Lecture-5
1-9-2024

Effect of temperature on Ge Diode

$$1. \left\{ \begin{array}{l} 200^\circ C \rightarrow Si \text{ (P-n)} \\ 200^\circ C \rightarrow Ge \text{ (Zener)} \end{array} \right.$$

$$2. \left\{ \begin{array}{l} \text{Breakdown voltage } Si = 2000V \\ Ge = 400V \end{array} \right.$$

$$3. \left\{ \begin{array}{l} \text{Silicon is more available and cheap than Ge} \end{array} \right.$$

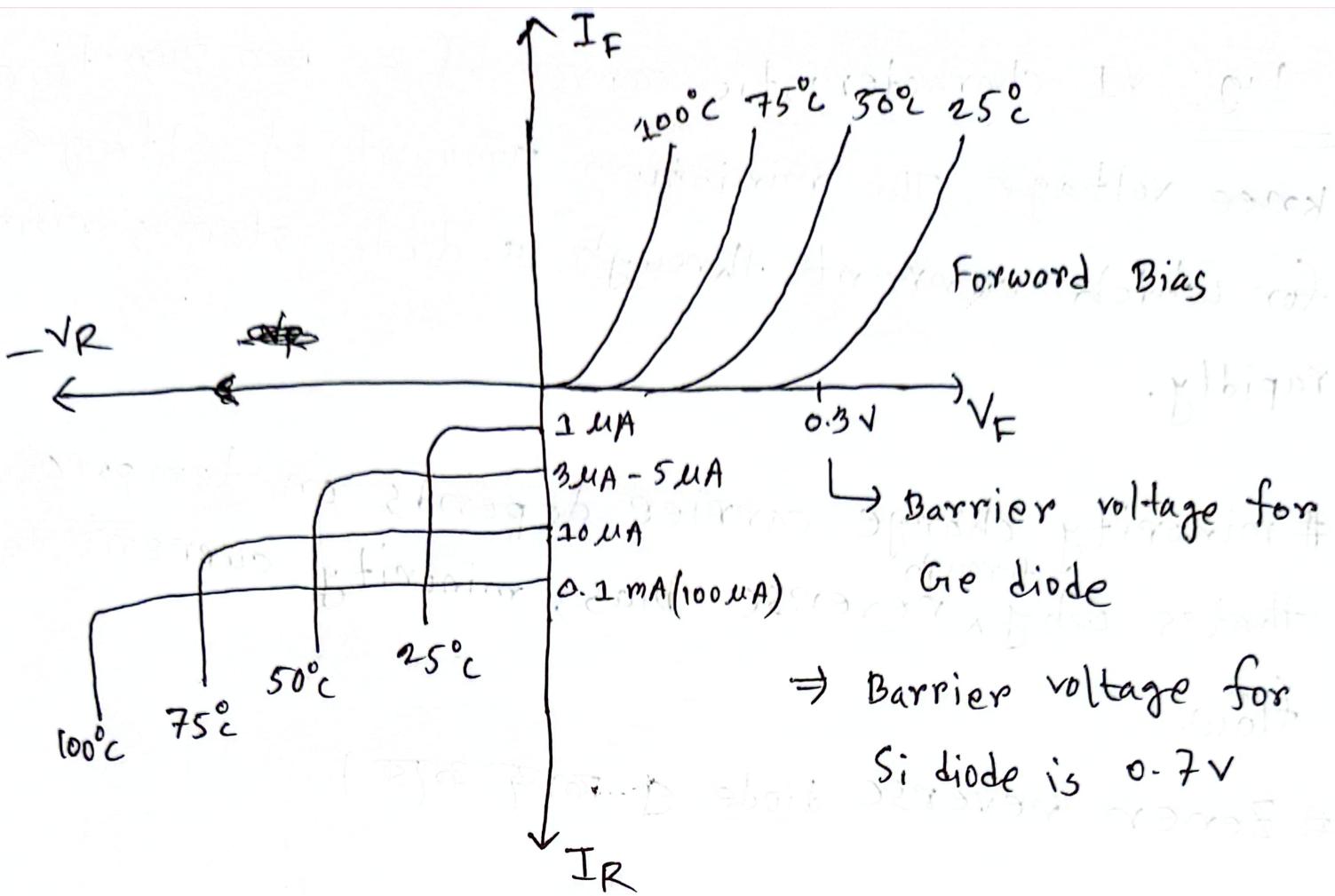
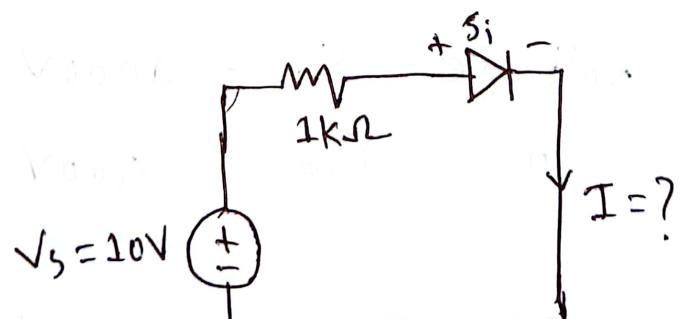


Fig : 1.24 (Book)

With the increase of temperature forward bias characteristics for of a Ge diode becomes more ideal

Math Part

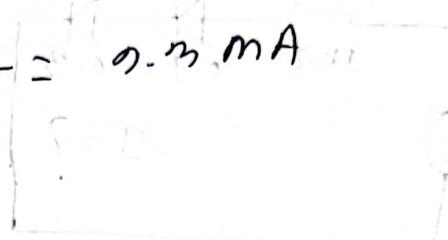


Two condition:

1. Supply voltage, $v_s > 0.7$?
2. Diode ~~is~~ direction forward bias?

method - 1:

$$I = \frac{10 - 0.7}{1k\Omega} = 0.3 \text{ mA}$$

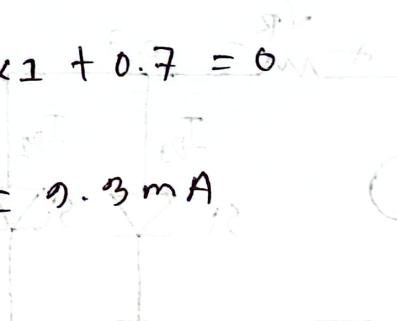


method - 2: Applying KVL,

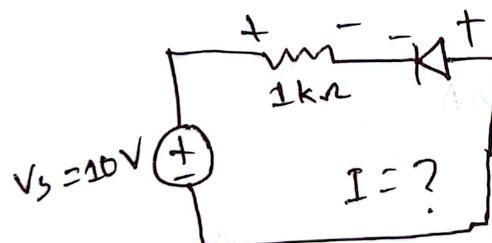
$$-10V + v_R + 0.7 = 0$$

$$\text{or, } -10 + I \times 1 + 0.7 = 0$$

$$\text{if } I = \frac{10 - 0.7}{1k\Omega} = 0.3 \text{ mA}$$



Type: 2

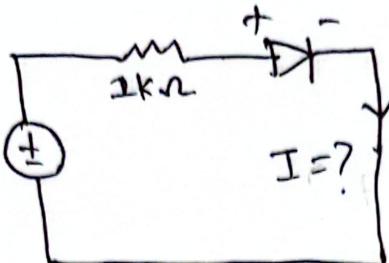


Hence diode is attached in opposite direction with v_s , that's why it is an open circuit.

$$\therefore I = 0$$

Type-3

$$V_s = 0.5 \text{ V}$$

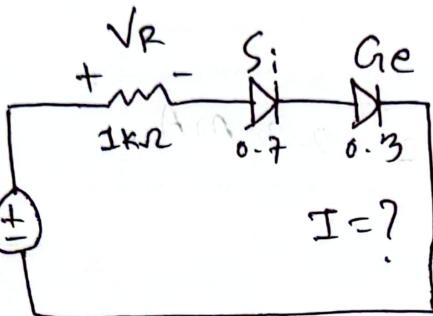


$$V_s < 0.7$$

So... diode will not active, Hence $V_s < 0.7$

Type-4

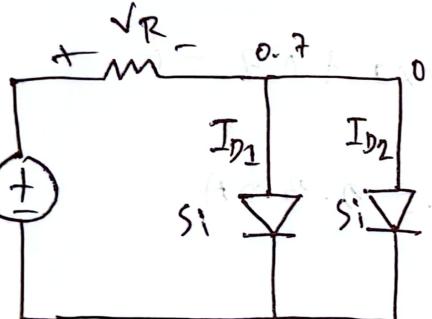
$$V_s = 10 \text{ V}$$



$$\therefore I = \frac{10 - 0.7 - 0.3}{1 \text{ k}\Omega} = 0 \text{ mA}$$

Type-5

$$V_s = 20 \text{ V}$$

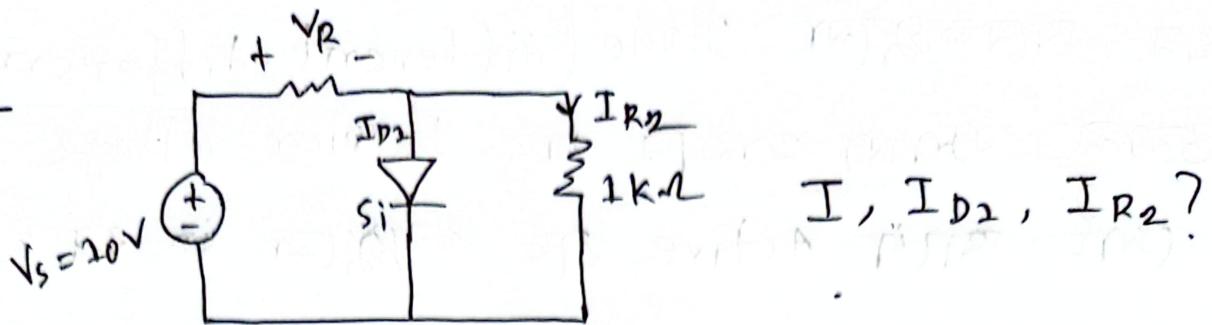


Calculate I, I_{D1}, I_{D2}

Here, $I = \frac{20 - 0.7 - 0.7}{1 \text{ k}\Omega} = 18.6 \text{ mA}$

Now, $I_{D1} = I_{D2} = \frac{I}{2} = 9.3 \text{ mA}$

Type-6



Here, $I = \frac{10 - 0.7}{1} = 9.3mA$

$$V = IR$$

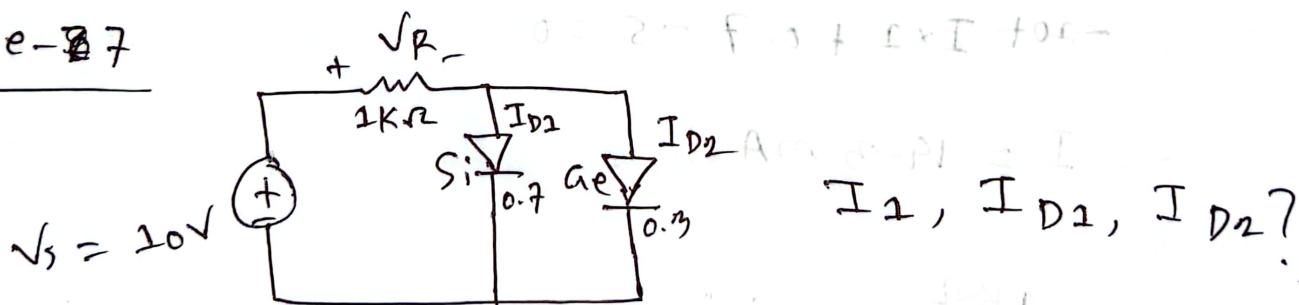
$$I_{R2} = \frac{V}{R} = \frac{0.7}{1} = 0.7mA$$

Applying, KCL, $I = I_{D1} + I_{R2}$

$$\text{or, } I_{D1} = (9.3 - 0.7)mA$$

$$= 8.6mA$$

Type-7



এখন, Ge এর voltage 0.3V হলে Ge এর diode

কার্য active তথ্য, $I = I_{D2} = \frac{10 - 0.3}{2} = 4.7mA$

$$I_{D2} = 0$$

$$\therefore I_{D2} = 0.7mA$$

ଯଦ୍ବା ଅନେକତାରୀ Diode (different different)
ଯମାନ୍ତରାନ୍ ସ୍ଥାନ୍ ଖଳାରୀ ମାର୍ ବରି ଲୋକୁ
କହୁ ଓଟି ଆଗ୍ରା ଏବେ ଅନ୍ଧାରୀ କାହାରୀ ପରିଷ୍ଠା

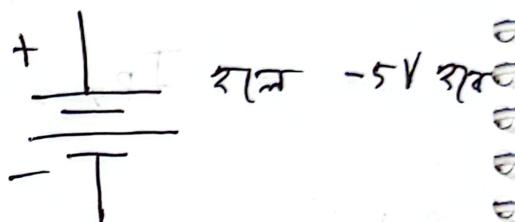
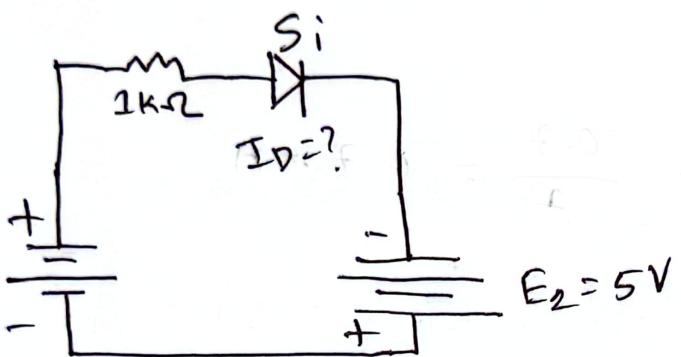
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Math Part

Lecture-6

02.09.2024

Q.1



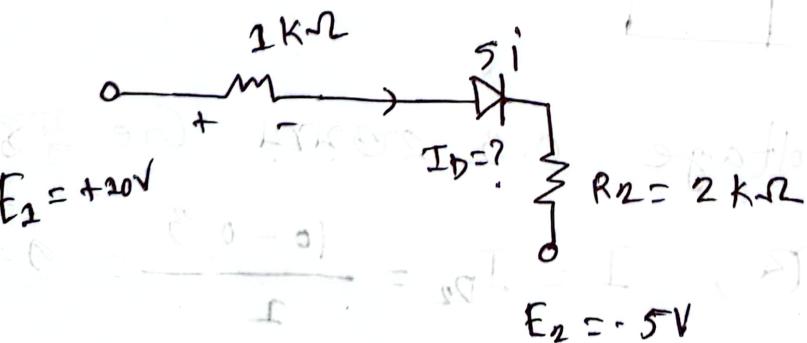
$$I = \frac{20 + 5 - 0.7}{1} = 19.3 \text{ mA}$$

Applying KVL,

$$-20 + I \times 1 + 0.7 - 5 = 0$$

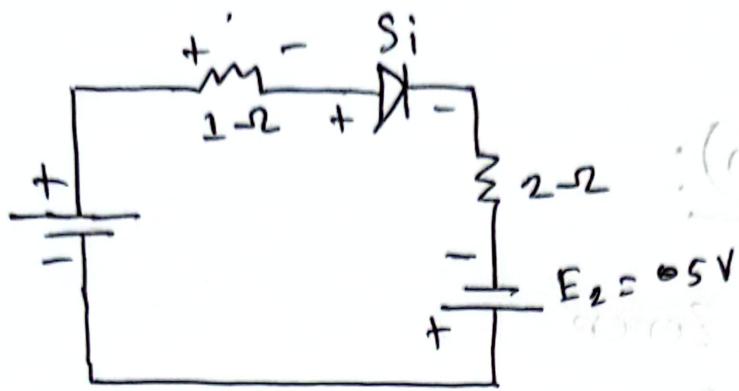
$$\therefore I = 19.3 \text{ mA}$$

Q.2



$$A = R_2 / (R_1 + R_2) = \frac{20 - 5}{1 + 2} = 10 \text{ mA}$$

$$A = 10 \text{ mA}$$



Applying KVL,

$$-20 + I \times 1 + 0.7 + 2 \times I - 5 = 0$$

$$\text{or, } I + 2I = 14.3$$

$$\therefore I = 4.767 \text{ mA}$$

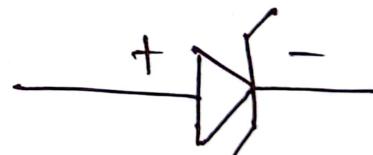
Zener Diode

Sathya Chennai India

⇒ Heavily doped

⇒ Thin depletion layer

⇒ $(1.8 - 200)\text{V}$ doping এবং পোর্ট ফিল্ড



⇒ 5.5V (জ্যাব মেট্রিক স্কেল)



মাত্র doping করণের উন্নত charge carrier বাড়ায়।

এবং ফল Depletion layer প্রতির শুধু মাত্র। এবং

Breakdown voltage ১৩৮২১

operation (3 region):

① In forward bias Zener

diode behave as a forward
p-n diode

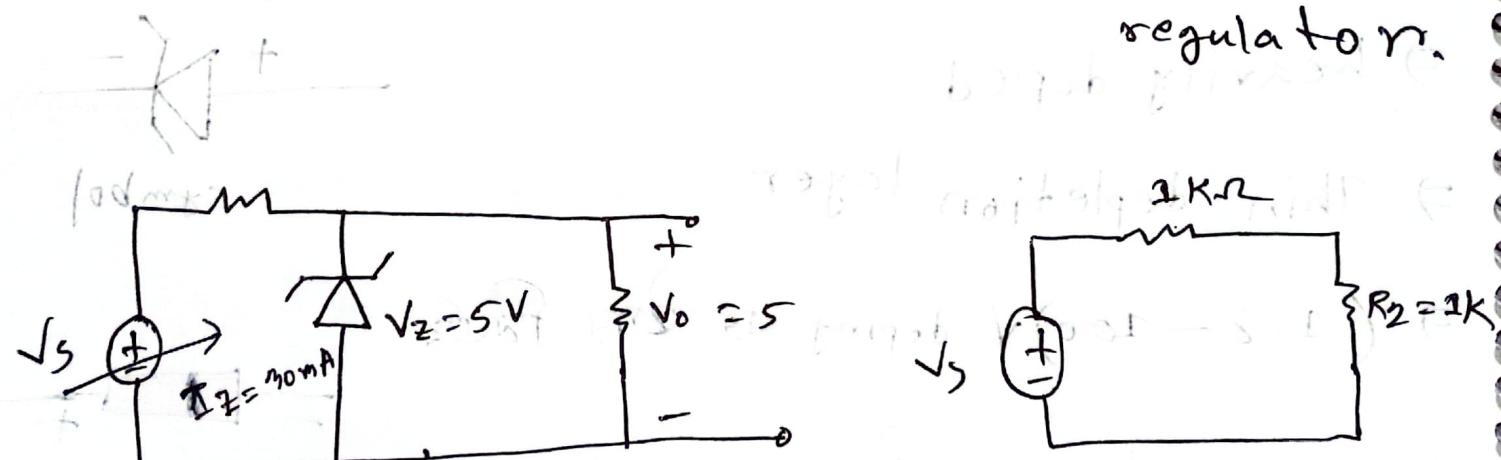
② During reverse Bias $V_Z = 5V$,

when, $V_D < V_Z$, diode will be open circuited

③ During Reverse Bias

when $V_D > V_Z$, diode will work as a voltage

regulator.

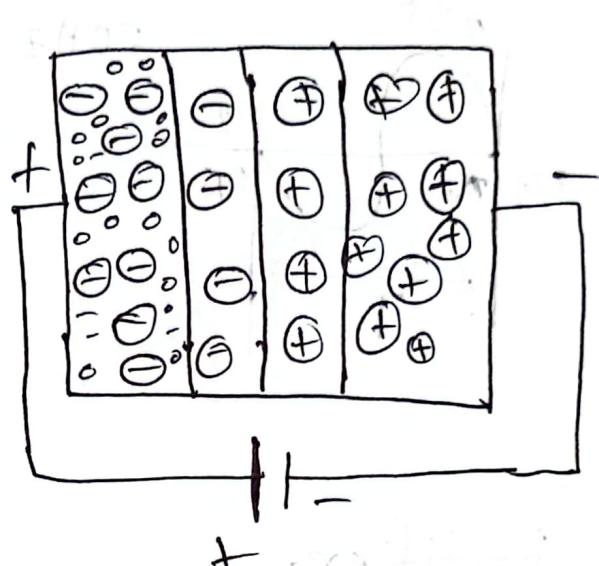
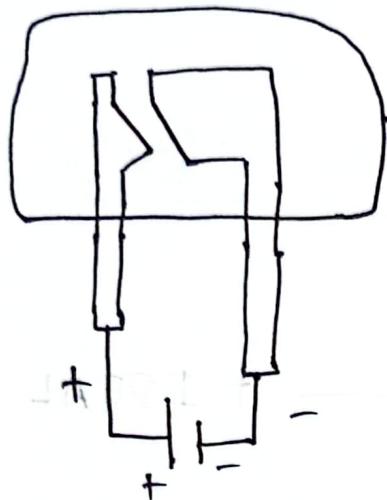


$$2V = V_{R_2} = \frac{1}{2+1} = \frac{1}{3}$$

0.5 < V_Z circuit open

LED (Light Emitting Diode)

→ Emits light when energised.



$$E_g = \frac{hc}{\lambda} \rightarrow 400 - 700 (\text{nm})$$

Materials → GaAsP, GaP

→ Define Electroluminescence?

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Lecture - 8

Application of Diode

09.09.2024

1. Rectifier circuit

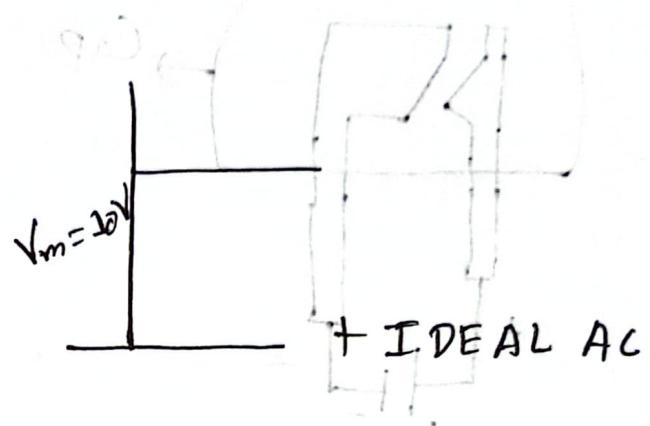
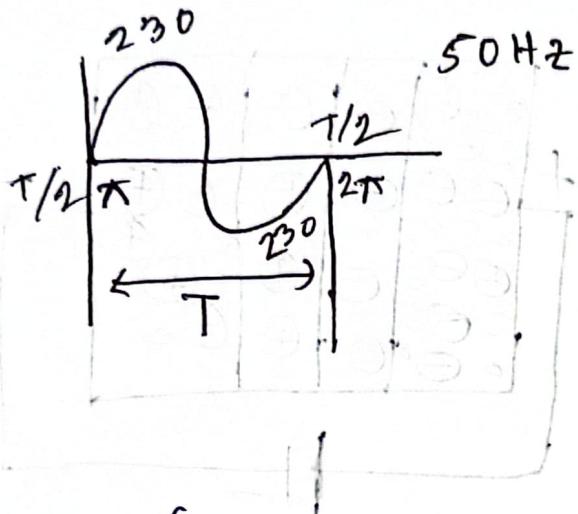
2. clipper

3. clamper

} → wave shaping circuit

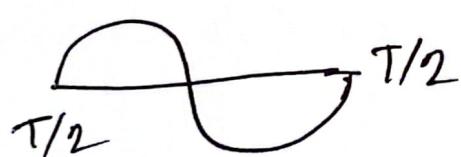
Rectifier

A device that converts AC into DC.



Types of Rectifier:

1. Half Wave Rectifier

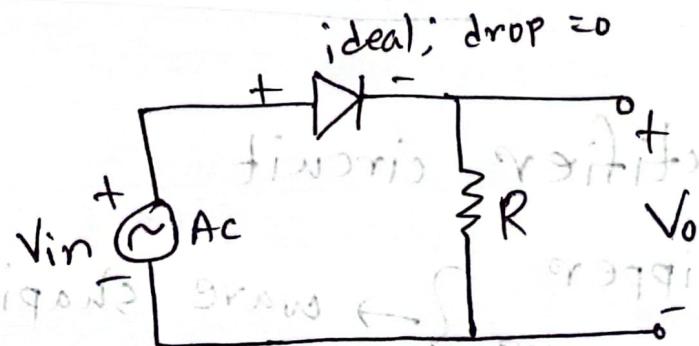


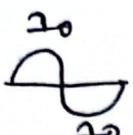
2. Full Wave Rectifier



Half Wave Rectifier

When diode positive,



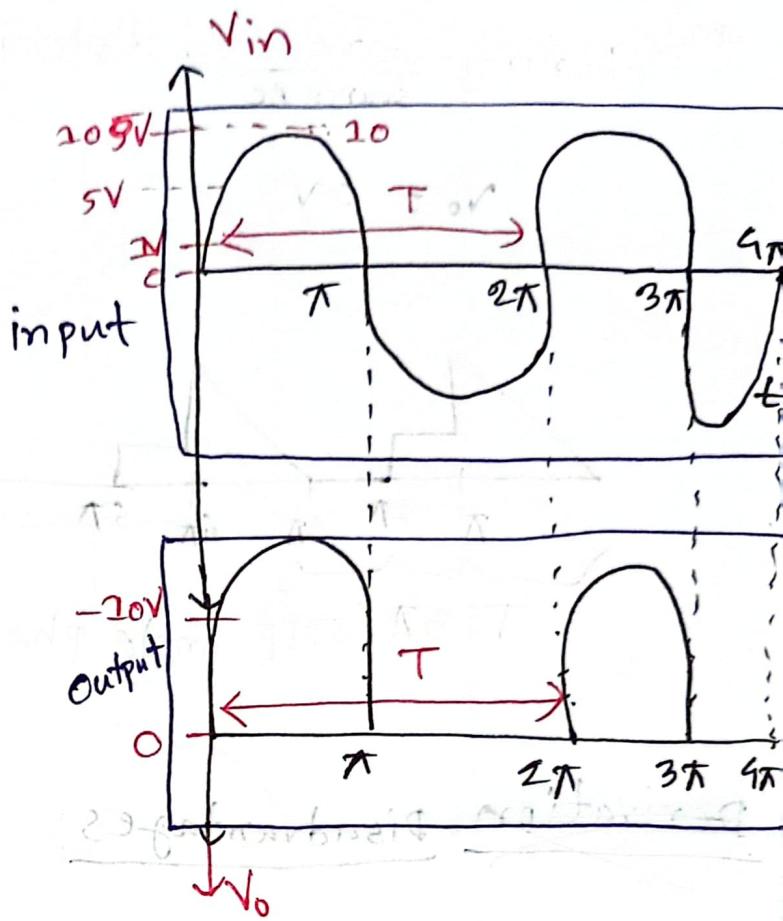
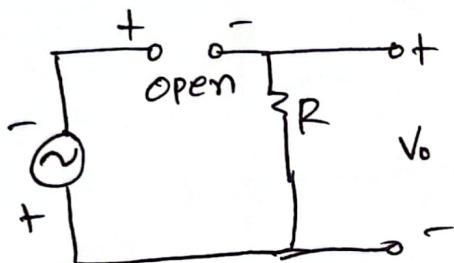
 During $\frac{(+)\text{ve}}{\text{source AC}}$ half,

Diode is active,

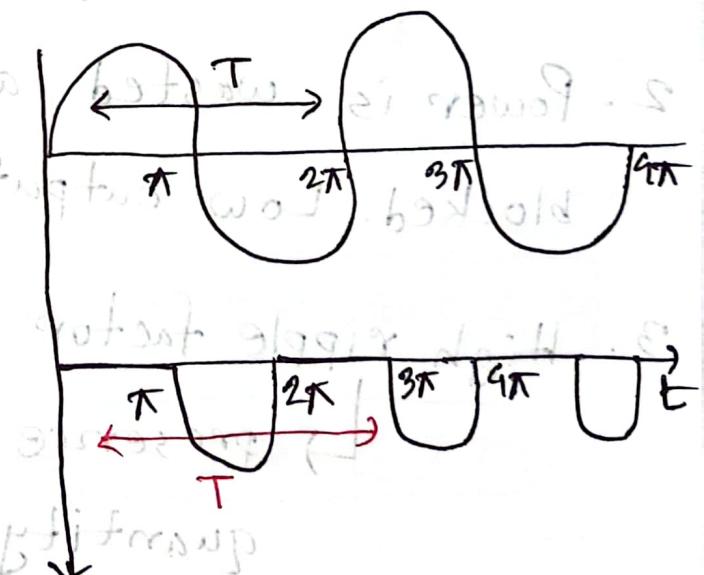
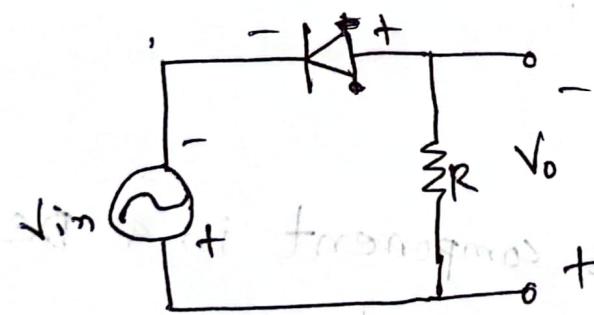
$$\therefore V_o = V_{in}$$

During $\frac{(-)\text{ve}}{\text{source AC}}$ half, diode is open

$$\therefore V_o = 0V$$



During $\frac{(+)\text{ve}}{\text{source AC}}$ half, diode is negative,



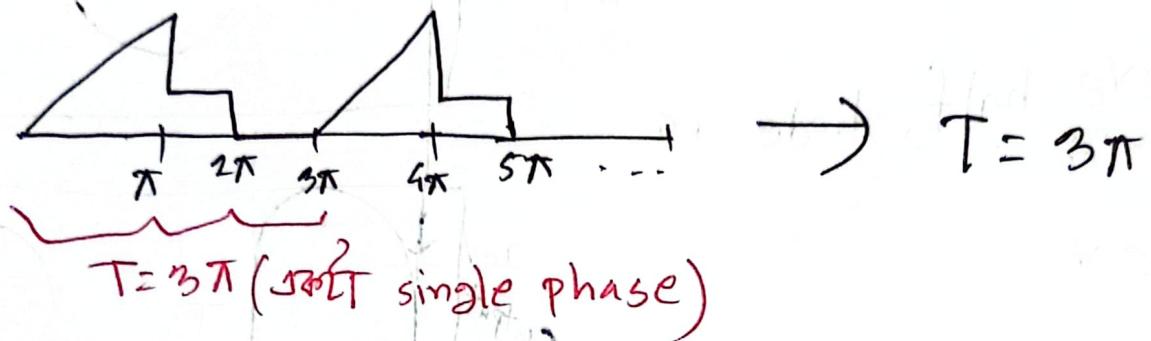
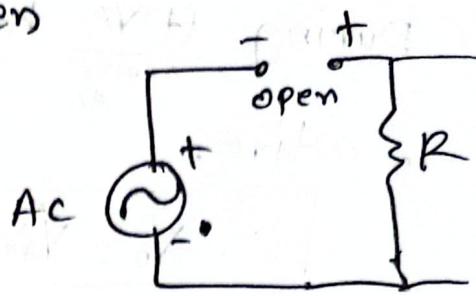
During $\frac{(-)\text{ve}}{\text{source AC}}$ half, diode is active

$$T = 2\pi$$

$$\therefore V_{in} = V_o$$

and, During (+)ve source AC, diode is open

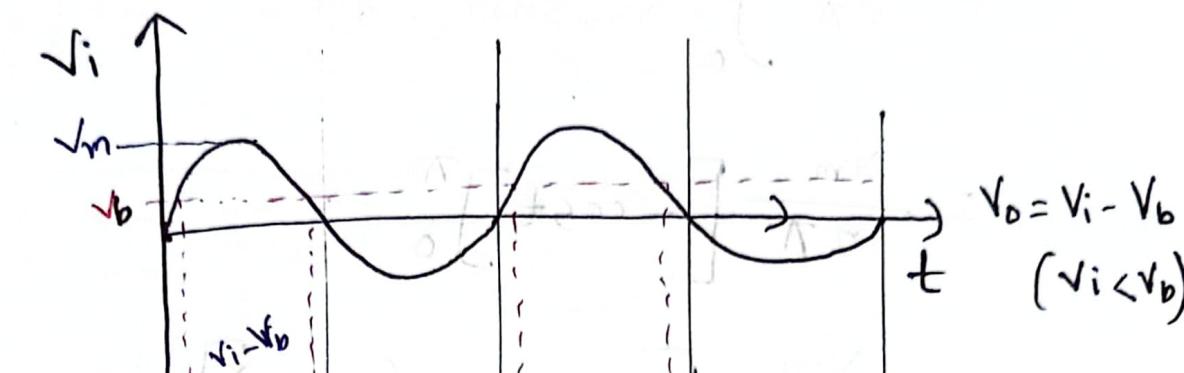
$$V_o = 0V$$



~~Derivation Disadvantages:~~

1. Low output voltage
2. Power is wasted as one of the half cycle is blocked. (Low output power.)
3. High ripple factor
 - ↳ presence of AC component in a DC quantity is called ripple.

Derivation:

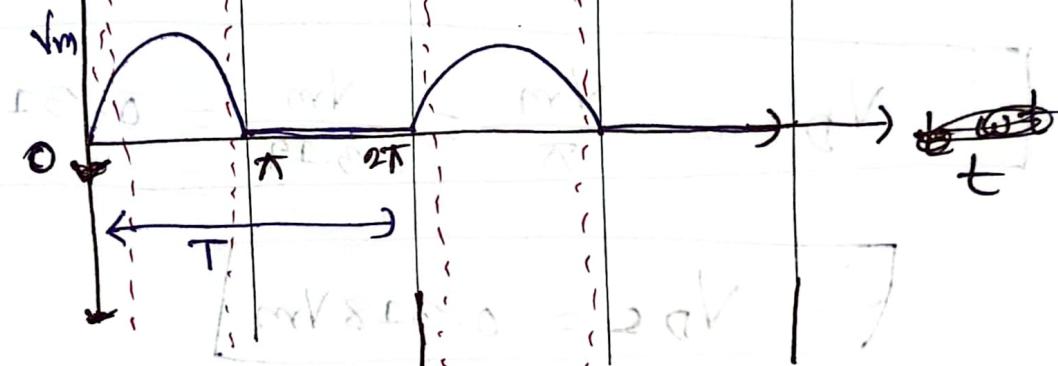


Ideal diode, V_0

$$V_0 = 0$$

$$V_0 = V_i \rightarrow +^{\text{ave}}$$

$$V_0 = 0 \rightarrow -^{\text{ave}}$$



Output Voltage, (V_{DC})

$$V_0 = V_m \sin \omega t \rightarrow 0 \leq \omega t < \pi$$

$$\left[+b \right] + \left[+b \right] \rightarrow \pi \leq \omega t \leq 2\pi$$

$$\therefore V_{DC} = \int_0^{\pi} V_0 dt / \pi \quad [T=2\pi]$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin \omega t dt + \int_{\pi}^{2\pi} 0 \cdot dt \right]$$

$$= \frac{1}{2\pi} \int_0^\pi V_m \sin t \cdot dt$$

$$= \frac{V_m}{2\pi} \left[-\cos t \right]_0^\pi$$

$$= \frac{V_m}{2\pi} \left[-\cos\pi - (-\cos 0) \right]$$

$$= \frac{V_m \times 2}{2 \times \pi}$$

$$\therefore V_{DC} = \frac{V_m}{\pi} = \frac{V_m}{3.14} = 0.318 V_m$$

$$\therefore V_{DC} = 0.318 V_m$$

again, for, $V_{rms} = \sqrt{\frac{1}{T} \int_0^T V_o^2 dt}$

$$[T = \frac{\pi}{\omega} \geq t_0 \geq 0] = \sqrt{\frac{2}{2\pi} \left[\int_0^\pi V_m^2 \sin^2 t dt + \int_\pi^{2\pi} 0 \cdot dt \right]}$$

$$= \sqrt{\frac{V_m^2}{2\pi} \int_0^\pi \sin^2 t dt}$$

$$= \sqrt{\frac{V_m^2}{2\pi} \left[\int_0^\pi \sin^2 t dt \right]} = \frac{V_m}{\sqrt{2\pi}}$$

$$V_{AC} = \sqrt{\frac{V_m^2}{2\pi}} \int_0^\pi \frac{1}{2}(1 - \cos t) dt$$

$$= \sqrt{\frac{V_m^2}{4\pi}} \left[t - \frac{\sin t}{2} \right]_0^\pi$$

$$= \sqrt{\frac{V_m^2}{4\pi}} \times (\pi - 0)$$

$$= \frac{V_m}{2}$$

$$\therefore V_{rms} = V_{AC} = \frac{V_m}{2}$$

extra

$$I_{DC} = \frac{V_{DC}}{R} = \frac{V_m/\pi}{R} = \frac{V_m}{R\pi} = \frac{I_m \times R}{R \times \pi}$$

$$\therefore I_{DC} = \frac{I_m}{\pi}$$

Similarly,

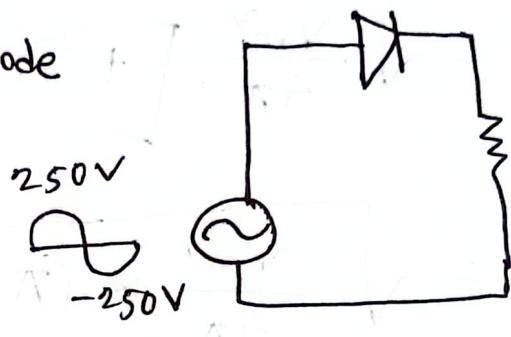
$$I_{AC} = \frac{V_{AC}}{R} = \frac{V_m/2}{R} = \frac{V_m}{2R} = \frac{I_m \times R}{2 \times R}$$

$$\therefore I_{AC} = \frac{I_m}{2}$$

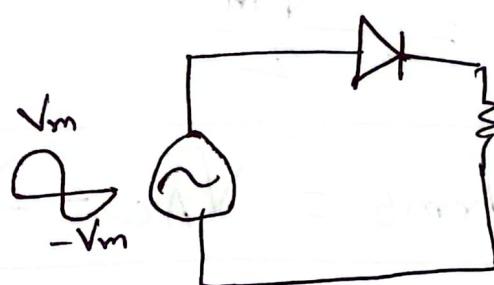
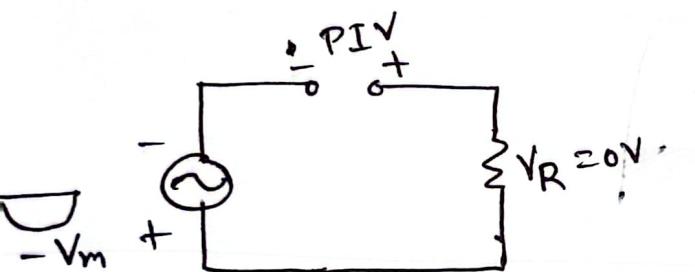
PIV rating for Half Wave Rectifier

Lecture - 9
15.09.2024

मार्गिक या voltage फल Diode
रहे इधर ना तरी PIV rating



During (-)ve half cycle diode is open



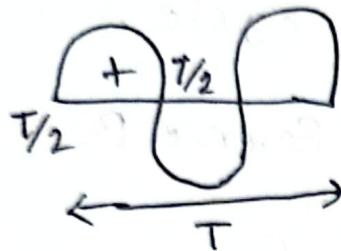
Applying KVL, $+V_m - PIV = 0$

$\Rightarrow PIV = V_m \rightarrow$ एवं Diode use करते ही
इधर या $PIV \geq V_m$ रहे

$$\frac{mI}{R} = \frac{mV}{R} = \frac{mV}{\frac{mV}{A}} = \frac{A}{1} = IA = I$$

$\frac{mI}{R} = IA = I$

Full Wave Rectifier

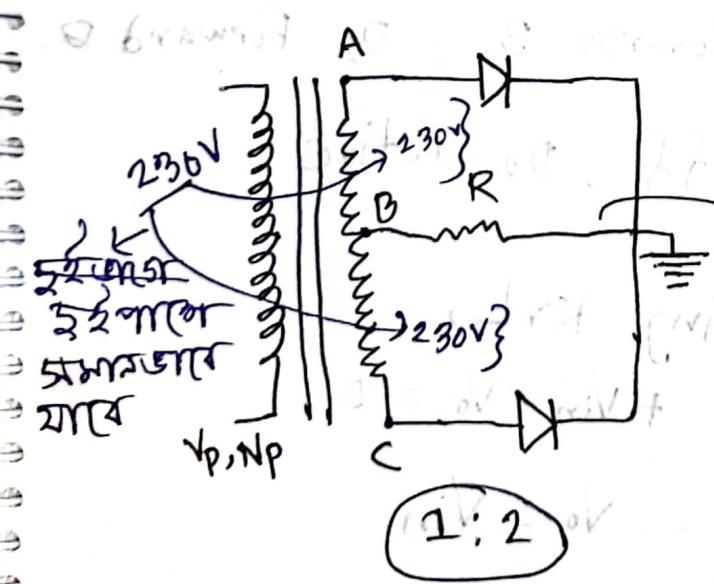


Types:

- 1 Full wave rectifier with centre tapped transformer
2. Bridge rectifier [4 diode] { ১ ব্রিজ একটি ফিল্ড সেল }

(2 diode কার্য)

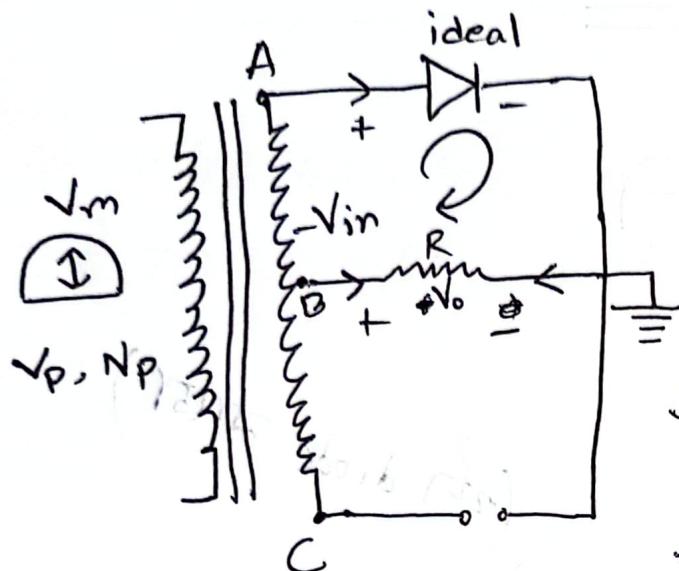
Full Wave Rec with Centre - . . .



$$N_{AB} = N_{BC} \quad \left| \frac{V_p}{N_s} = \frac{N_p}{N_s}; V_p \propto N_p \right.$$

মাঝ (মধ্যে) wire করে
ground-এ কানক | ফাল
AB, BC কর অস আগ হিতে

For Positive half cycle

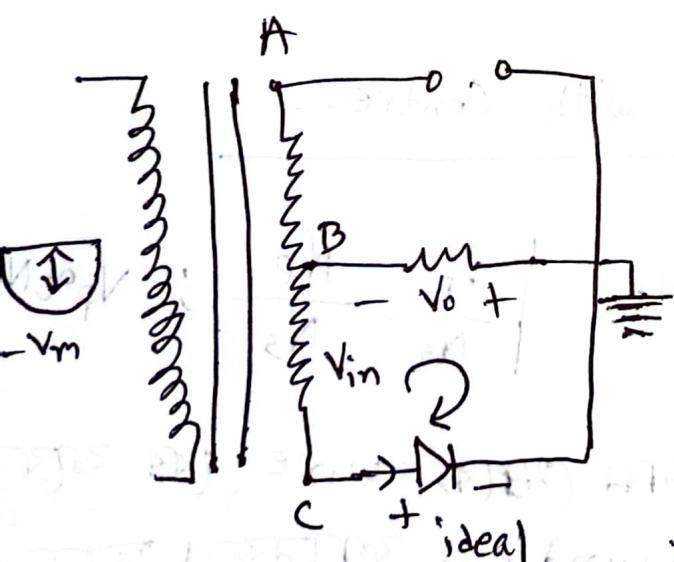


During $(+)^{ve}$ half cycle,
 D_1 Forward B., D_2 Reverse B.

$\therefore D_1$ active, D_2 off

$$\therefore V_o = V_{in} \quad \left\{ \begin{array}{l} \text{applying KVL,} \\ -V_{in} + V_o = 0 \\ \therefore V_o = V_{in} \end{array} \right.$$

For Negative half cycle



During $(-)^{ve}$ half cycle

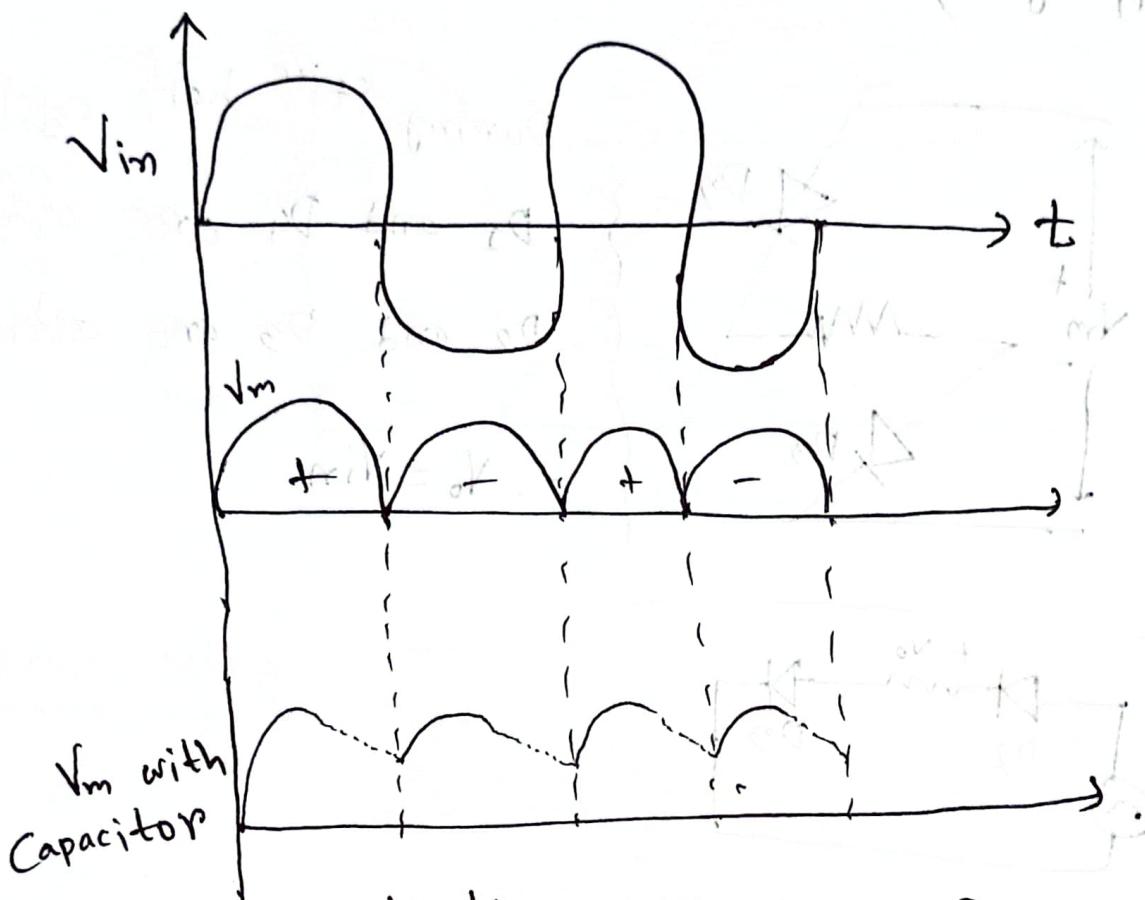
D_1 Reverse B., D_2 Forward D.

$\therefore D_1$ off, D_2 active

\therefore Applying KVL,

$$+V_{in} - V_o = 0$$

$$\therefore V_o = V_{in}$$

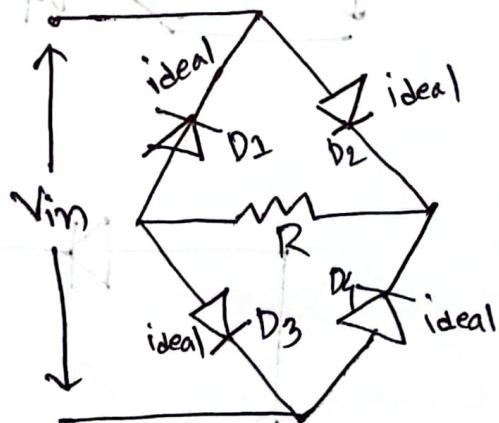
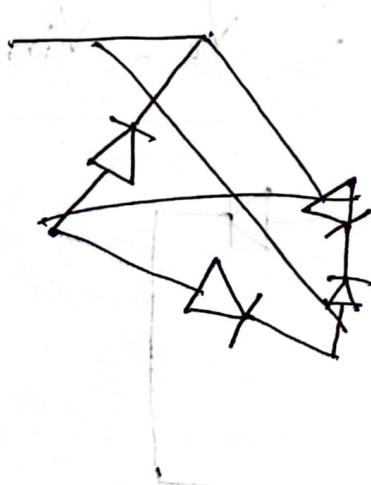


pulsating $D_c = A_c + D_C \}$ ripple factor

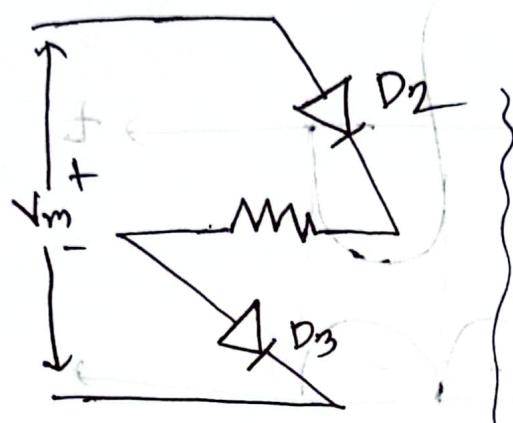
EEE 1231

** Bridge Rectifier

Lecture - 10
22.09.2024



positive half cycle;

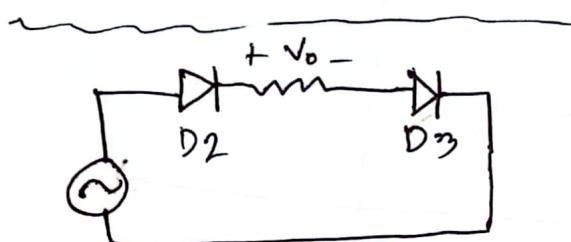


During $(+)^{ve}$ half cycle

D_2 and D_4 are off.

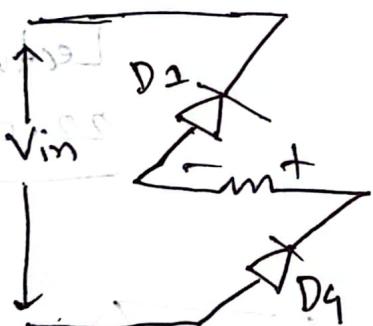
D_2 and D_3 are active

$$\therefore V_o = V_{in+}$$



negative half cycle { extra + 2A = 30 pathalog

negative half cycle,

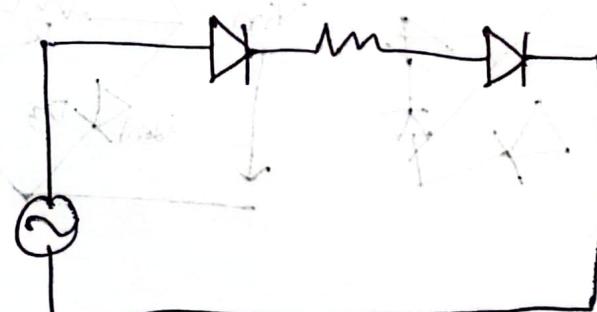


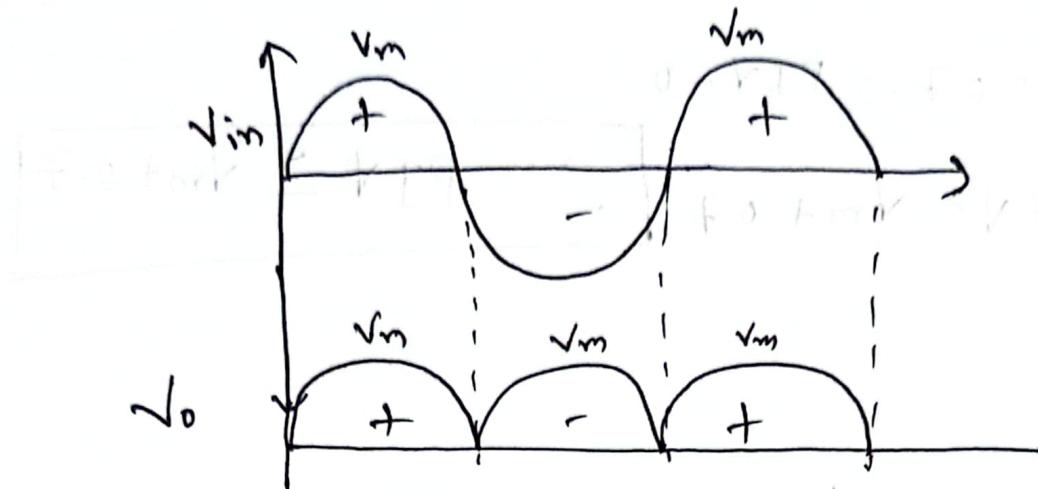
During $(-)^{ve}$ half cycle

D_2 and D_3 are off.

D_1 and D_4 are active

$$\therefore V_o = V_{in-}$$





V_o = 2V_m

Output voltage:

$$V_{DC} = \frac{2V_m}{\pi}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

both bridge and centre tapped

Centre tapped : $\rightarrow V_{DC} = \frac{2V_m - 0.7/0.3}{\pi L}$

bridge tapped : $\rightarrow V_{DC} = \frac{2V_m - 2 \times 0.7/0.3}{\pi L}$

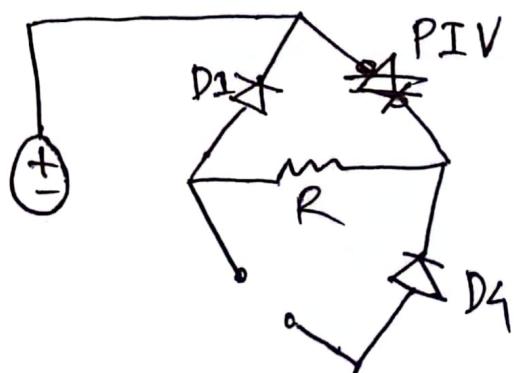
PIV rating

when ideal diode,

$$+V_o - \phi \cdot PIV = 0$$

$$\Rightarrow PIV = V_o(\max)$$

$$\therefore PIV = \sqrt{m} \mid PIV \geq \sqrt{m}$$



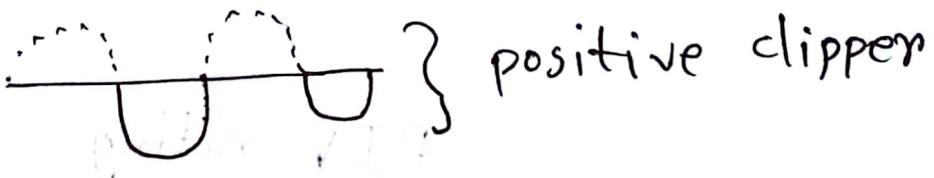
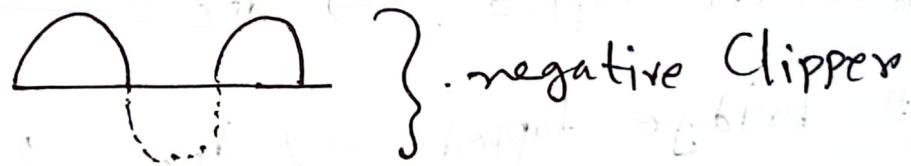
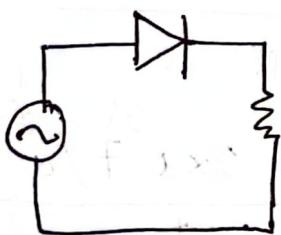
when Si diode,

$$+V_o + 0.7 - PIV = 0$$
$$\therefore PIV \leq V_m + 0.7$$

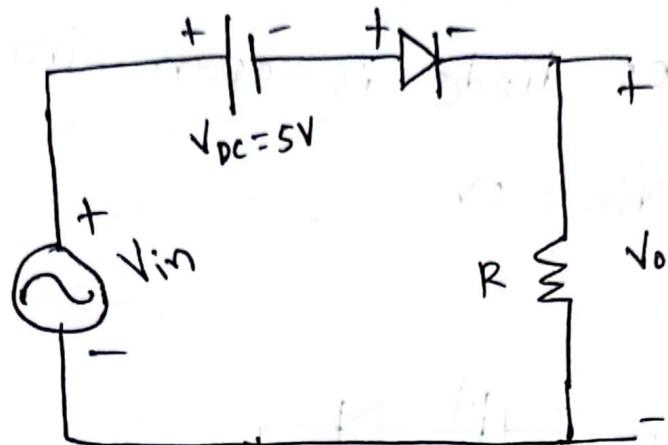
$$\therefore PIV \geq V_m + 0.7$$

* 2. Clipper

Clipper: Clipper is a device that clips off a portion of the input waveform without distorting the remaining part.



Type-1



During (+)ve half cycle,

when $V_{in} < V_{DC}$

D_1 is off, so

$$V_o = 0V$$

when $V_{in} > V_{DC}$

Applying KVL, for Top branch

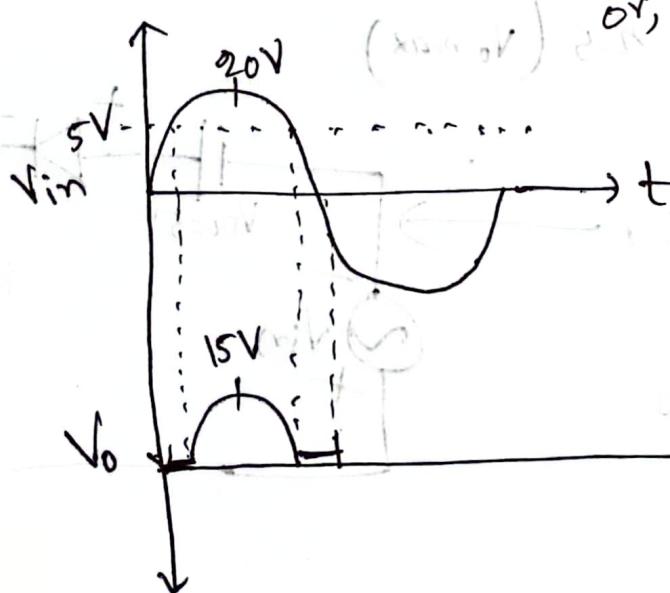
$$-V_{in} + V_{DC} + V_o = 0$$

$$\Rightarrow V_o = V_{in} - V_{DC}$$

$$\text{or, } 5 - 5 = 0V$$

$$\text{or, } 7 - 5 = 2V$$

$$\text{or, } 20 - 5 = 15V$$



$30V > 20V$ results

$30V + 5V = 0V$

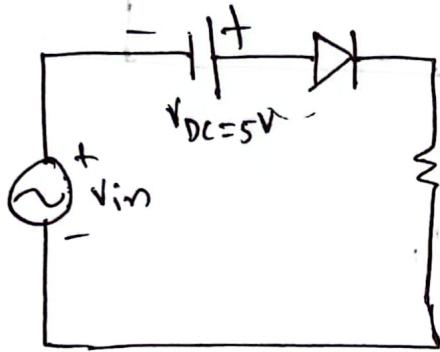
$$T = 2\pi f$$

$$f = \omega / 2\pi$$

and During $(-)^{ve}$ half cycle,
for both sources diode is open circuited,

$$V_{in} = 0V$$

Type-2



During $(+)^{ve}$ half cycle, both source diode is active

$$-V_{in} - V_{DC} + V_o = 0$$

$$\therefore V_o = V_{in} + V_{DC}$$

$$= 0 + 5 = 5V \quad (V_o \text{ min})$$

$$= 20 + 5 = 25 \quad (V_o \text{ max})$$

During $(-)^{ve}$ half cycle,

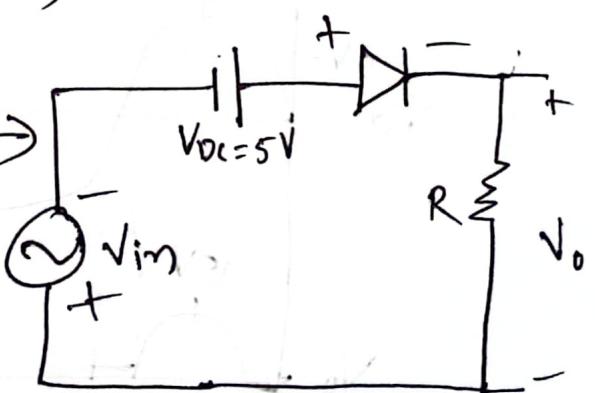
when $V_{in} < V_{DC}$

$$+V_{in} - V_{DC} + V_o = 0$$

$$\therefore V_o = -V_{in} + V_{DC}$$

$$= 0 + 5 = 5$$

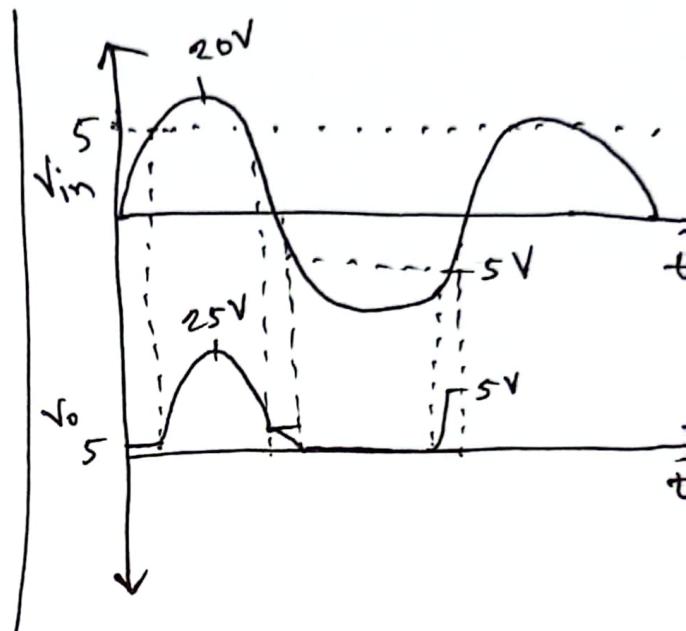
$$= -5 + 5 = 0$$



when $V_{in} > V_{DC}$, $D_0 - D_2$ (diode) is open.

$$\begin{aligned}\therefore V_o &= 0V \quad \text{if } V_{in} > V_o \\ &= -(5+5)V = 0V \\ \text{or, } &= (-4+5)V = 1V \\ \text{or, } &= (-2+5)V = 3V \\ \text{or, } &= (0+5)V = 5V\end{aligned}$$

Book → Biased series
clipper.

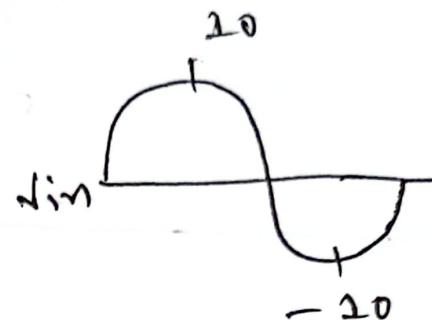
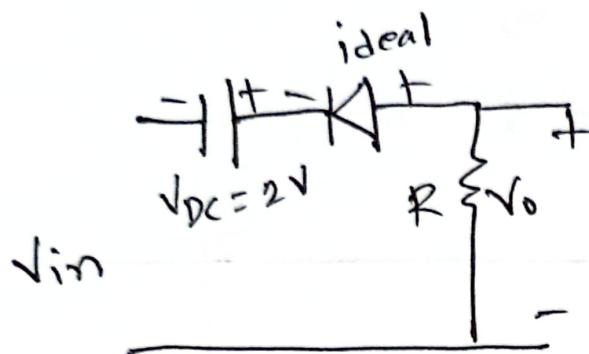


EEE 1232

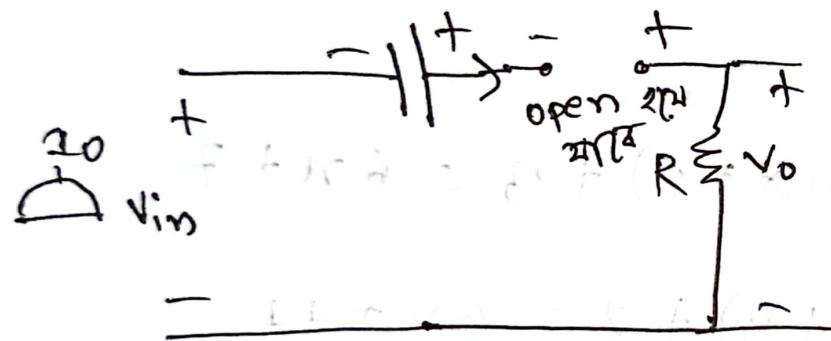
Clipper Math

Lecture - 12

23.09.2024

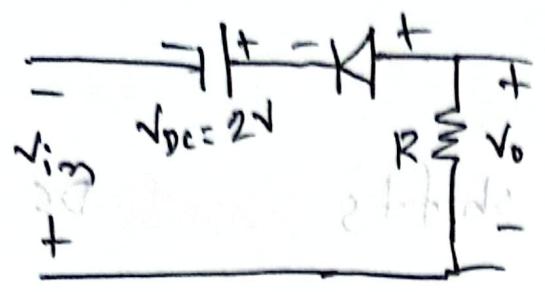


During $(+)^{\text{ve}}$. (half cycle),



for both sources diode
is open,
 $V_o = 0V$

During (-)ve half cycle (negative)



when $V_{in} < V_{DC}$,
diode open circuited

$$V_o = 0V$$

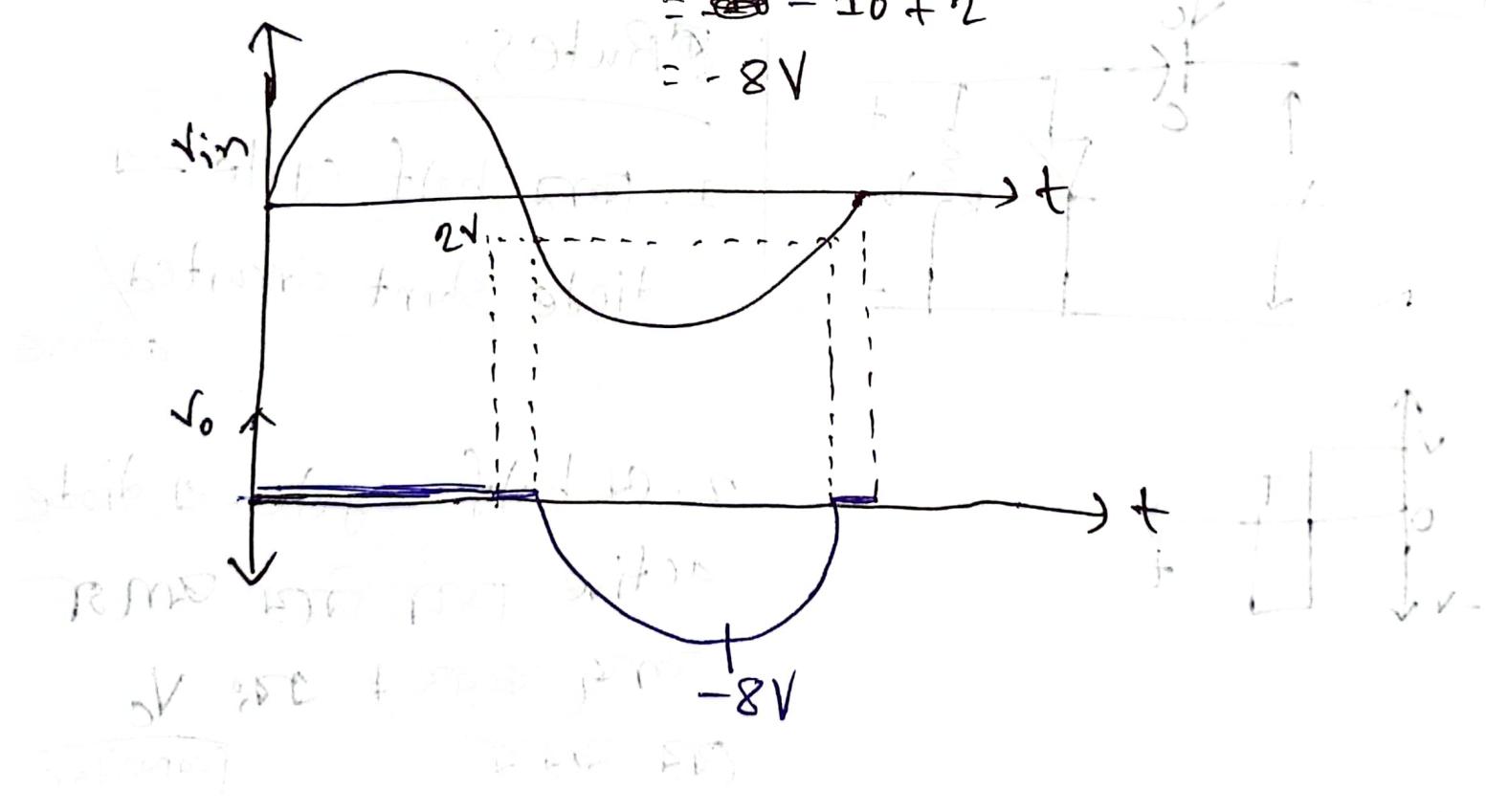
and, when $V_{in} > V_{DC}$

KVL,

$$+V_{in} - V_{DC} + V_o = 0$$

$$\therefore V_o = -V_{in} + V_{DC}$$

$$\begin{aligned} &= -20 + 2 \\ &= -8V \end{aligned}$$

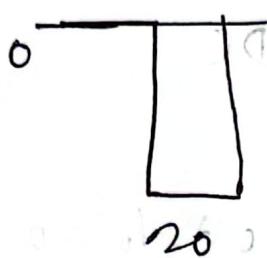
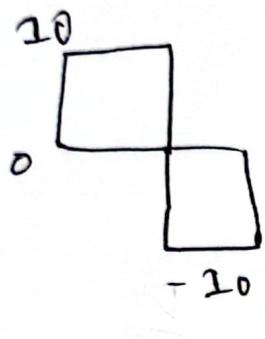


and voltage different.

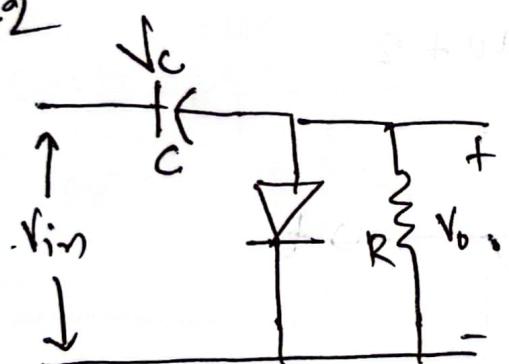
positive or negative?

Clamper

→ Clamper is a circuit that shifts input DC level into another DC level.

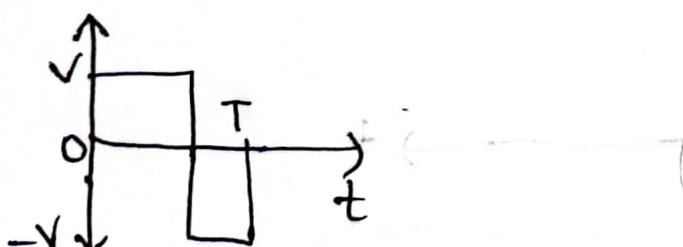


Math-2



Rules:

1. ~~for half cycle -~~ diode short circuited/ active



2. ~~(V half cycle -) diode active~~ নিয়ে আসো

বাল্ক করবে $v_o = V_c$
যেখানে V_c
is the value of capacitor

3. finally other half cycle এর জন্য v_o বের করবে

for (+)^{ve} half cycle,

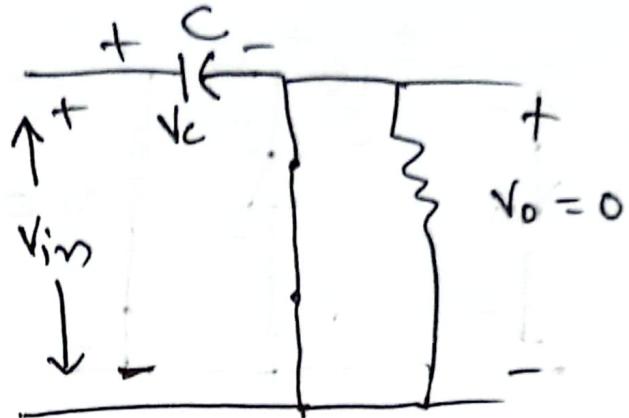
diode is active

$$V_o = 0V$$

$$\therefore -V_{in} + V_C = 0$$

$$\therefore V_C = V_{in}$$

$$= 20V$$



$(2\pi/2)$ half cycle \rightarrow diode short $2\pi/2$ $\pi\pi/2$ $(3\pi/2)$ half-cycl \rightarrow capacitor charge $2\pi/1$

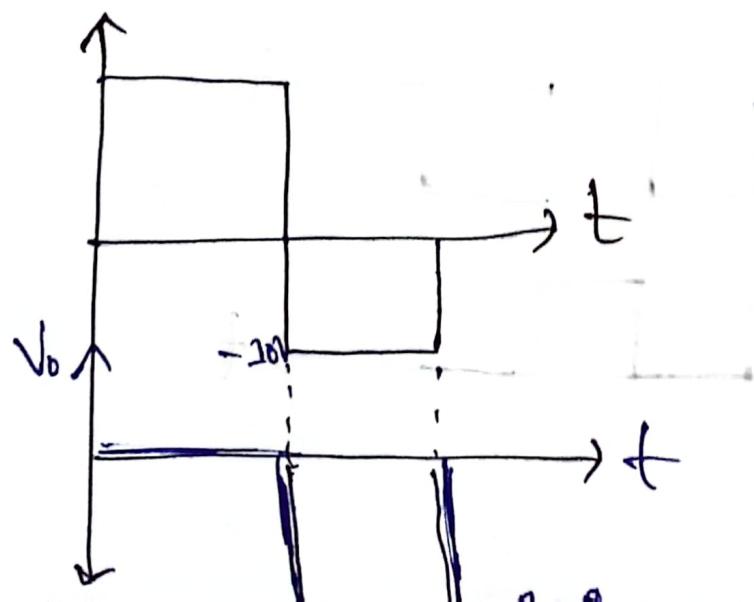
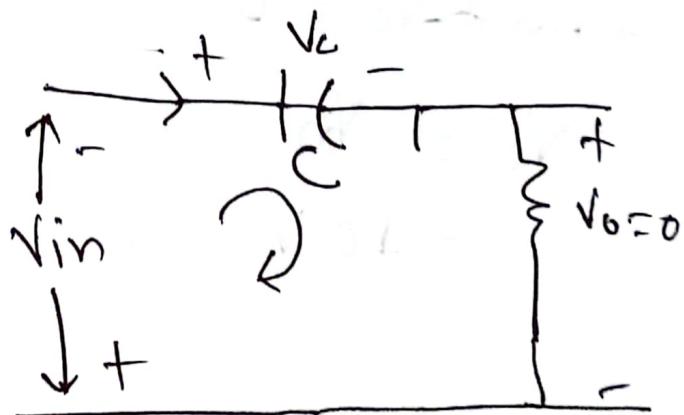
For (-)^{ve} half cycle,

$$+V_{in} + V_C + V_o = 0$$

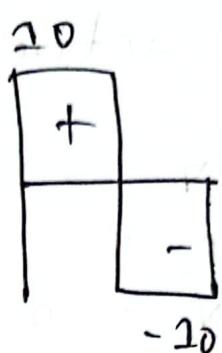
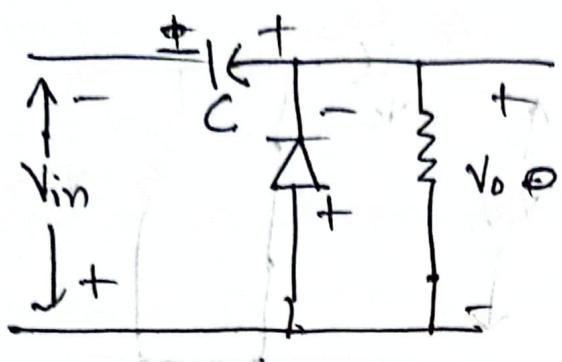
$$\therefore V_o = -V_{in} - V_C$$

$$= -20 - 20$$

$$= -40V$$



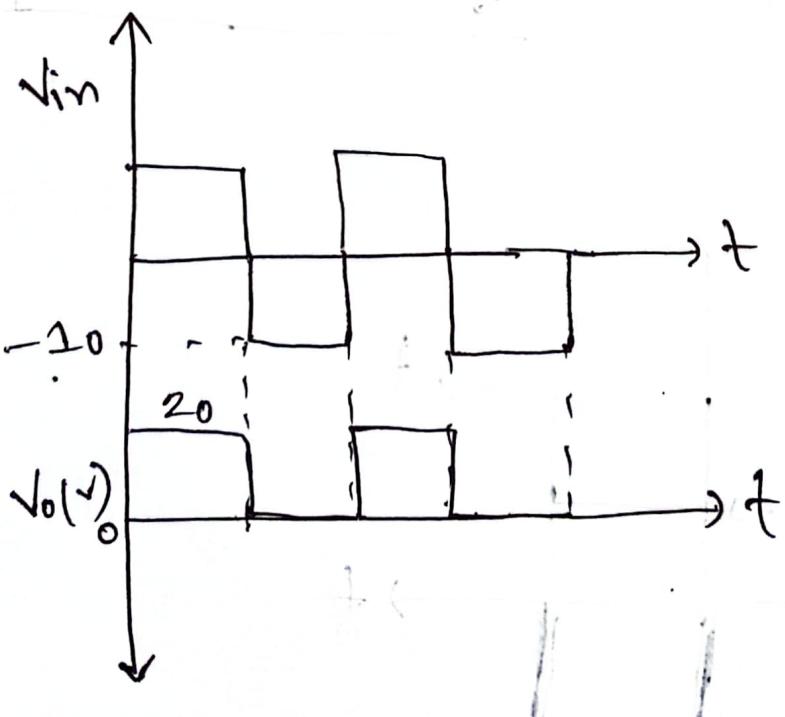
Math-3



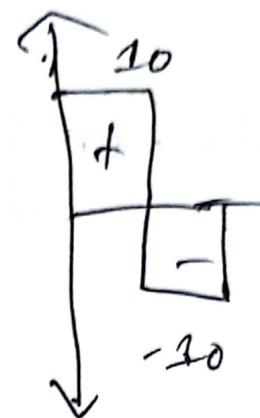
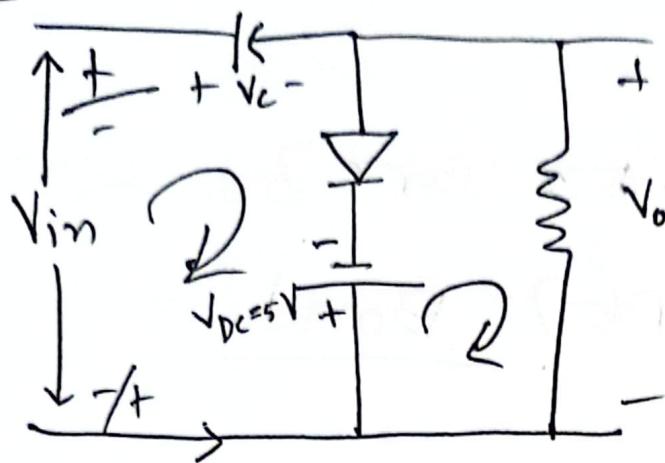
for $(-)^\text{re}$ half cycle,
diode is active,
 $\therefore V_o = 0$

$$+V_{in} - V_C = 0 \\ \therefore -V_C = V_{in} \\ = 20 \text{ V}$$

for $(+)^\text{re}$ half cycle,

$$-V_{in} - V_C + V_o = 0 \\ \text{or, } V_o = V_C + V_{in} \\ = 10 + 20 \\ = 20 \text{ V}$$


math - 4



During $(+)^{\text{ve}}$ half,

diode is active (short circuited)

$$V_o = -5V$$

$$-V_{in} + V_c - V_{DC} = 0$$

$$V_c = 5 + \frac{V_{in}}{20V} = 15V$$

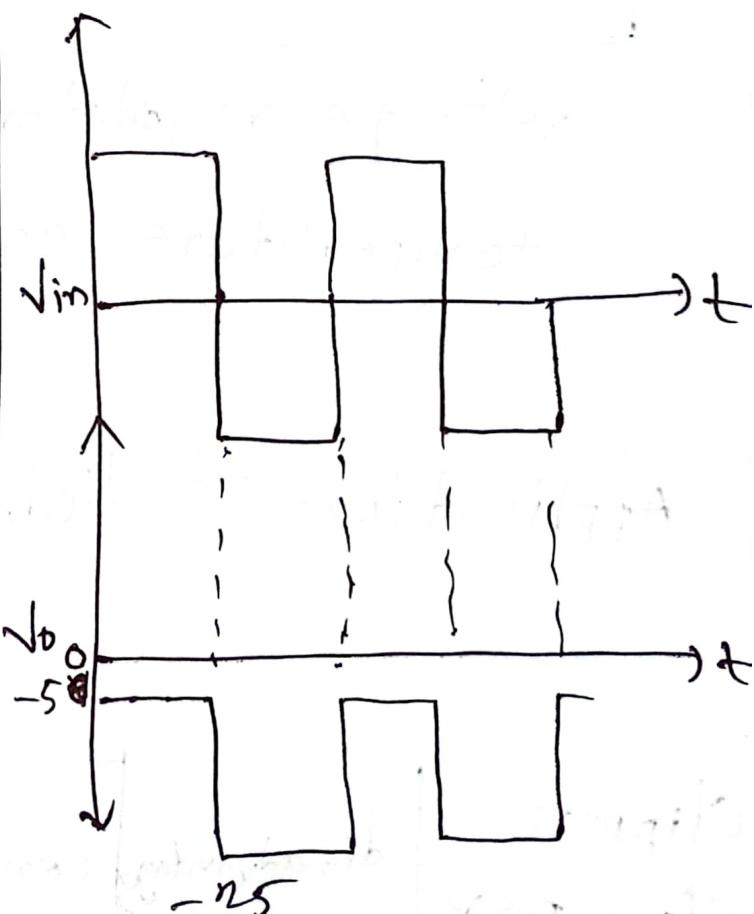
During $(-)^{\text{ve}}$ half,

$$+V_{in} + V_c + V_o = 0$$

$$V_o = -V_{in} - V_c$$

$$V_o = -10 - 25$$

$$V_o = -25V$$



EEE 1232

Semester final

Lecture - 1

20.08.2024

BJT

BJT: BJT is a three terminal device that consists of either two N-type materials and one P-type material or two P-type material and one N-type material.

Transistor के Amplifier and switch फ़िल्ड्स में उपयोग है।

Amplifier के लिए कमाते minimum 3 terminal होते हैं। i.e. एक terminal → controller

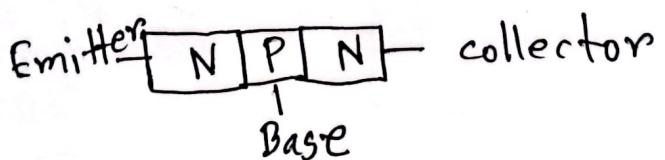
Types of BJT: There two types:

1. NPN —

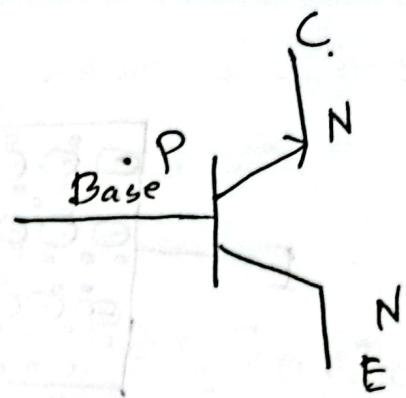
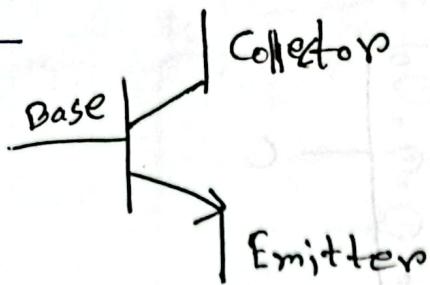
N	P	N
---	---	---

2. PNP —

P	N	P
---	---	---



Symbol



N-P-N BJT : এর পথে

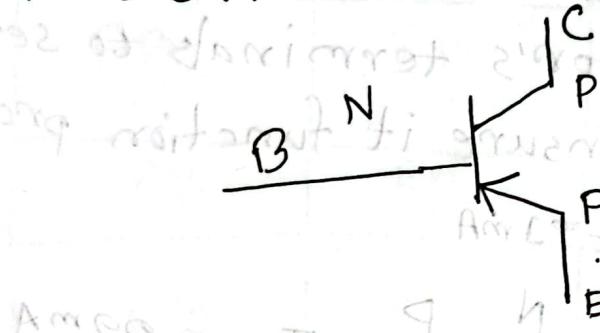
চিহ্ন বাইরের দিক

গ্রিসি

বেগুনি

Type: 2

P-N-P BJT: এর পথে চিহ্ন ক্ষেত্রে থামে



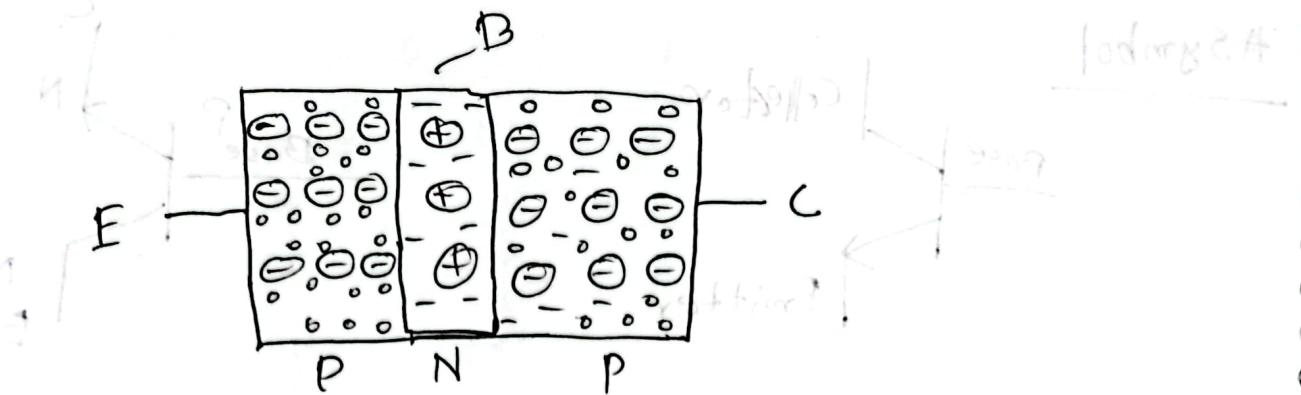
p-type পথে যদি N-type এর দিকে current flow করবে।

Construction

Emitter = Heavily doped (অর্ধপথ current flow)

Base = lightly doped (অর্ধপথ current flow)

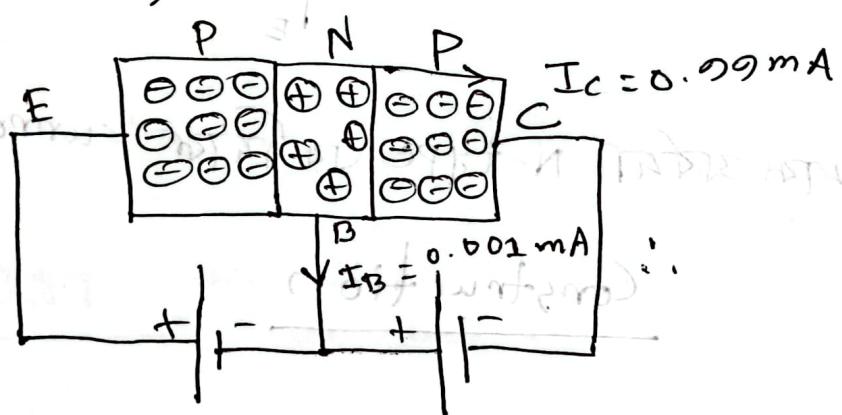
Collector = moderately doped



Biasing

* Biasing: BJT biasing is the process of applying voltages to the transistor's terminals to set its operating operating points and ensure it function properly, in a circuit.

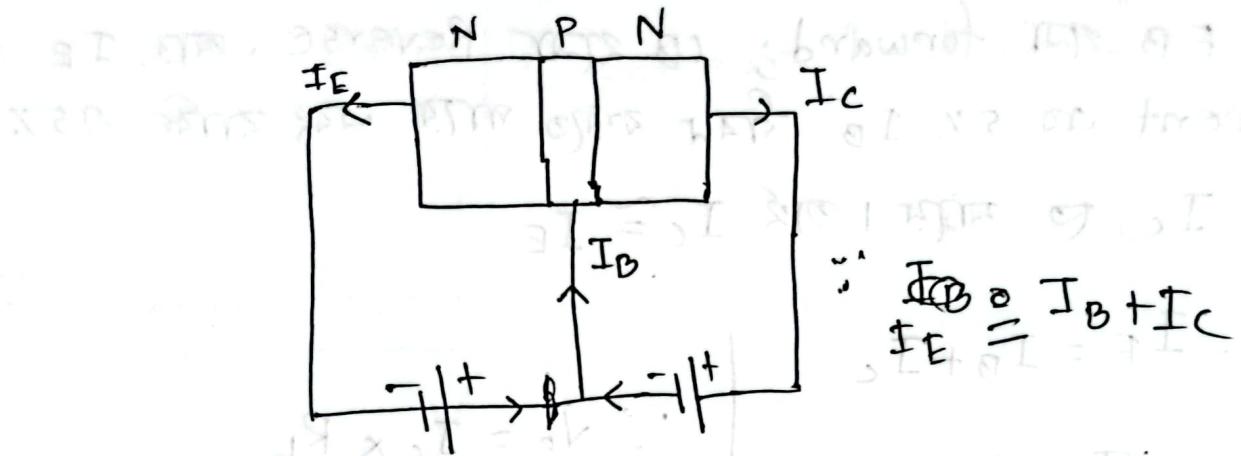
$$\rightarrow I_E = -1\text{mA}$$



(w.r.t. I_E terminal side) base bias = nothing

∴ $FB = \text{Forward Bias}$ } $FB \xrightarrow{RB} \text{Amplifiers}$

$RB = \text{Reverse Bias}$ } $RB \xrightarrow{\text{nothing}} \text{nothing}$

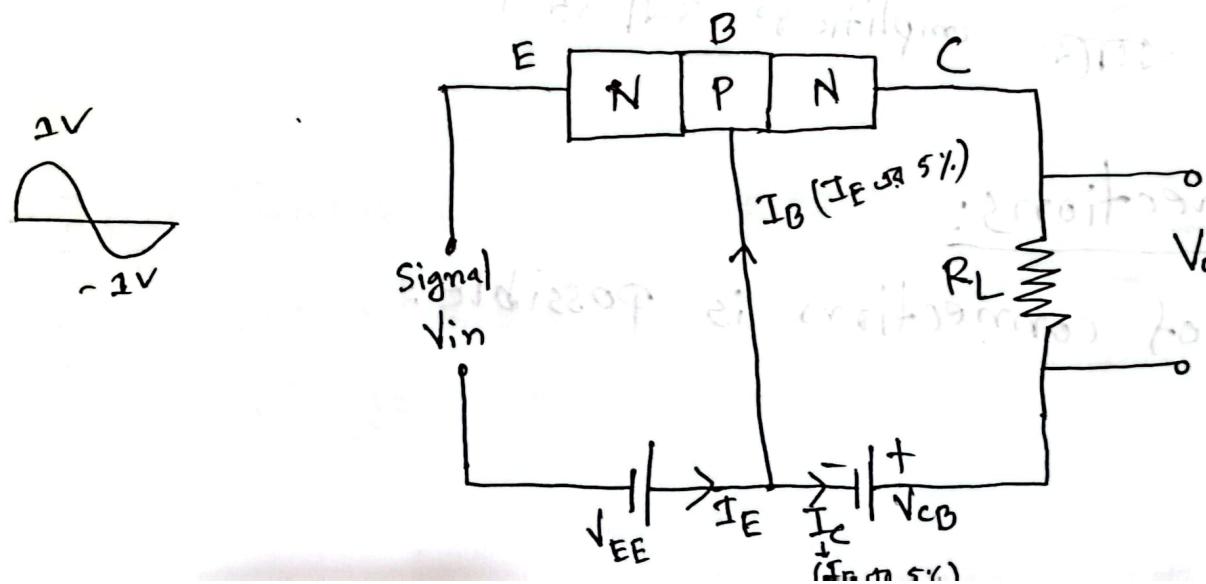


Junction	E-B	C-B	Application
Biassing	Forward Bias	Reverse Bi-as	Amplifier
	FB	FB	Switch on (saturation)
	RB	RB	switch off (cut off)
	RB	FB	not used

B J T as an Amplifier

Lecture-2

21.10.2024



Note: EB হলো forward; CB হলো Reverse. আবু I_E এর current এর ৫%. I_B গুরুত্ব কমাতে পারে এবং বাৰি ১৫% current I_C কো মানুন। তাহুৰ $I_C \approx I_E$

$$\therefore I_E = I_B + I_C$$

$$\therefore I_E \approx I_C$$

$$\therefore V_o = I_C \times R_L$$

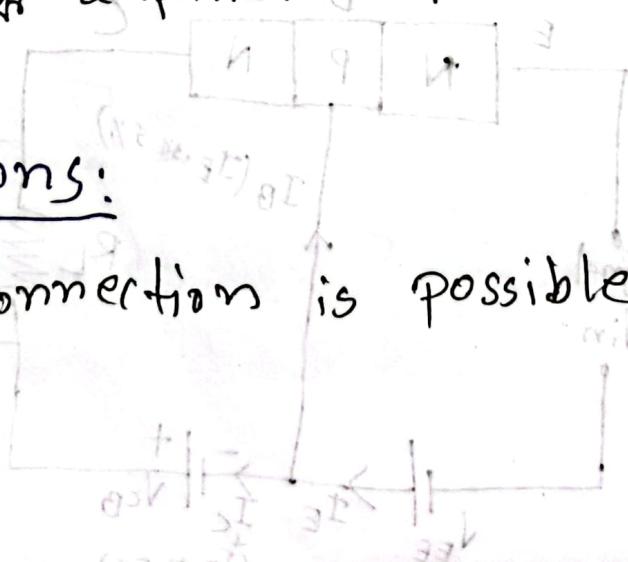
Amplifier: An amplifier is an electronic device that increases the strength of a signal, such as sound or electrical current, making it louder.

$$\text{Amplifier} = \frac{\text{Output}(V_o)}{\text{Input}(V_{in})}$$

ব্যাখ্যা: The input মুকে weak signal এবং ছোট current মানে R_L এর মধ্যে দিয়ে একাধিক মানে V_o এর বেশি current পাওয়া যায়, এজনে amplifier বলা হয়।

BJT Connections:

3 types of connection is possible.



2. Common Base:

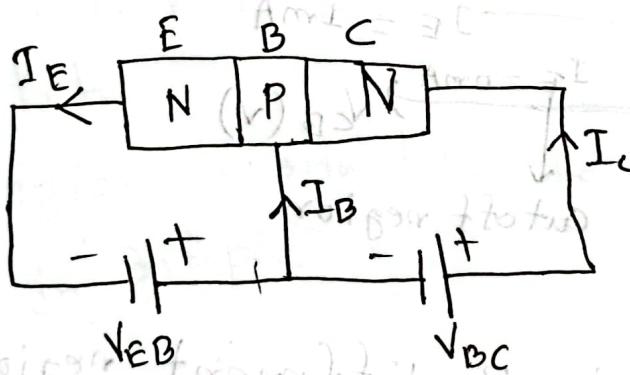
2. Common Emitter

widely used
because high current gain

3. Common Collector:

2. Common Base:

Common Base: A common Base connection, is a type of transistor configuration where the base terminal is common to both the input and output junction.



$$I_E = I_B + I_C$$

↓

current I_E

বিদ্যুৎ এবং শব্দে পরিদর্শক
Battery (+) হলো

Input Parameters:

Input Current = I_E

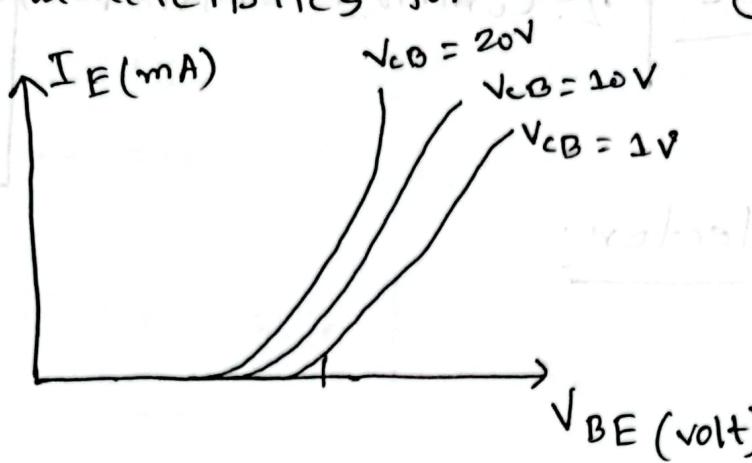
Input Voltage = V_{BE}

Output parameters:

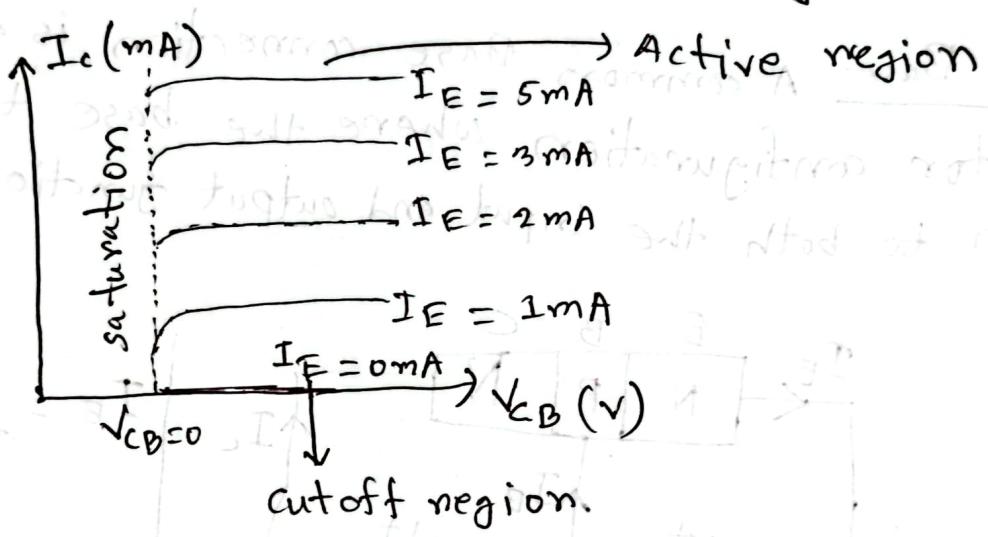
Output current = I_C

Output voltage = V_{BC}

Input characteristics for CB configuration



Output characteristics for CB configuration:



A BJT can work in 3 different regions:

1. Active region 2. Saturation 3. Cut-off region

B. $\beta E = \text{forward bias}$
 $\beta V = \text{forward bias}$

$\beta E = \text{forward bias}$
 $\beta V = \text{forward bias}$

Active region: BJT works in active region when E-B forward, C-B reverse. In active region BJT works as an amplifier.

Region-1

Saturation region: When E-B junction and C-B junction both are in forward. In saturation BJT works as an on switch and once it turns ON.

V_{BE} is constant at 0.7 volt.

It is situated at the left hand side of $V_{CB} = 0$

Cutoff region: BJT works in cut-off region when E-B reverse and C-B reverse. In cut-off region BJT works as an off switch.

* Cut-off region is situated further below;

$I_E = 0 \text{ mA}$ in graph.

$$\beta = \alpha \cdot \frac{I_C}{I_B} = \alpha \cdot \frac{0.99}{1} \quad [\text{always } \alpha < 1]$$

current gain
from CB config.

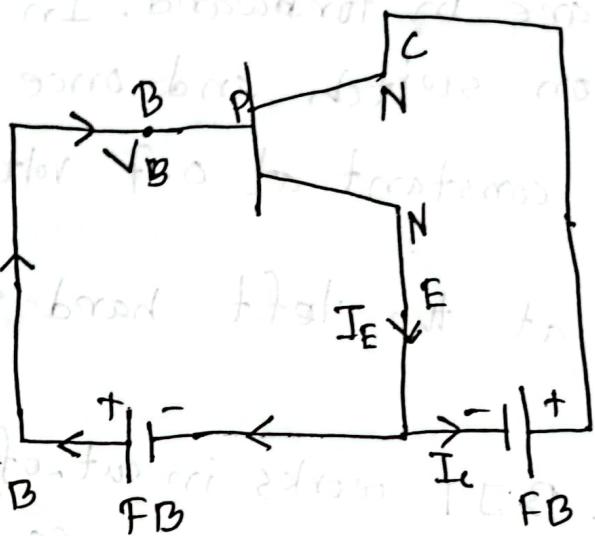
Config base of amplifier এখন কোন অসমীয়া
কথা নেই হাতে

* Common base current flow amplifier ক্ষয়তি পরিচ্ছে
না। তবুও কাজ করবে না।

Lecture - 3

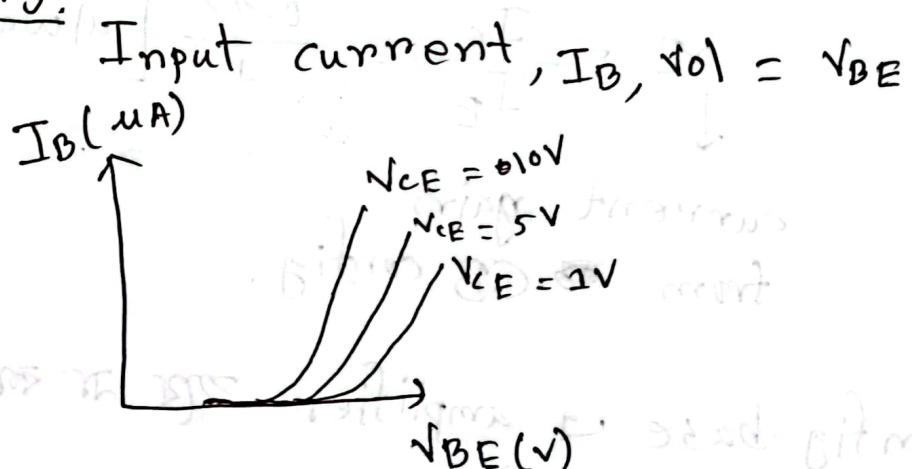
27.10.2024

Common Emitter Configuration



In CE configuration / Emitter terminal is common to both input and output side.

Input parameters:



output parameter:, output current = I_C

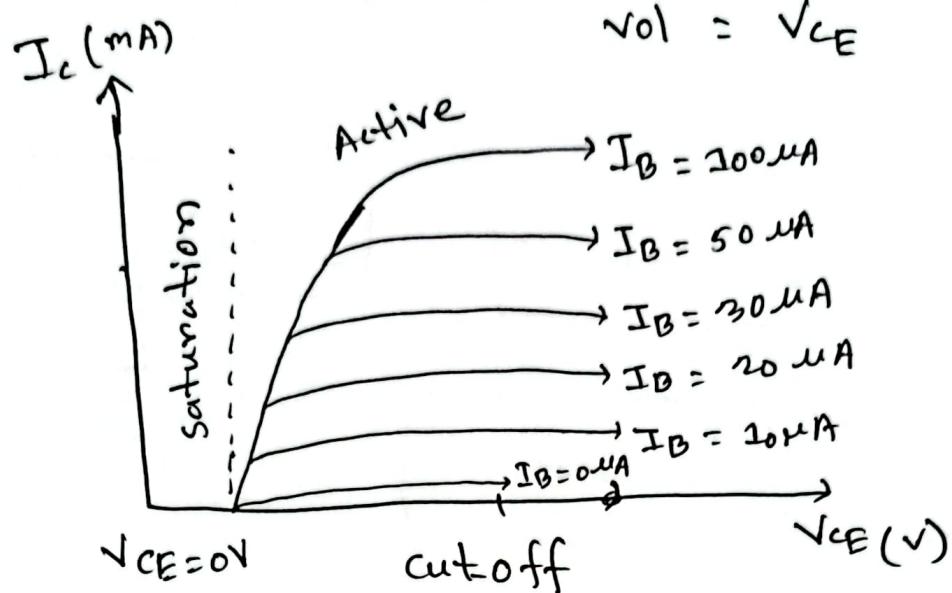


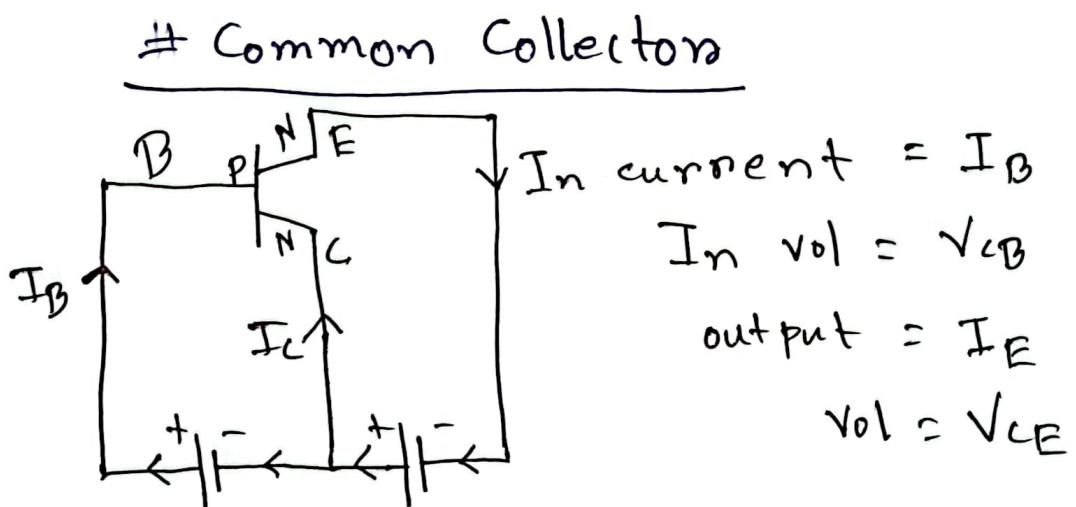
Fig: output characteristic for CE config

Q. Find out the mostly used BJT config.?

$$\beta = \frac{I_C}{I_B} \rightarrow \text{current gain factor for CE config.}$$

$$= \frac{0.2}{0.02} = 100 \quad [\beta \gg 1]$$

Q. Briefly describe why CE config is widely used?



BJT vs Math

MATH:

$$1. I_E = I_B + I_C$$

$$2. I_E = I_B(\beta + 1)$$

$$3. \beta = \frac{I_C}{I_B}$$

$$4. \alpha = \frac{I_C}{I_E}$$

common base configuration

$$* I_E = I_B + I_C$$

$$\text{or, } \frac{I_C}{\alpha} = I_B + I_C$$

$$\text{or, } I_B = \frac{I_C}{\alpha} - I_C$$

$$I_B = I_C \left(\frac{1}{\alpha} - 1 \right)$$

$$I_B = I_C \left(\frac{1-\alpha}{\alpha} \right)$$

$$\therefore \frac{I_B}{I_C} = \frac{1-\alpha}{\alpha}$$

$$\frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

$$\frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

$$5. \beta = \frac{\alpha}{1-\alpha}$$

$$\frac{I_C}{I_B} = \beta$$

Math: 1

$$I_C = 2 \text{ mA}$$

$$\beta = 100$$

$$I_E = ?$$

OR,

$$I_E = I_B(\beta + 1)$$

$$\beta = \frac{I_c}{I_B}$$

$$\text{or, } 100 = \frac{1}{I_B}$$

$$I_B \times 100 = 1$$

$$\text{or, } I_B = \frac{1}{100} \text{ mA}$$

$$\therefore I_E = I_c + I_B$$

$$= 1 + \frac{1}{100}$$

$$= 1.01 \text{ mA}$$

good answer
mitigation

$$\frac{qI}{qI} = qI$$

$$= qI$$

$$\frac{\text{Math-2}}{B} \quad I_E = 1 \text{ mA} \quad \beta = 100$$

$$I_B = ? \frac{1}{\beta+1} = \frac{1}{101}$$

$$\beta = \frac{I_c}{I_B}$$

$$I_E = I_B + I_c$$

$$I_E = I_B (\beta + 1)$$

$$\beta = \frac{I_c}{I_B}$$

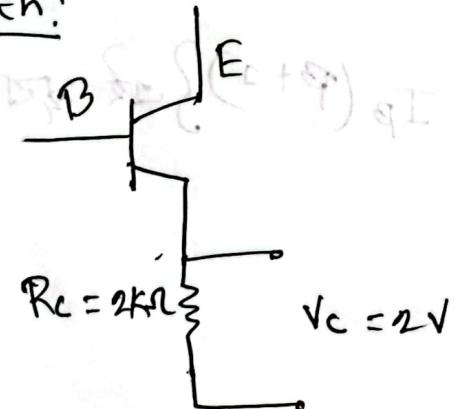
$$I_B = 100 + 1$$

$$I_c = (100 \times 0.0001) \text{ mA}$$

$$I_B = 0.0001 \text{ mA}$$

$$= 0.0001 \text{ mA}$$

Slide Math:



Sol'n:

$$V = IR$$

$$V_C = I_C R_C$$

$$\frac{V_C}{R_C} = I_C$$

$$\therefore I_C = 2 \text{ mA}$$

$$\therefore \alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha} = 2.052 \text{ mA}$$

$$I_C = 0.1 \text{ mA}$$

$$\alpha = 0.05$$

$$I_B = ?$$

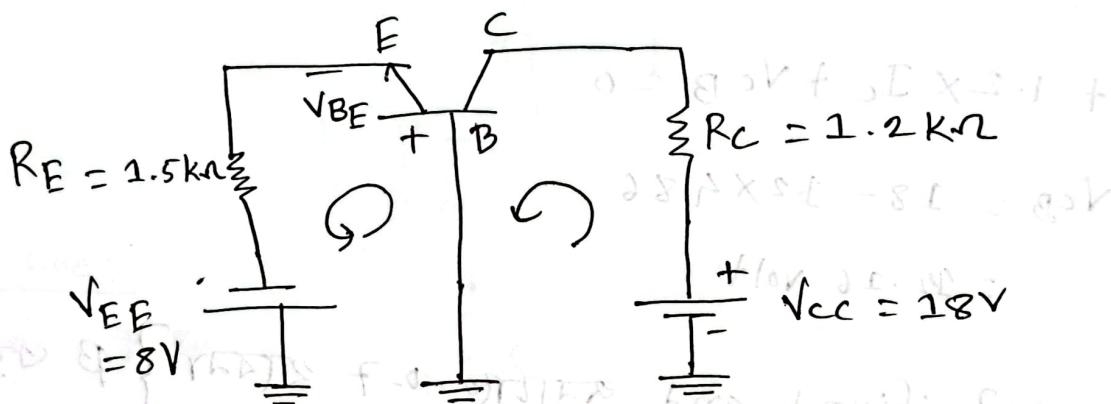
$$\text{or, } I_B = I_C + I_P$$

$$I_B = I_E - I_C$$

$$= (1.052 - 1) \text{ mA}$$

$$= 0.052 \text{ mA}$$

Slide example-4:



common base configuration transistor যেখানে
fixed হন্ত রয়েছে

$$V_{BB} = 0.7 \text{ (fixed)}$$

$$I_C = ?$$

$$V_{CB} = ?$$

$$I_C \cong I_E$$

$$+V_E - I_E * R_E - V_{BE} = 0 \quad (\text{NDL})$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_B}$$

$$= \frac{8 - 0.7}{2.5} = 4.86 \text{ mA}$$

$$I_C \approx I_E \rightarrow I_C = 4.86 \text{ mA}$$

$V_{CB} = \text{Right loop } \rightarrow \text{KVL apply}$] এবং মনে কর $V_{BE} = 0.7 \text{ V}$
যখন আবেগ স্থাপিত হবে।

$$-18 + 1.2 \times I_C + V_{CB} = 0$$

$$V_{CB} = 18 - 1.2 \times 4.86$$

$$= 12.26 \text{ volt}$$

$\{ V_{BE} = 0.7 \text{ fixed and অন্যটি } 0.7 \text{ রাখো } \} \beta \text{ এর মান}$

অঙ্গ রা নকলি $I_E \approx I_C$

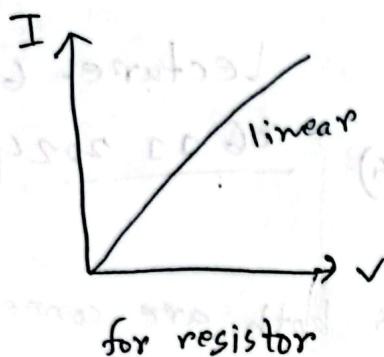
$$\left. \begin{array}{l} S = I_E \\ S = 4.86 \end{array} \right\}$$

$$(6 \times 1) \text{ f.o. = 6A}$$

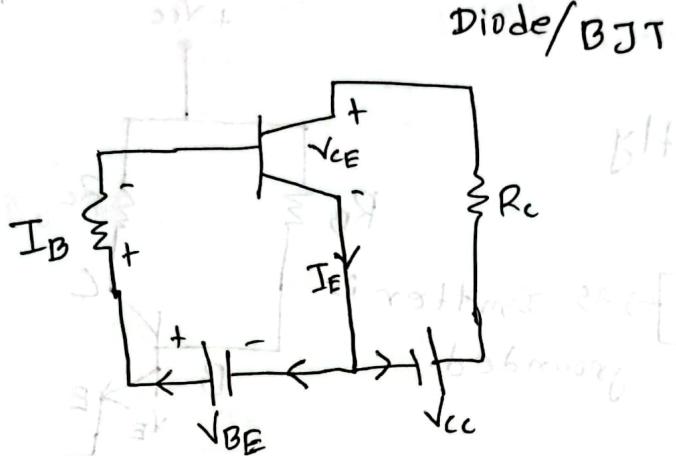
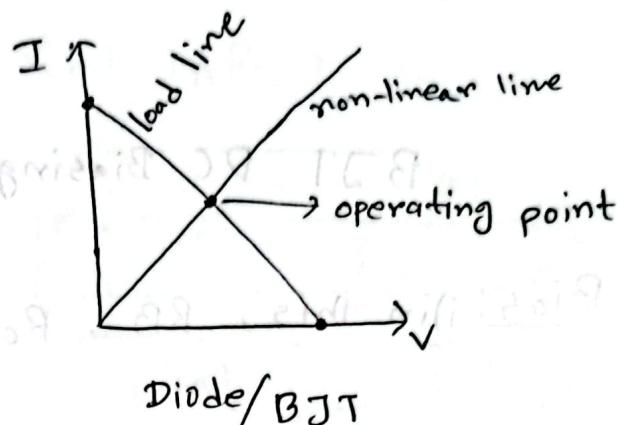
$$S = I_E$$

(A)

$$0 = 38k - 38 \times 3I - 3V +$$

Load Line Analysis

for resistor

Input side:

$$-V_{BE} + I_B R_B = 0$$

$$\therefore V_{BE} = I_B R_B$$

Output side:

$$-V_{CE} + I_C R_C + V_{CC} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

When, $I_C = 0$,

$$V_{CE} = V_{CC}$$

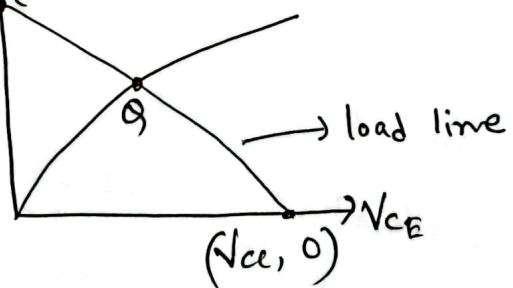
again,

When $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C}$$

for, $(V_{CC}, 0)$ and $(0, \frac{V_{CC}}{R_C})$

$$(0, \frac{V_{CC}}{R_C})$$



Operating point: The point of intersection between characteristics curve and load line is called the operating point.

Lecture-6

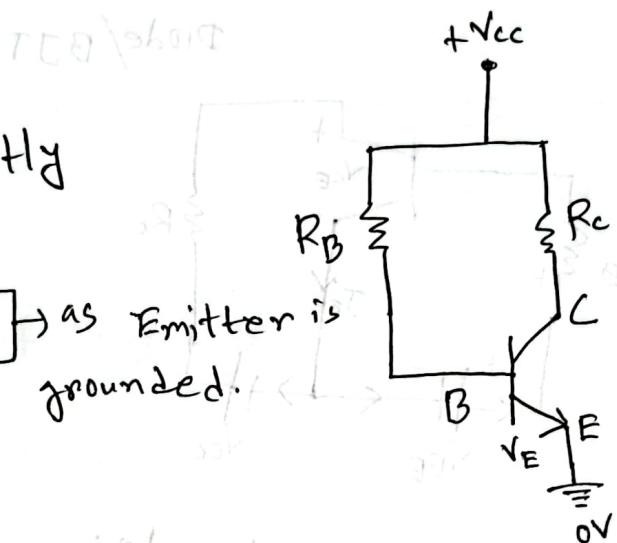
BJT DC Biasing (Chapter-4)

06.11.2024

1. Fixed Bias: i) in this, R_B , R_C resistors both are connected to V_{CE}

ii) Emitter is directly grounded.

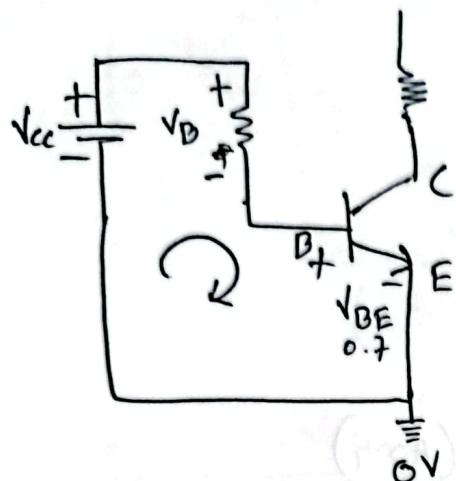
$$V_{E0} = 0V \rightarrow \text{as Emitter is grounded.}$$



Q. Why is DC Biasing Done?



Calculate ν_E , ν_B , ν_C , I_c , I_D , I_E , ν_{CE} ?



RVL_1

$$-V_{CC} + I_D R_B + V_{BE} = 0$$

$$\therefore I_D = \frac{V_{CC} - V_{BE}}{R_B} \quad 1$$

$$\therefore I_C = \beta I_B$$

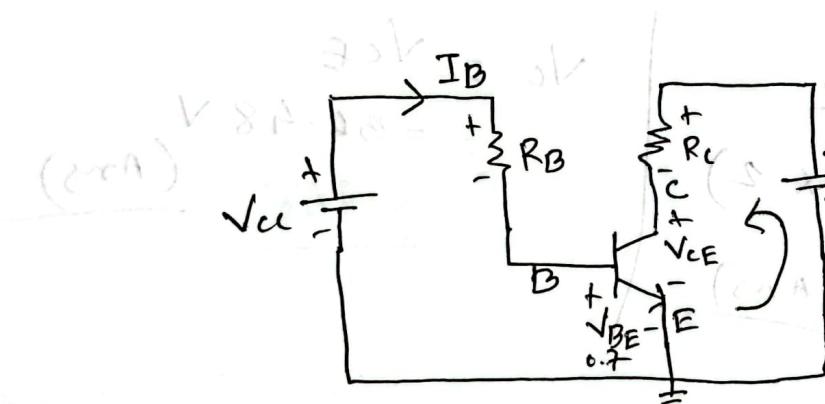
$$I_C \approx I_E$$

2

3

$$V_{BE} = V_B - V_{E0} \cancel{\approx}$$

$$\therefore V_B = V_{BE} = 0.7V$$



$$-V_{CC} + R_C I_C + V_{CE} = 0$$

$$\text{or, } V_C = V_{CC} - I_C R_C \quad 4$$

$$\text{or, } V_{CE} = V_{CC} - I_C R_C$$

$$\therefore V_{CE} = V_{CC} - V_C \quad 5$$

Input	Output
2. $I_D = \frac{V_{CC} - V_{BE}}{R_B}$	2. $V_{CE} = V_{CC} - V_C$
2. $I_C = \beta I_B$	2. $V_{CE} = V_{CC} - I_C R_C$
3. $I_E \approx I_C$	2. $V_C = V_{CE} = V_{CC} - I_C R_C$

practice Math:

$$V_{CC} = +25V$$

$$R_B = 50k\Omega$$

$$R_C = 2k\Omega$$

$$\beta = 90$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15 - 0.7}{50} = 0.286 \text{ mA (Ans)}$$

$$I_E = 90 \times 0.286 = 25.74 \text{ mA (Ans)}$$

$$I_E = 25.74 \text{ mA } [\because I_E \approx I_e] \quad (\text{Ans})$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_E R_C \\ &= 15 - (25.74 \times 2) \\ &= -36.48 \text{ V} \quad (\text{Ans}) \end{aligned}$$

$$\begin{aligned} V_C &= V_{CE} \\ &= -36.48 \text{ V} \quad (\text{Ans}) \end{aligned}$$

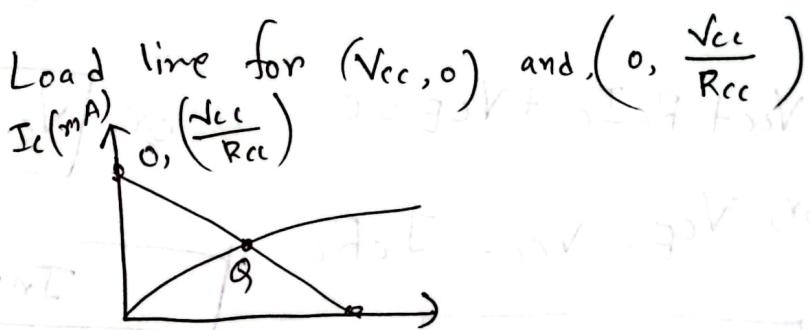
$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

$$\text{When, } I_C = 0$$

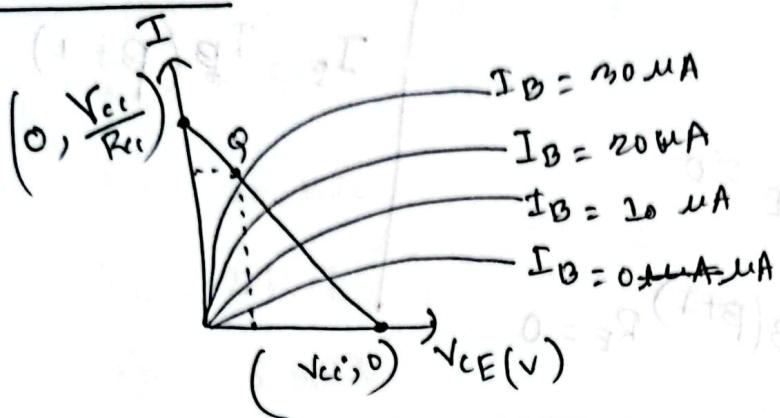
$$V_{CE\max} = V_{CC}$$

$$\text{and, } V_{CE} = 0, I_{C\max} = \frac{V_{CC}}{R_C}$$



$I_{C\max}$ or I_c saturation \Rightarrow
 $I_{C\text{sat}} \approx 35$

Example - 4.3



$$I_C = \frac{V_{CE}}{R_C}$$

$$\text{or, } R_C = \frac{20 \text{ V}}{10 \text{ mA}} = 2 \text{ k}\Omega$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

$$\text{or, } R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{20 - 0.7}{25 \mu A}$$

$$I_C = 10 \text{ mA}$$

$$R_B = ?$$

$$R_C = ?$$

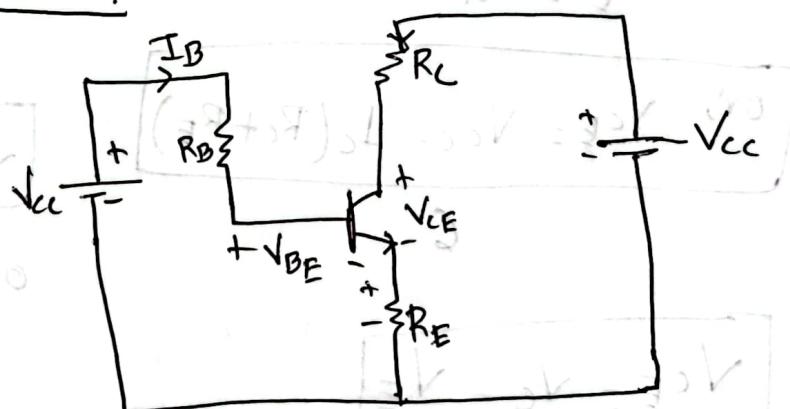
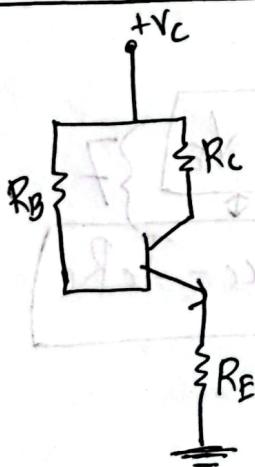
$$\sqrt{V_{CE}} = 20 \text{ V}$$

$$3V + 38V = 41V$$

BJT DC Biasing

Lec - 7
10.11.2024

2. Emitter Stabilized Bias:



Input:

Applying KVL,

$$-V_{cc} + I_B R_B + V_{BE} + I_E R_E = 0$$

or, $-V_{cc} + I_B R_B + V_{BE} + I_B (\beta+1) R_E = 0$ $R_E = 0$

$$I_E = I_B (\beta+1)$$

$$\therefore I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_E} \quad (1)$$

$$I_C = \frac{\beta I_B}{2}$$

and $I_E \approx I_C$

(3)

$$\therefore V_E = I_E R_E \quad (4)$$

$$V_{BE} = V_B - V_E$$

$$\therefore V_B = V_{BE} + V_E \quad (5)$$

Output:

$$-V_{cc} + R_C \times I_C + V_{CE} + I_E R_E = 0$$

or, $V_{CE} = V_{cc} - I_C R_C - I_E R_E$

$$\text{or, } V_{CE} = V_{cc} - I_C (R_C + R_E) \quad (6)$$

$$V_C = V_{CE} + V_E \quad (7)$$

or, $V_C = V_{cc} - I_C R_C$

and

$$V_{CE} = V_C - V_E \quad (6)$$

Given, $\beta = 200$

$$V_{BE} = 0.7$$

$$V_{CC} = 20V$$

$$R_B = 200k\Omega$$

$$R_C = 2k\Omega$$

$$R_E = 1.5k\Omega$$

Using standard values (and $\frac{1}{20+2} \approx 5\%$)

$$\textcircled{1} I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 2) R_E} = \frac{20 - 0.7}{200 + (200+2) \times 1.5} = 0.054mA$$

Using $I_C = \beta I_B$

$$\textcircled{2} I_C = 200 \times 0.054 = 5.4mA$$

$$\textcircled{3} I_E \approx I_C = 5.4mA$$

$$\textcircled{4} V_E = I_E \times R_E = (5.4 \times 1.5) = 8.1V$$

$$\textcircled{5} V_C = V_{CC} - I_E R_C = 20 - (5.4 \times 2) = 9.2V$$

$$\textcircled{6} V_{CE} = V_C - V_E = (9.2 - 8.1)V = 1.1V$$

$$\textcircled{7} V_B = V_{BE} + V_E = 0.7 + 8.1 = 8.8V$$

Load-line:

When, $I_C = 0$

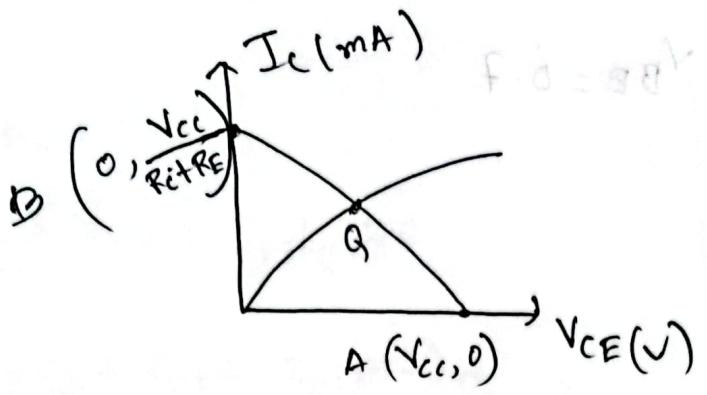
$$(V_{CE}, I_C) = (V_{CC}, 0)$$

when,

$V_{CE} = 0$

$$I_{CC} = \frac{V_{CC}}{R_C + R_E}$$

$$\therefore (V_{CE}, I_C) = \left(0, \frac{V_{CC}}{R_C + R_E} \right)$$



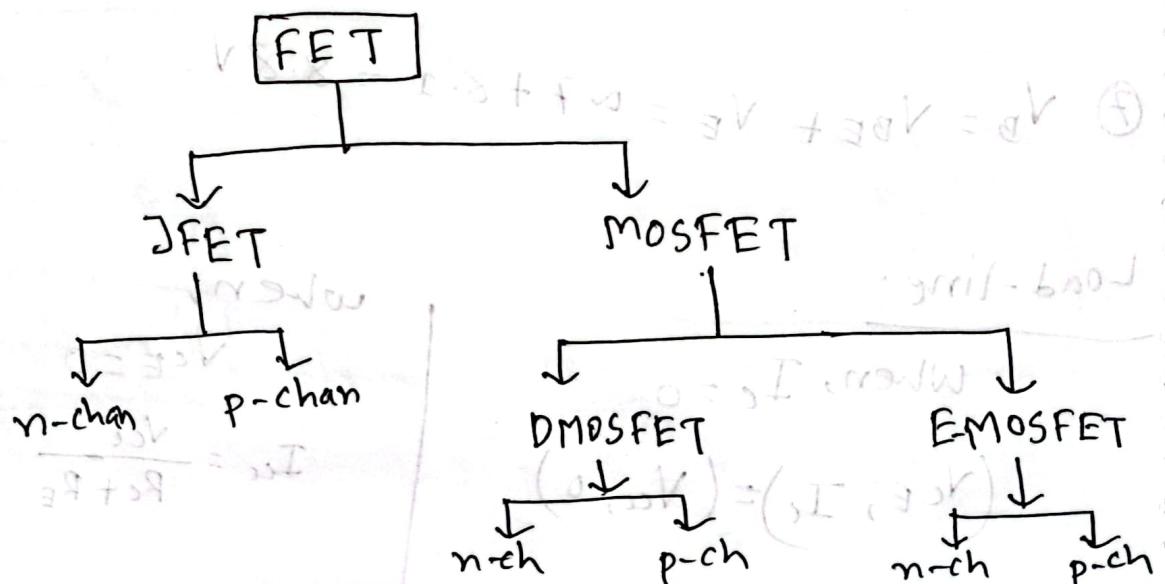
$$(I_{C_{sat}} = \frac{V_{ce}}{R_{fe} + R_E}) \text{ (Ex. 4.5)} \quad \boxed{\text{H.W. Example - 4.21}}$$

Emitter stabilized bias provide more stability than fixed bias. As it increases the output voltage and current remains closer to the point they were set by applying DC bias. Despite change in temperature and P-factor.

Lecture - 8

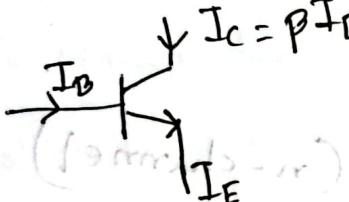
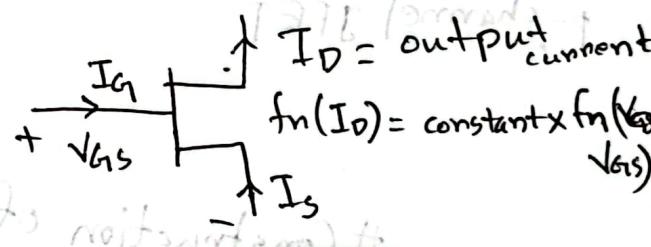
13.11.2024

Field Effect Transistor.

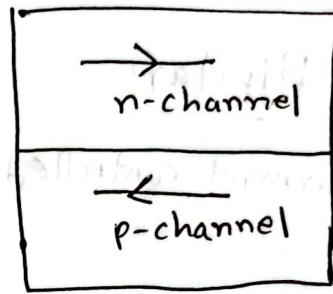
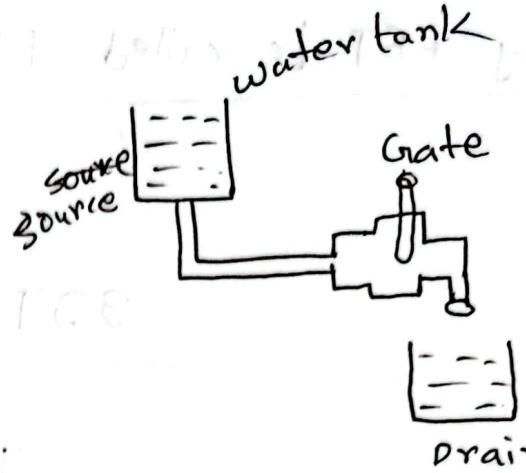
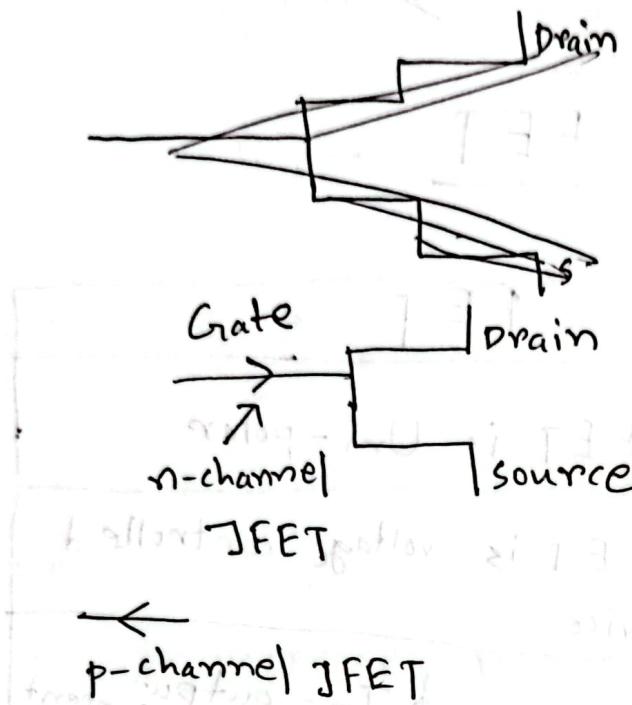


Q. Why FET is called FET?

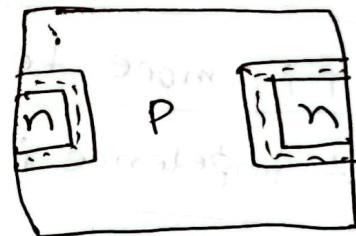
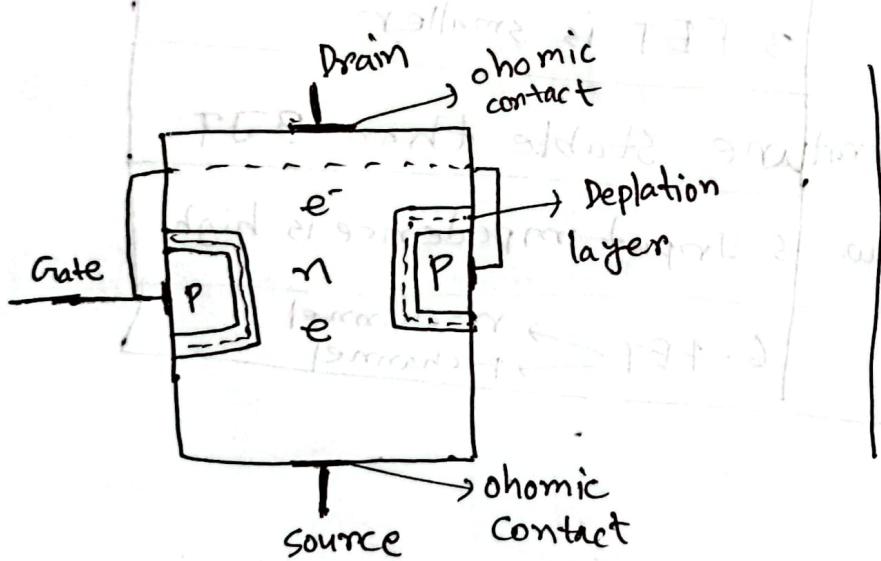
BJT vs FET

BJT is	FET
1. BJT is Bipolar Device	1. FET is Uni-polar Device
2. BJT is current controlled Device	2. FET is voltage controlled Device
$I_c = \beta I_B$ 	$I_D = \text{output current}$ $f_n(I_D) = \text{constant} \times f_n(V_{GS})$ I_S 
3. BJT is bigger	3. FET is smaller
4. FET is more temperature stable than BJT.	
5. Input impedance is low.	5. Input impedance is high.
6. BJT → npn → pnp	6. FET → n-channel → p-channel

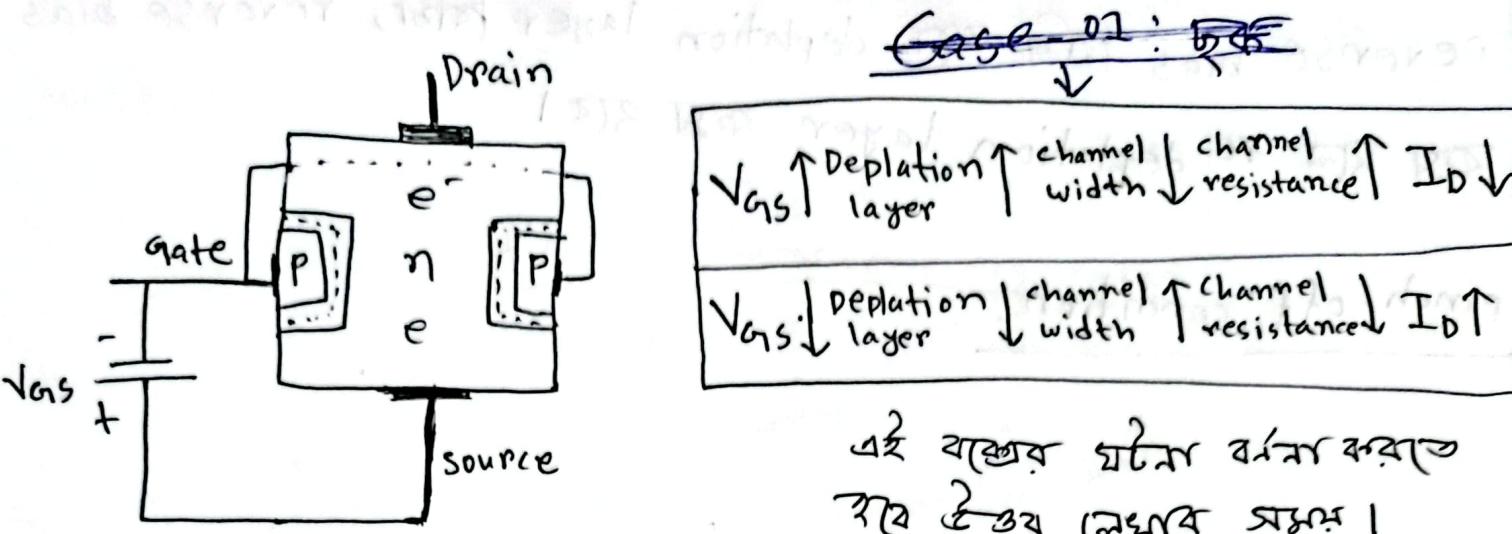
Symbol of JFET:



Construction of a JFET (n-channel)



Basic Working: Q. Explain why JFET is voltage controlled device?



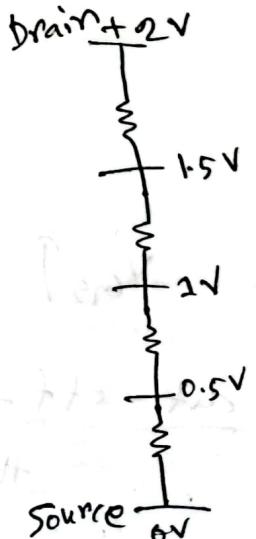
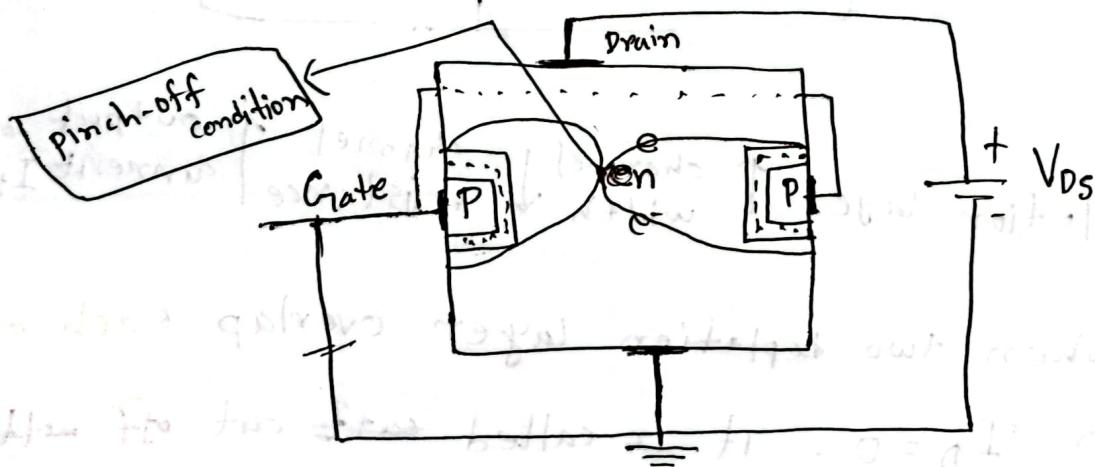
Get to source voltage V_{GS} , controls the flow of current I_D , "Gate" is always reversed bias. This is done due to two reasons

1. To set-up depletion layer.
2. To make the impedance high, so that $I_G = 0$, therefore

$$I_D \approx I_S$$

Detailed working of JFET (n-channel)

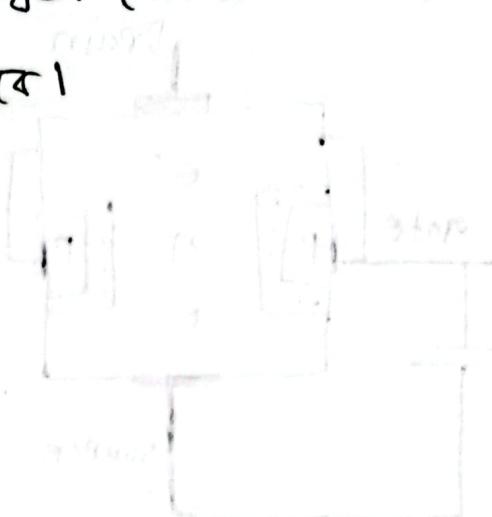
Case - 02: $\rightarrow V_{GS} = 0$ { Gate is directly connected to source }



reverse bias तरीके इलूटिलो डेप्लेशन लेयर कर, reverse bias
कर्म इलूटिलो डेप्लेशन लेयर कर देता

pinch-off condition:

तब तक जब डेप्लेशन लेयर बढ़ता है तब वह चैनल को कम कर देता है।



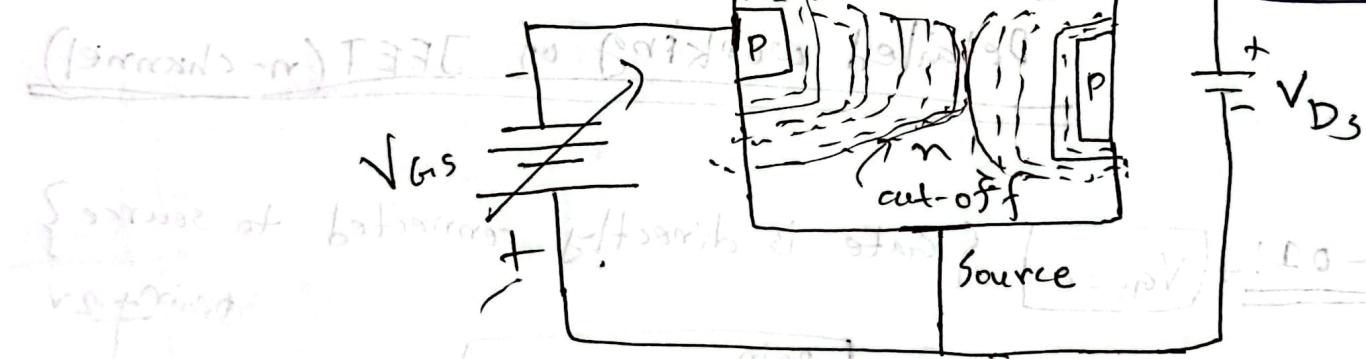
वॉल्टेज एवं अन्तर्गत pinch-off condition के लिए (अब) pinch-off voltage.

Q. Explain the process of the depletion layer, when setup $V_{GS} = 0$

Lecture - 9

17.11.2024

#Case-2 Gate is reverse biased, $\therefore V_{GS} < 0V$



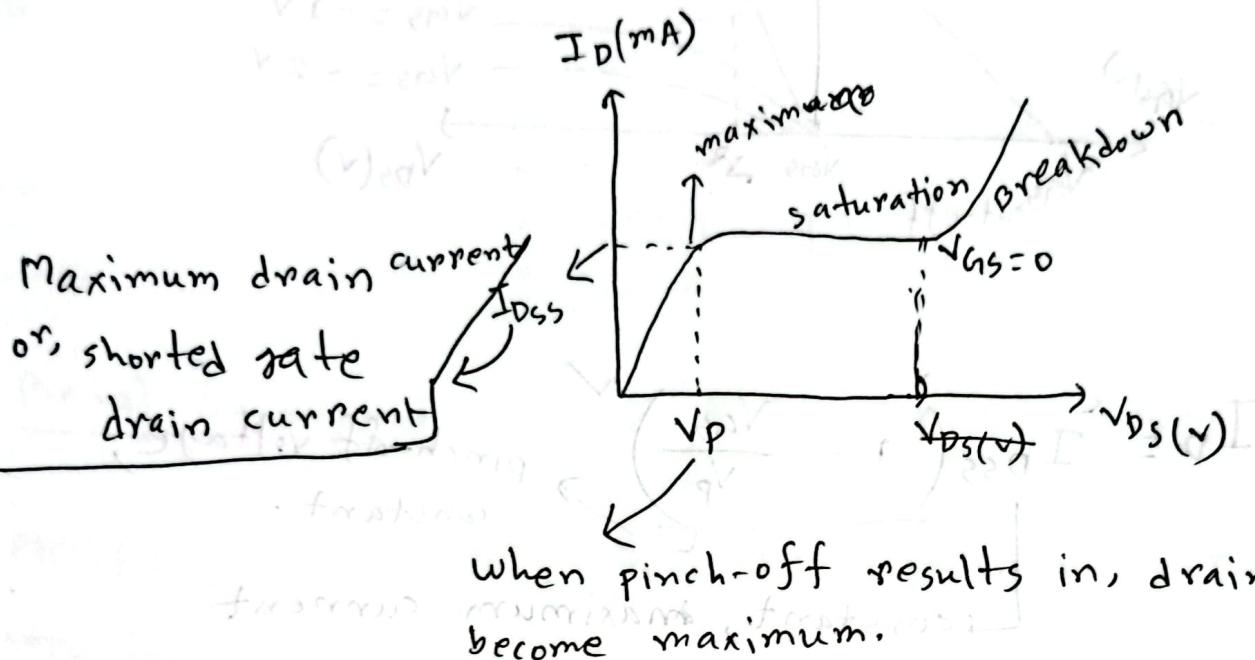
$V_{GS} \uparrow$ depletion layer \uparrow channel width \downarrow channel resistance \uparrow output current $I_D \downarrow$

Cut-off \rightarrow when two depletion layer overlap each other
then $I_D = 0$. it is called ~~cut~~ cut-off voltage condition

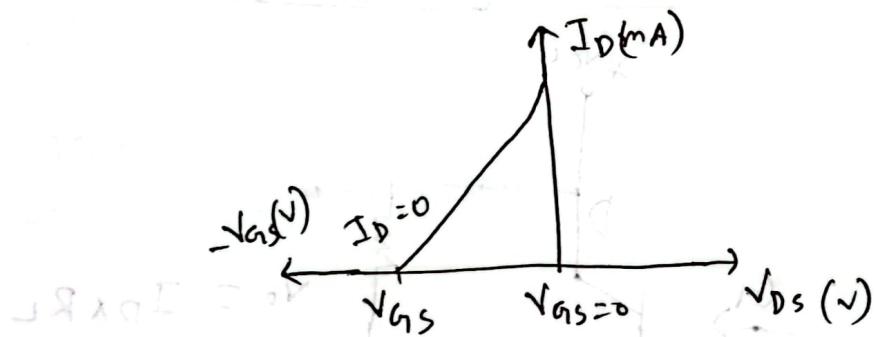
V_{GS} এবং V_{DS} দ্বারা নির্ভুল কেন্দ্র প্রতিরোধ $V_{DS\text{ cut-off}}$

$$V_{GS} = 0$$

Drain characteristics curve



Gate characteristics curve



from formula (প্রতিক্রিয়া):

when,

$$V_{GS} = 0$$

$$I_D = I_{DSS}$$

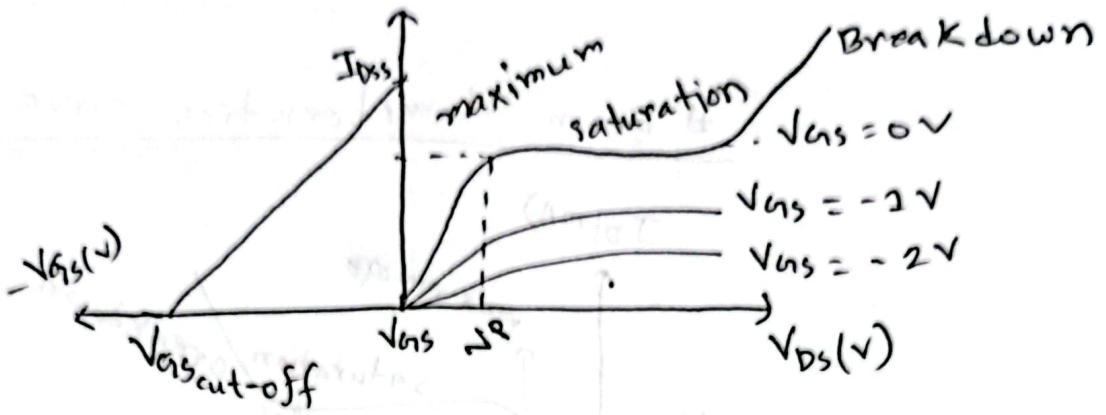
when,

$$V_{GS} = V_P$$

$$I_D = 0$$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

Both curve characteristics



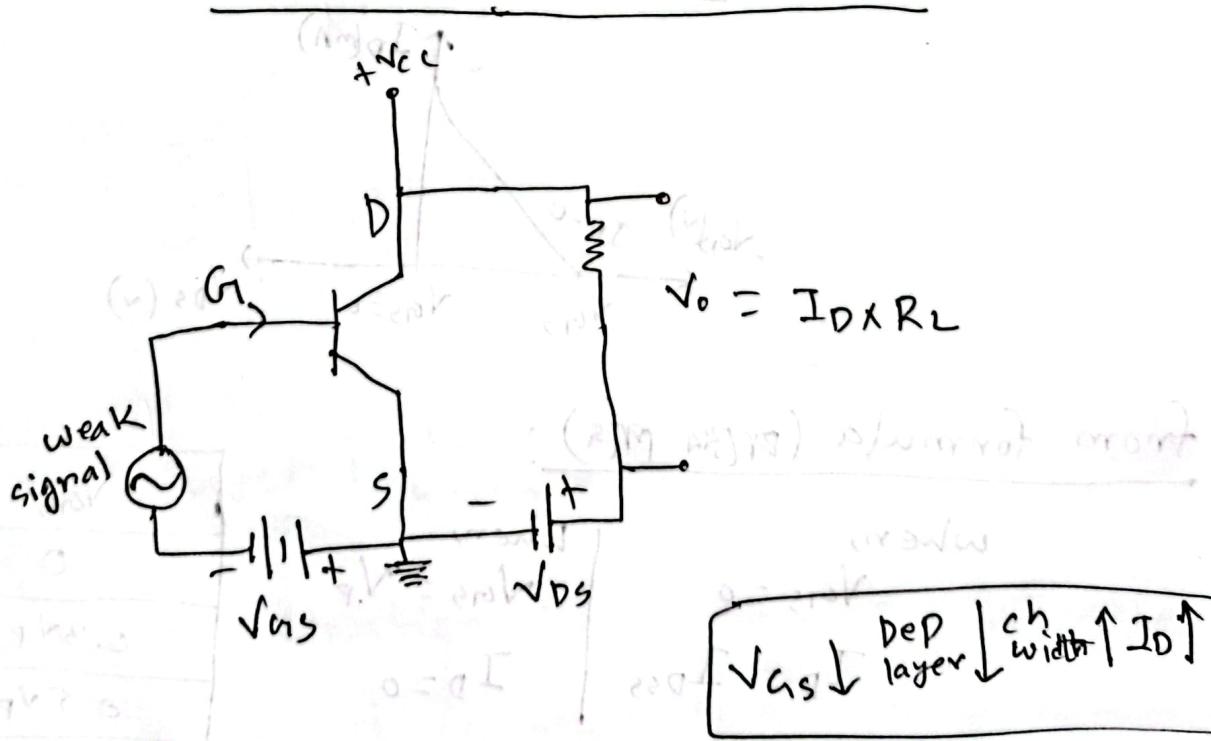
formul a:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)$$

pinchoff voltage, constant.

constant, maximum current

JFET as an amplifier



During (+) half of the input,

$$i) +2V - 3V = -1V$$

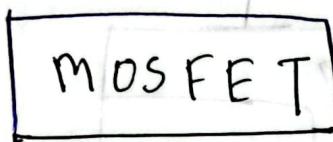
$$ii) 0V - 3V = -3V$$

During (-) half of the input,

$$i) -2V - 3V = -5V$$

$$ii) 0V - 3V = -3V$$

common source is widely used



Lecture - 20

no. 22. 2024

Metal oxide semiconductor field-effect transistor.

MOSFET is a field effect transistor with a MOS structure.

MOSFET have two types:

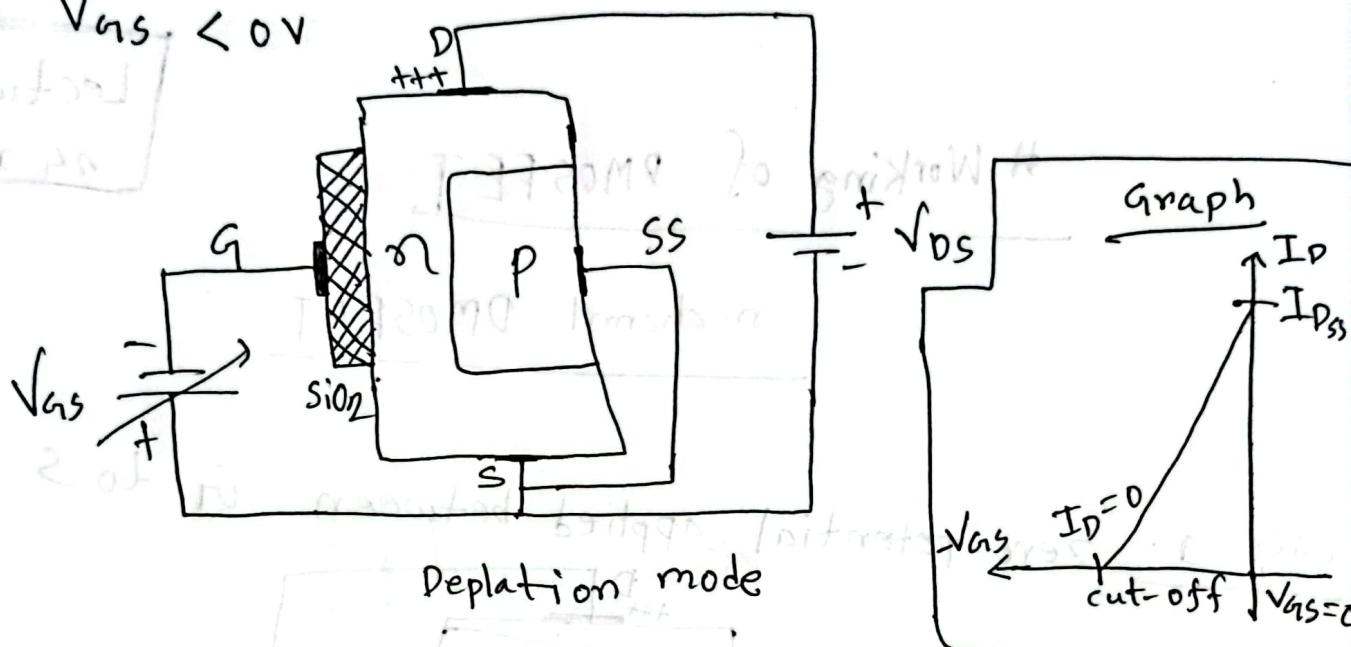
1. DMOSFFT \rightarrow Depletion type MOSFET

2. PFE-MOSFFT \rightarrow Enhancement type MOSFET

Gate के forward bias करने पर इनपुट विद्युत विपरीत गेट के reverse bias करने पर गेट का current flow होता है।

Case-2: negative potential is applied between G to S

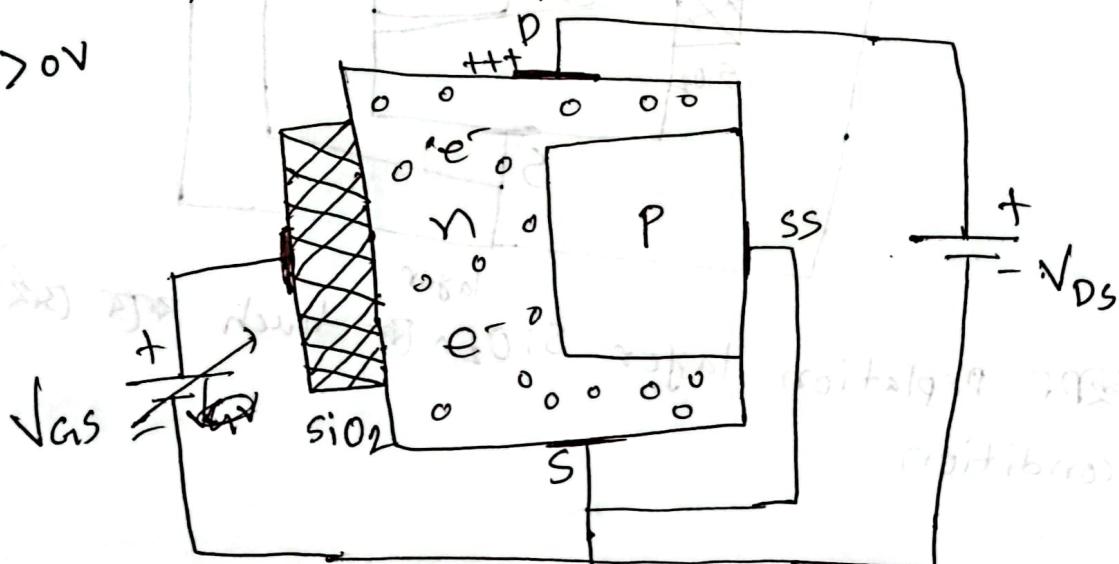
Here, $V_{GS} < 0V$



JFET (or) depletion mode-এ কাণ্ড মাঝে কিৰা? Explain ...

Case-3: positive potential is applied G to S ...

$V_{GS} > 0V$



Enhancement mode

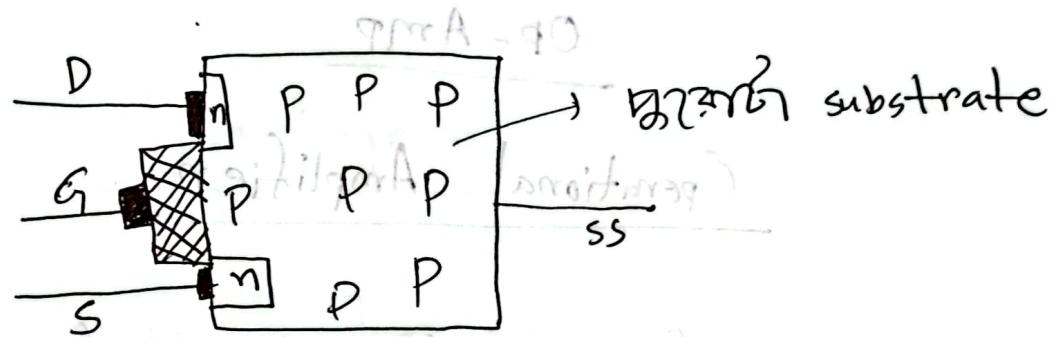
DMOSFET কি enhancement mode-এ কাণ্ড কৰিব পাৰ?

E-MOSFET

Enhancement - MOSFET

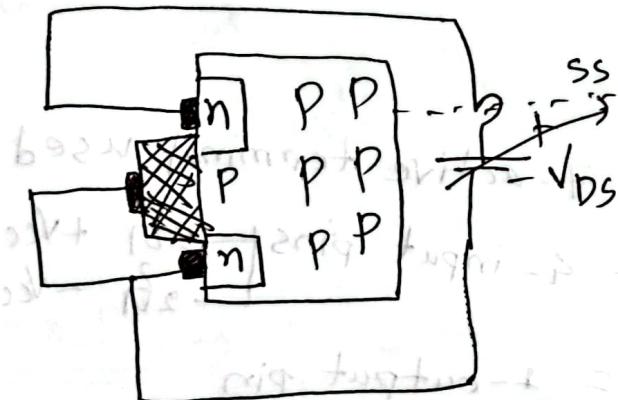
Construction: no-pre existing channel in E-MOSFET

n-channel



Case - 1:

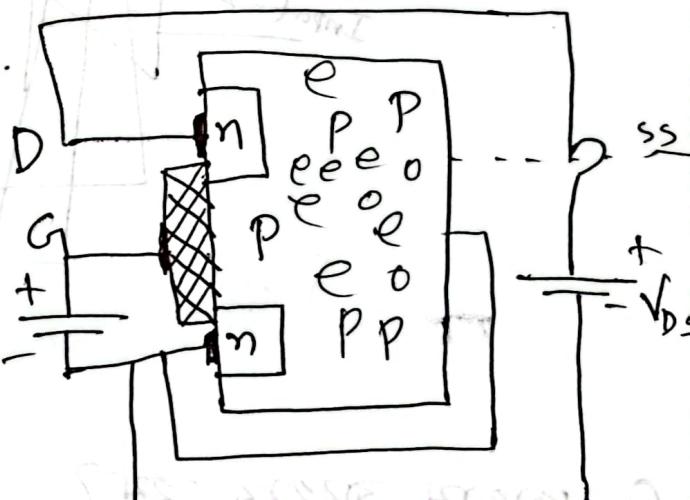
$$V_{GS} = 0$$



$I_D = 0$
no-channel is present

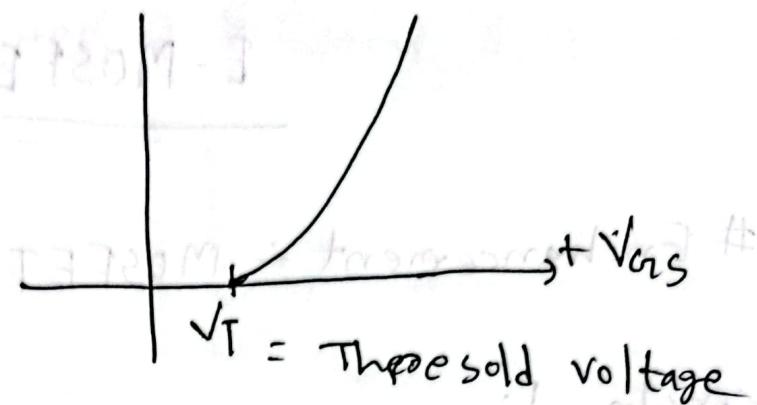
case :- 2:

$$V_{GS} > 0V$$



$$I_D = K(V_{GS} - V_T)^{\gamma}$$

$$\therefore K = \frac{I_D (\text{on})}{(V_{GS} - V_T)^{\gamma}}$$



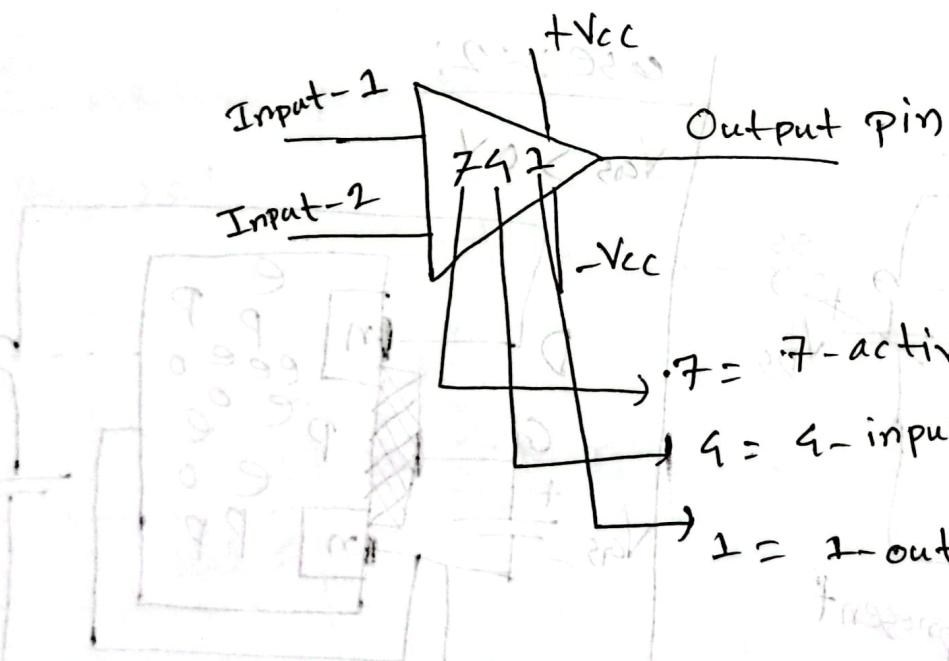
OP-Amp

Operational Amplifier

Lecture-12

27.11.2024

⇒ Voltage amplifier \rightarrow Ic circuit (8pin IC)



Q. কোনভাবে কার্যকর হবে?

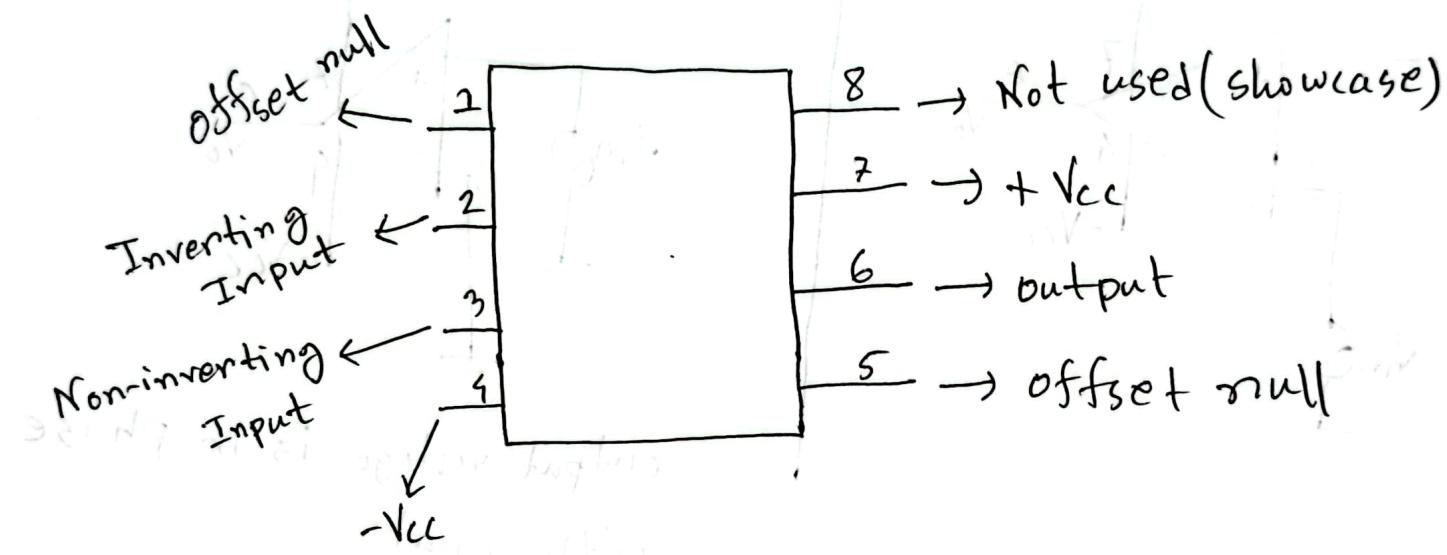
1. Mathematical :
 - i) Addition
 - ii) Subtraction
 - iii) Integration
 - iv) Differentiation

2. Oscilloscope

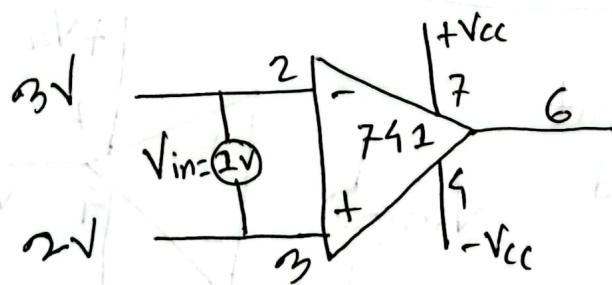
Analog to Digital conversion
3. ADC, DAC → Digital to Analog conversion

4. Voltage Follower/ Buffer || 5. Voltage comparator

pin diagram



symbol: → Differential amplifier എന്തു?



Again,

$$A = \frac{\text{Output}}{\text{input}}$$

|∴

$$A = \frac{V_o}{V_{in}}$$

→ differential input

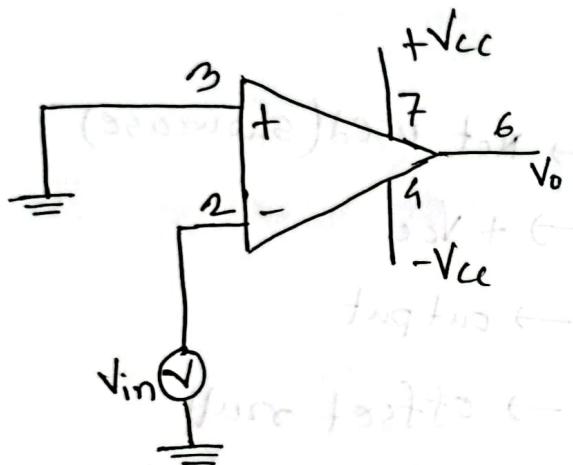
#Input modes of Op-Amp:

1. Inverting mode

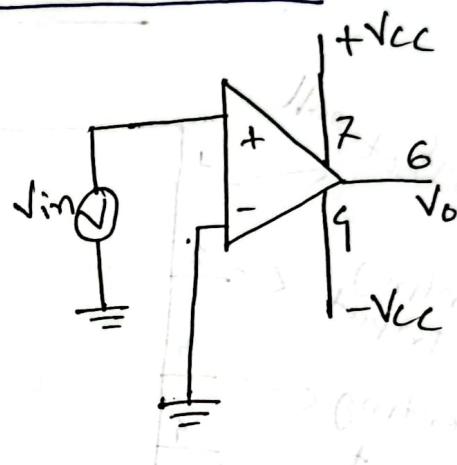
2. Non-inverting mode

3. Common mode

1. Inverting



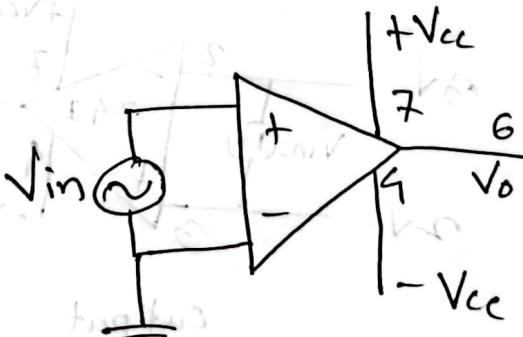
2. Non-inverting



output voltage is in phase with input

3. Common mode:

In common mode, output will be zero volt and again $A = 0$



$$\begin{aligned} V_o &= V_2 - V_3 \\ &= 0 - 0 \\ &= 0 \end{aligned}$$

$$\therefore V_o = -V_2$$

$$V_o = -AV_2 \rightarrow \text{Inverting mode}$$

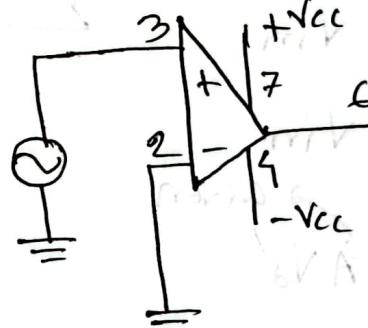
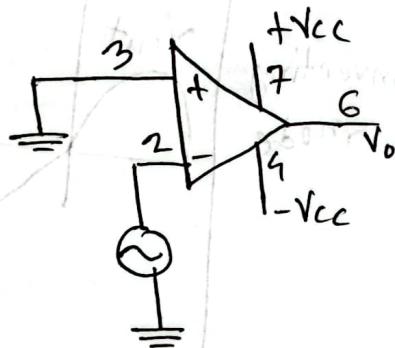
$$V_o = AV_2 \rightarrow \text{Non-inverting mode}$$

\therefore output voltage = gain \times differential voltage

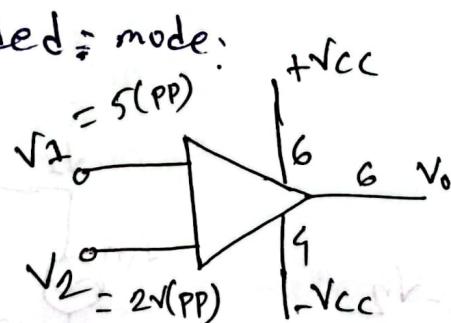
Operation mode

1. Differential mode:

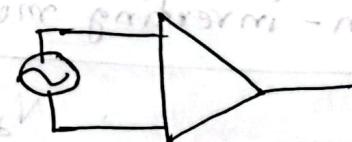
i) single ended mode:



ii) Double ended mode:



2. Common mode

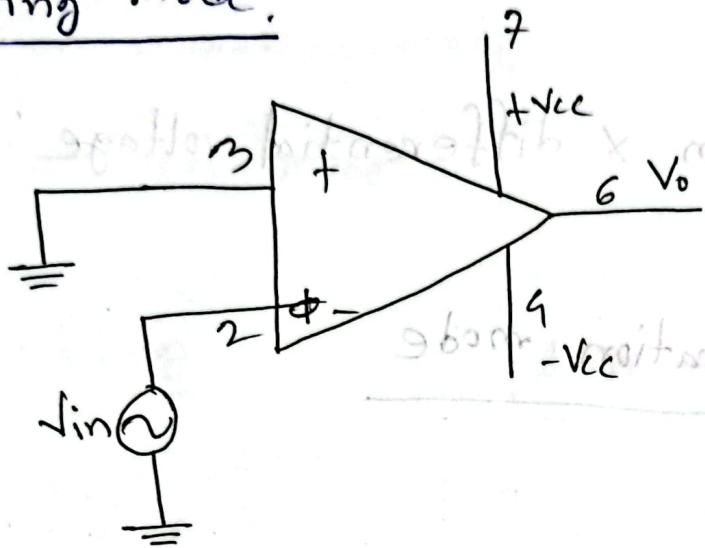


Characteristics Curve

Lecture-13

01.12.2024

Inverting mode:



$$V_d = V_2 - V_2$$

$$= 0 - V_{in}$$

$$\therefore V_d = -V_{in}$$

$$\therefore V_o = A V_d$$

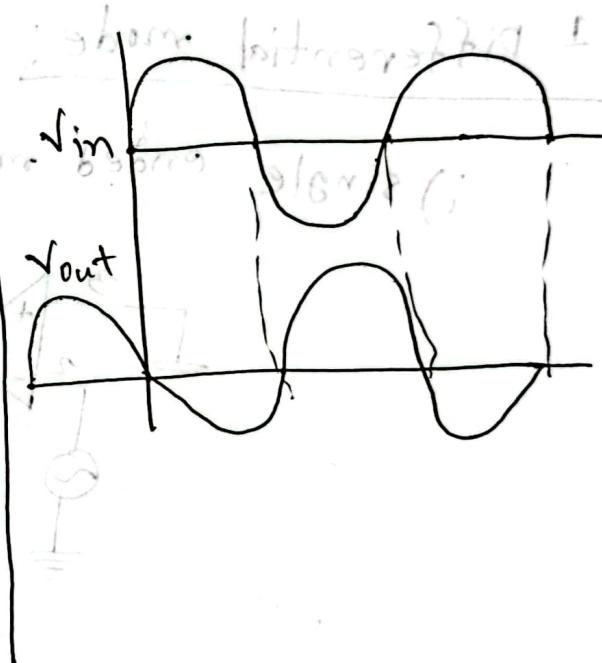
$$= A \times (-V_{in})$$

↳ differential input

$$\therefore V_o = -AV_{in}$$

for inverting mode

Graph



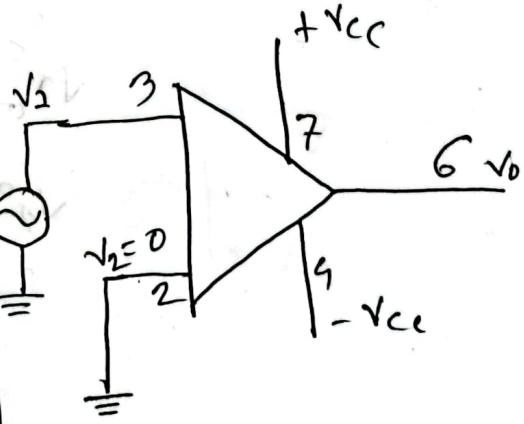
Non-inverting mode:

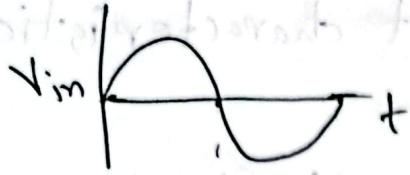
$$\therefore V_d = V_2 - V_2$$

$$= V_{in}$$

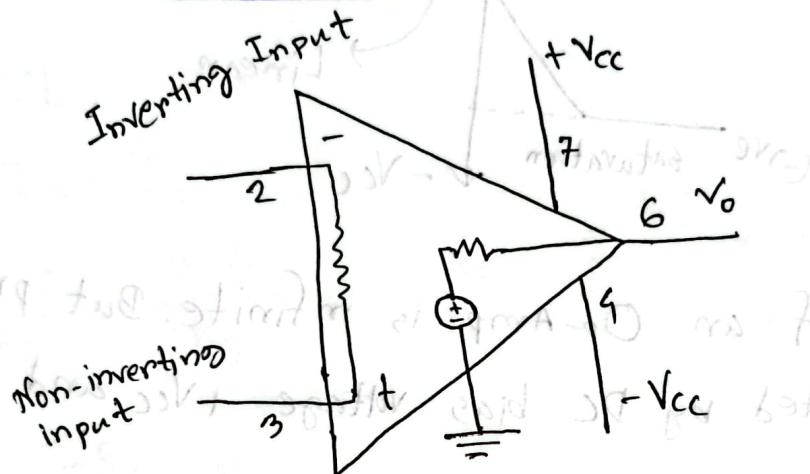
$$\therefore V_o = AV_d$$

$$\therefore V_o = AV_{in}$$





Equivalent Circuit

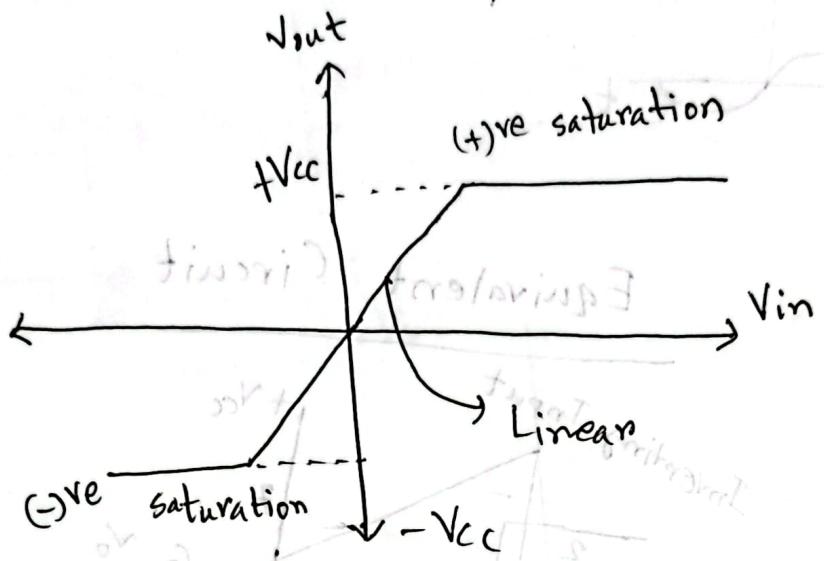


Ideal characteristic:

1. Voltage gain $A = \infty \rightarrow A = \frac{V_o}{V_d} \left[10^5 - 10^8 \right]$
2. Input impedance, $R_{in} = \infty$
3. Output " ", $R_{out} = 0$
4. Slew rate = ∞
5. CMRR = $\infty \rightarrow$ (common mode rejection ratio) $CMRR = \frac{ACM}{ADM}$
6. Bandwidth = $\infty \rightarrow$ filter ফিল্টার ব্যবহার করা যায়।

Voltage Transfer curve / Input-Output characteristics curve / Transconductance Curve

input-output (प्रिवेट)



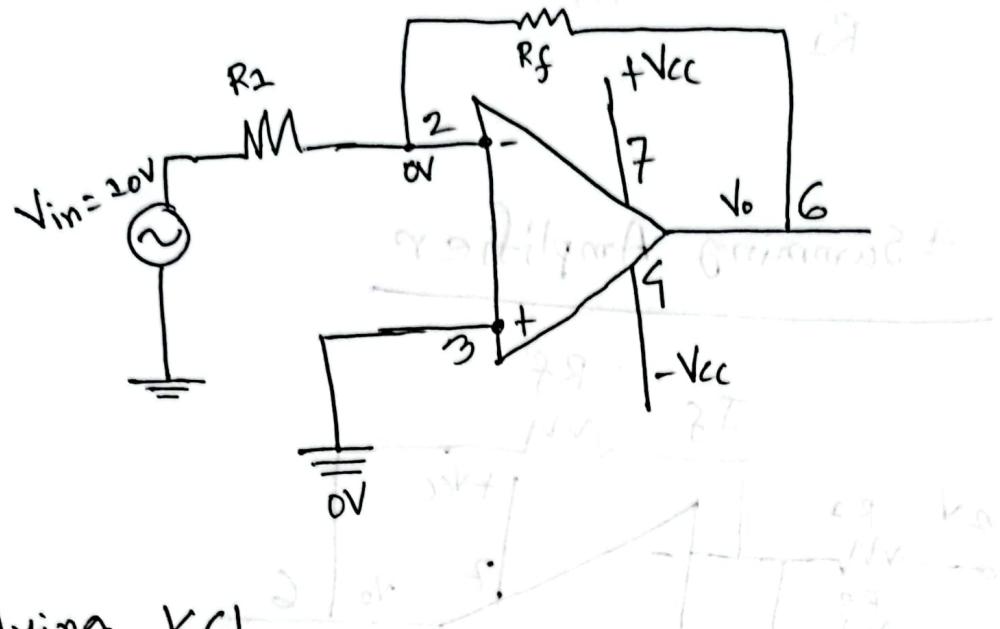
Ideally, gain of an Op-Amp is infinite. But practically output voltage is limited by DC bias voltage $+V_{CC}$ and $-V_{CC}$

Op-Amp can operate in 3 regions:

1. Positive saturation $\rightarrow V_o \cong +V_{CC}$
2. Linear sat region $\rightarrow -V_{CC} \leq V_o \leq +V_{CC}$
3. Negative Saturation $\rightarrow V_o \cong -V_{CC}$

Q. Explain inverting Amplifier with symbol and derivation?

Inverting Amplifier



Applying KCL,

$$I_{in} = I_f$$

$$\frac{V_{in} - 0}{R_2} = \frac{0 - V_o}{R_f} \quad \therefore V_o = \frac{-R_f}{R_2} \times V_{in}$$

$$V_o = \frac{-R_f}{R_2} \times V_{in}$$

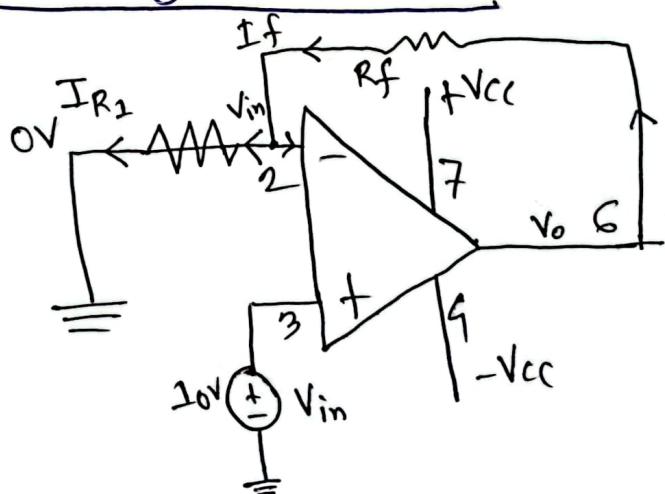
A
- মুক্ত করার ১৮০° ইনভের্ট

Non-inverting Amplifier

Applying KCL,

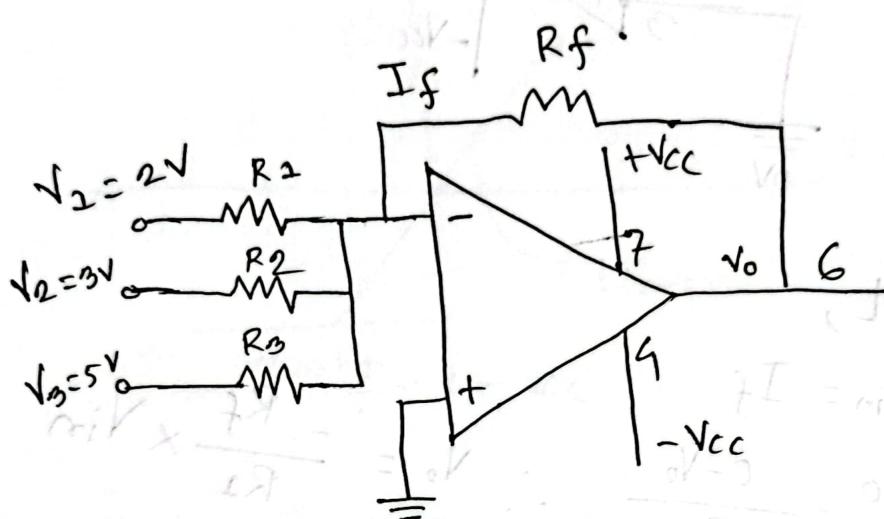
$$I_f = I_{R_2}$$

$$\Rightarrow \frac{V_o - V_{in}}{R_f} = \frac{V_{in} - 0}{R_2}$$



$$\therefore V_o = \frac{V_{in} \times R_f}{R_2} + V_{in}$$

Summing Amplifier



$$V_o' = \frac{-R_f}{R_1} \times V_1$$

$$V_o = \left(\frac{-R_f}{R_1} \times V_1 \right) + \left(\frac{-R_f}{R_2} \times V_2 \right) + \left(\frac{-R_f}{R_3} \times V_3 \right)$$

$$V_o'' = \frac{-R_f}{R_2} \times V_2$$

$$= -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

$$V_o''' = \frac{-R_f}{R_3} \times V_3$$

eqn

