Block diagram of 8086

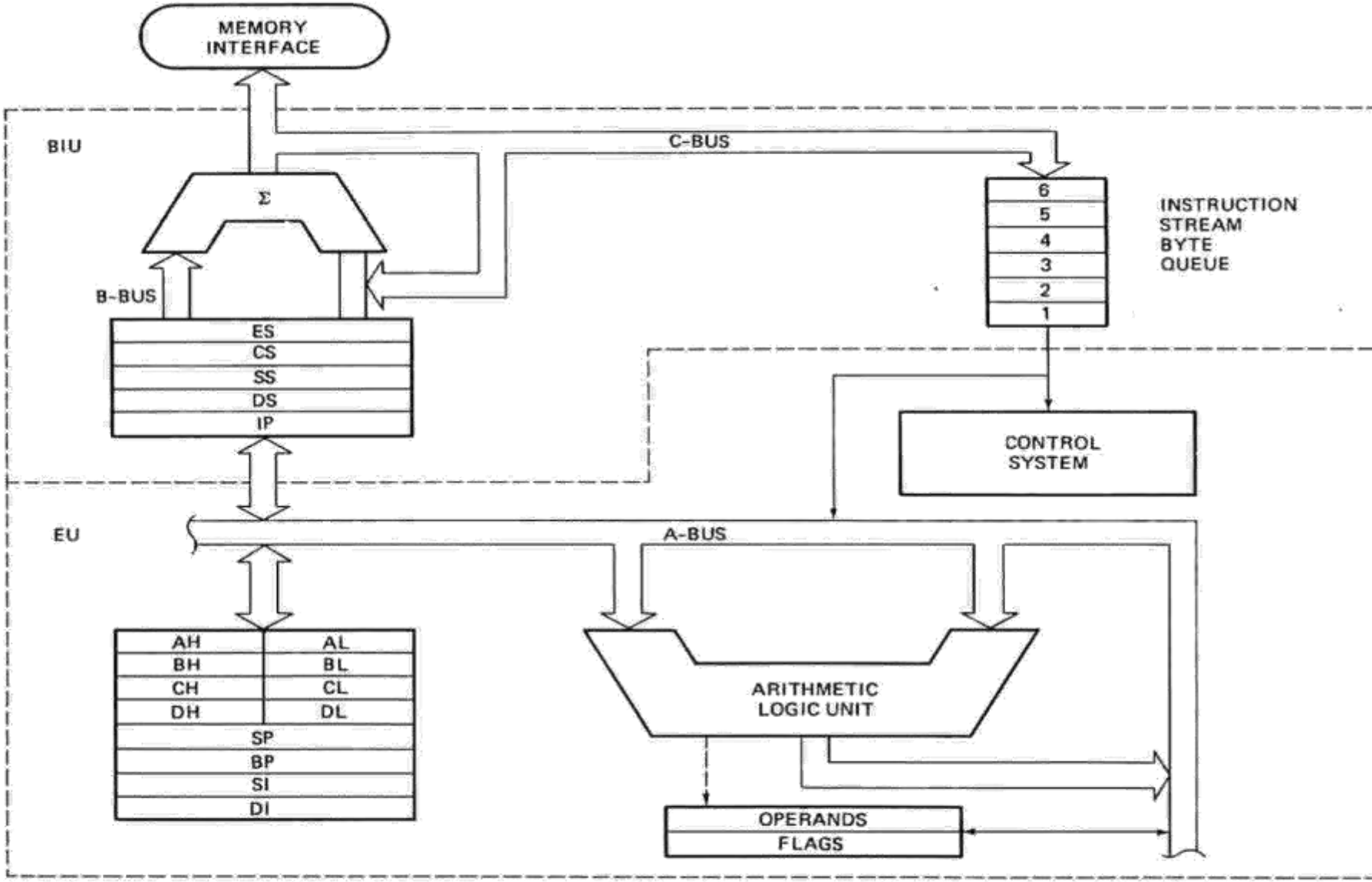
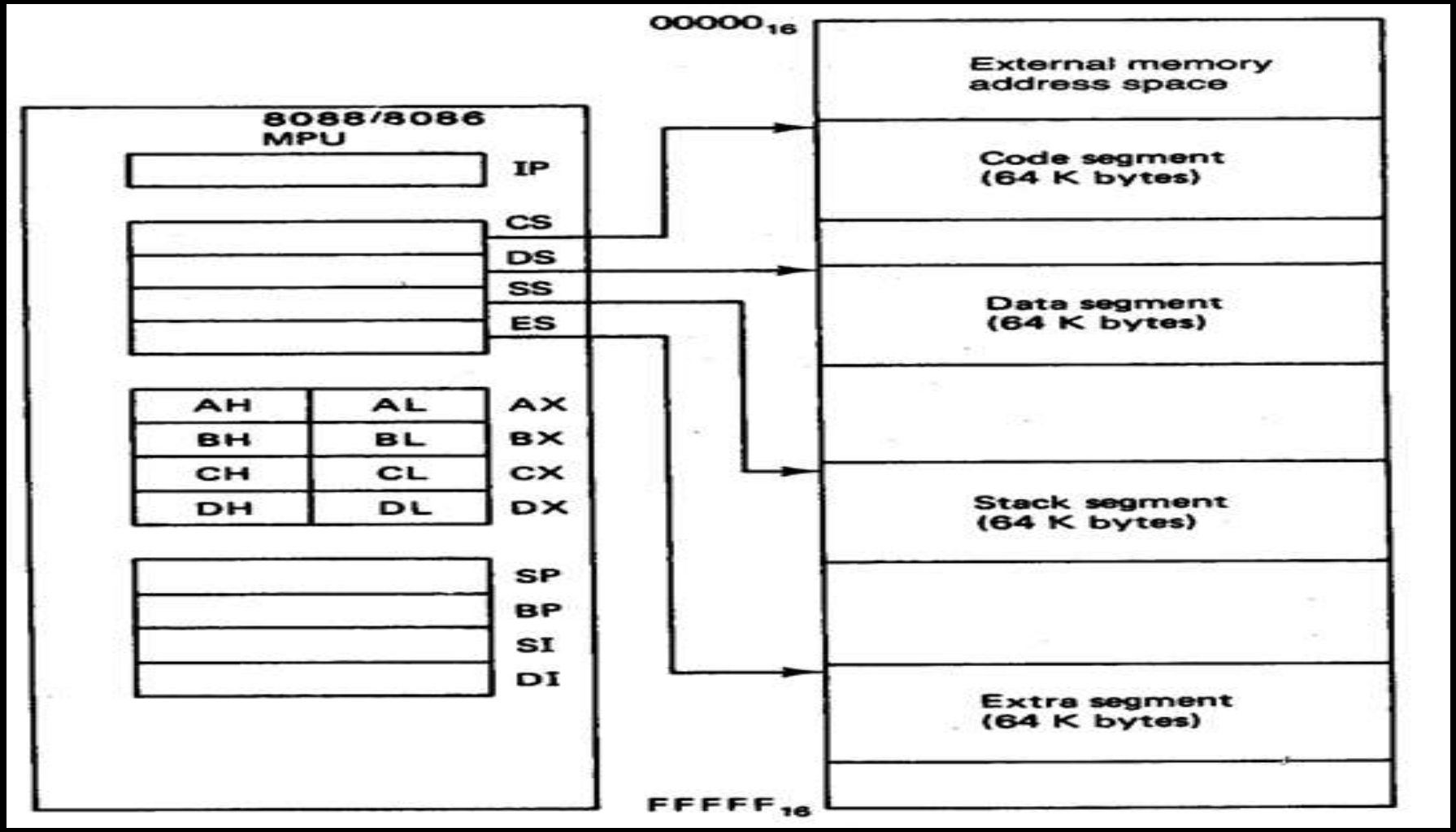
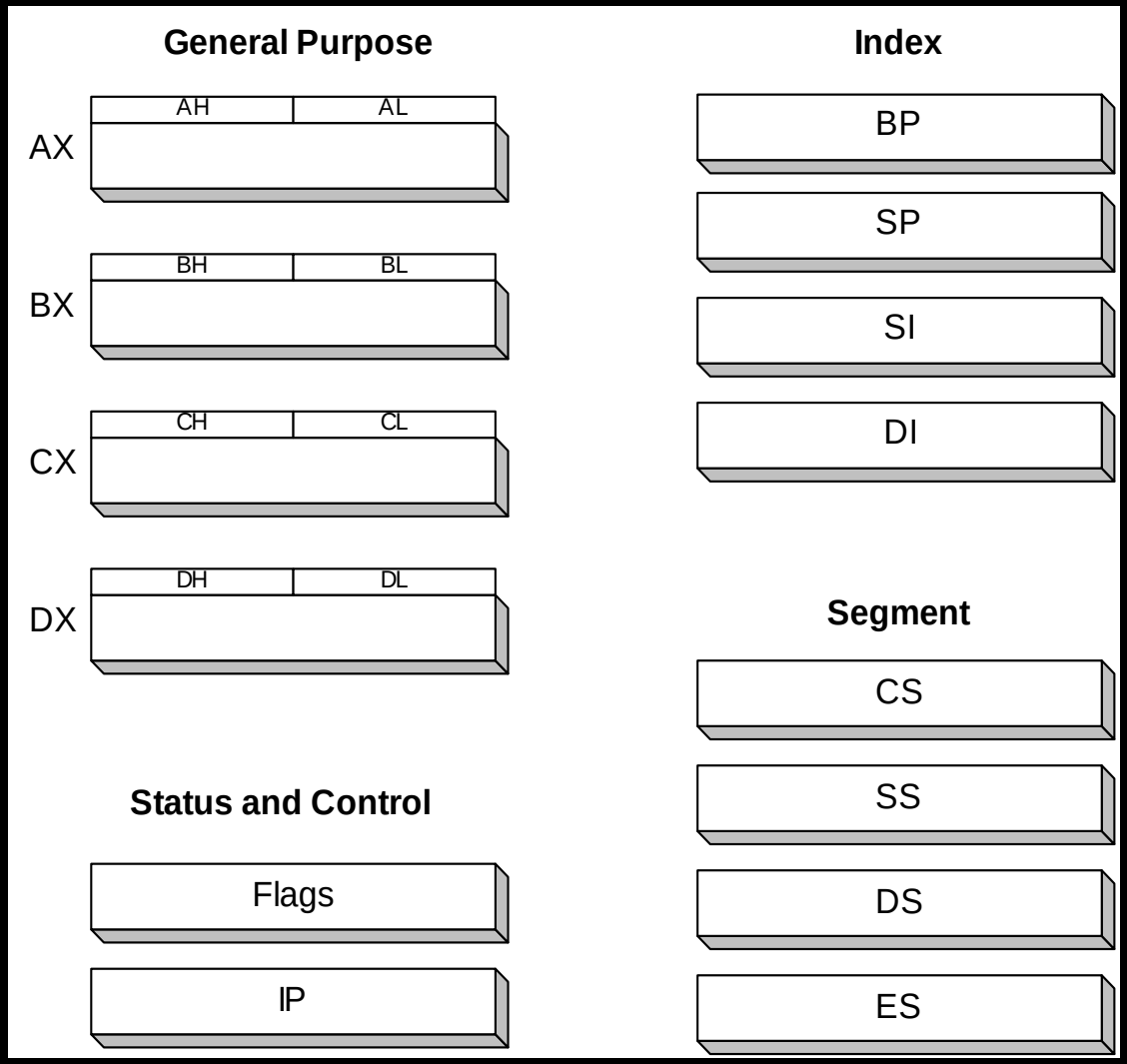


FIGURE 2-7 8086 internal block diagram. (*Intel Corp.*)

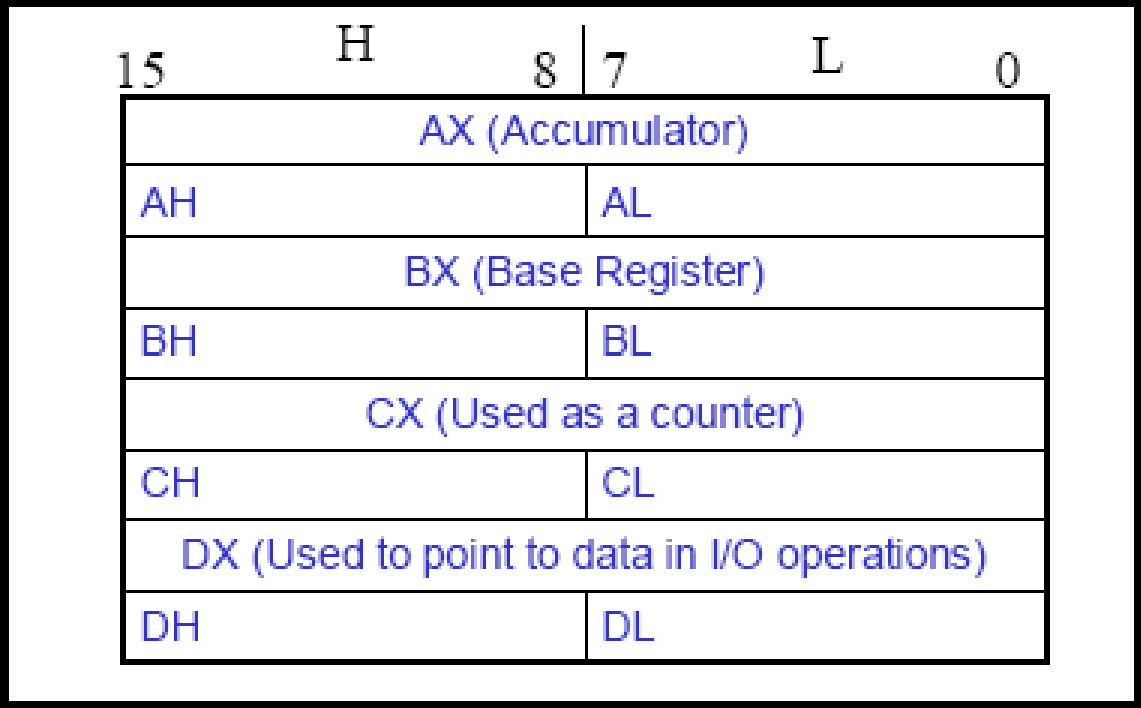
Software Model of the 8086 Microprocessors



8086 Registers



General Purpose Registers



AX - the Accumulator
BX - the Base Register
CX - the Count Register
DX - the Data Register

- Normally used for storing temporary results
- Each of the registers is 16 bits wide **(AX, BX, CX, DX)**
- Can be accessed as either 16 or 8 bits AX, AH, AL

General Purpose Registers

- **AX**
  - Accumulator Register
  - Preferred register to use in arithmetic, logic and data transfer instructions because it generates the shortest Machine Language Code
  - Must be used in multiplication and division operations
  - Must also be used in I/O operations
- **BX**
  - Base Register
  - Also serves as an address register

General Purpose Registers

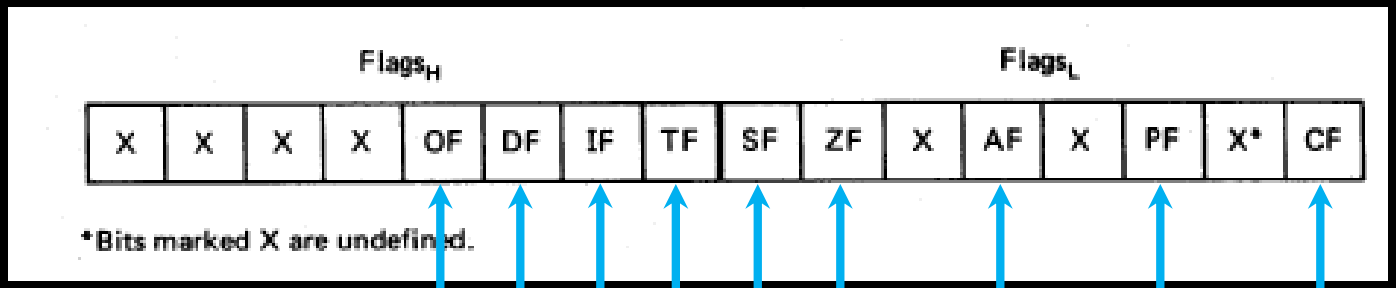
- **CX**
  - Count register
  - Used as a loop counter
  - Used in shift and rotate operations
- **DX**
  - Data register
  - Used in multiplication and division
  - Also used in I/O operations

Pointer and Index Registers

SP	Stack Pointer
BP	Base Pointer
SI	Source Index
DI	Destination Index
IP	Instruction Pointer

- All 16 bits wide, L/H bytes are not accessible
- Used as memory pointers
  - Example: MOV AH, [SI]
    - *Move the byte stored in memory location whose address is contained in register SI to register AH*
- IP is not under direct control of the programmer

Flag Register



Overflow

Direction

Interrupt enable

Trap

Sign

Zero

Auxiliary Carry

Parity

Carry

6 are status flags

3 are control flag

8086 Programmer's Model

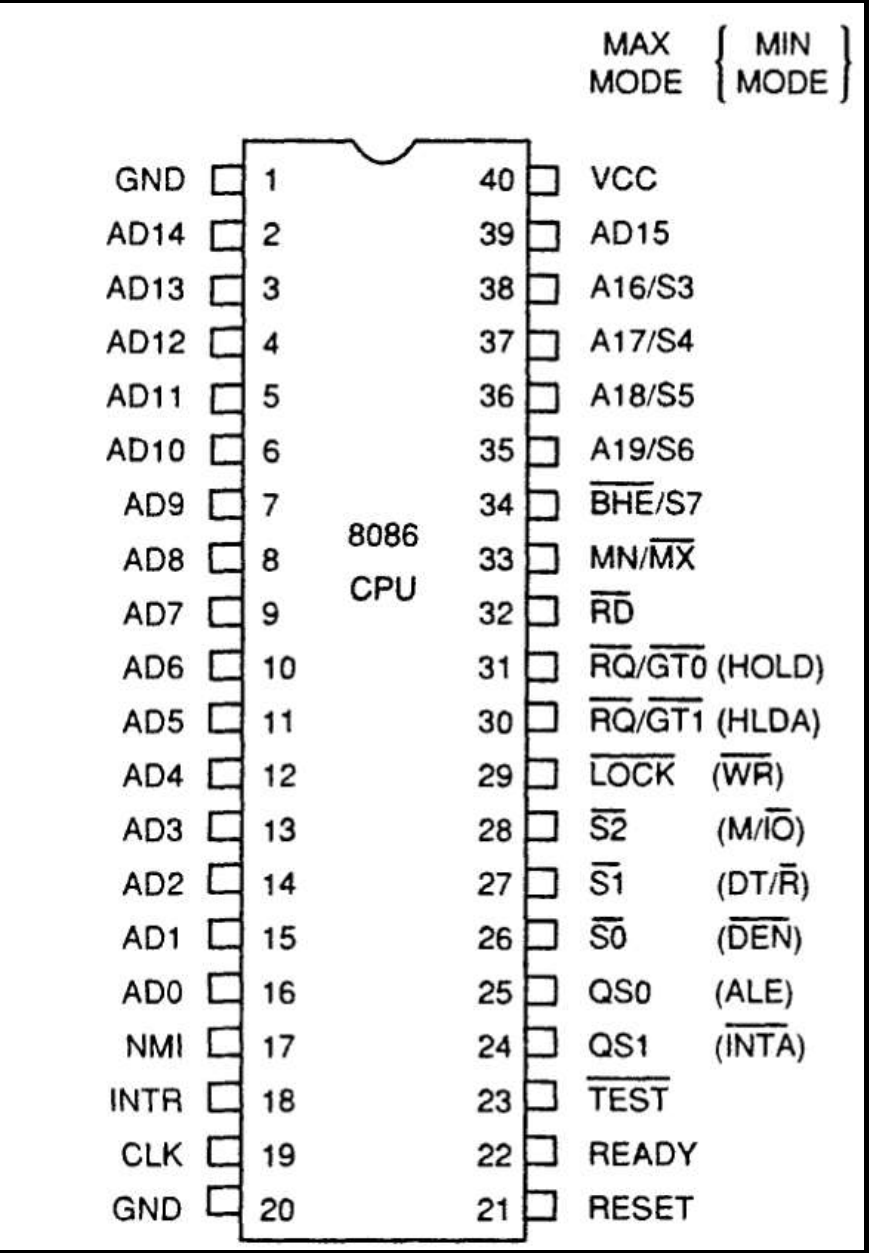
BIU registers
(20 bit adder)

ES		Extra Segment
CS		Code Segment
SS		Stack Segment
DS		Data Segment
IP		Instruction Pointer

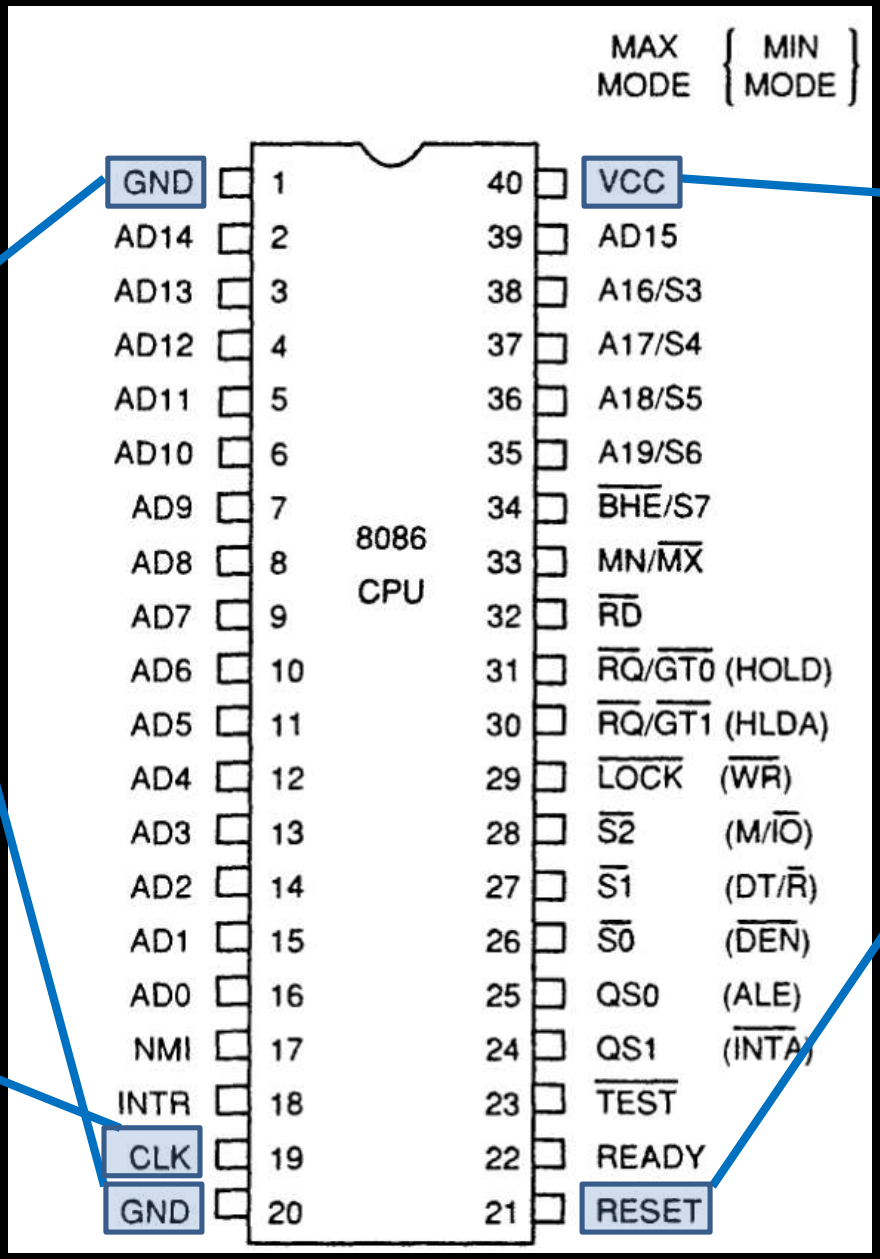
EU registers

AX	AH	AL	Accumulator
BX	BH	BL	Base Register
CX	CH	CL	Count Register
DX	DH	DL	Data Register
	SP		Stack Pointer
	BP		Base Pointer
	SI		Source Index Register
	DI		Destination Index Register
	FLAGS		

INTEL 8086 - Pin Diagram



INTEL 8086 - Pin Details



Ground

Clock

Power Supply

5V ± 10%

Reset

Registers, seg regs, flags

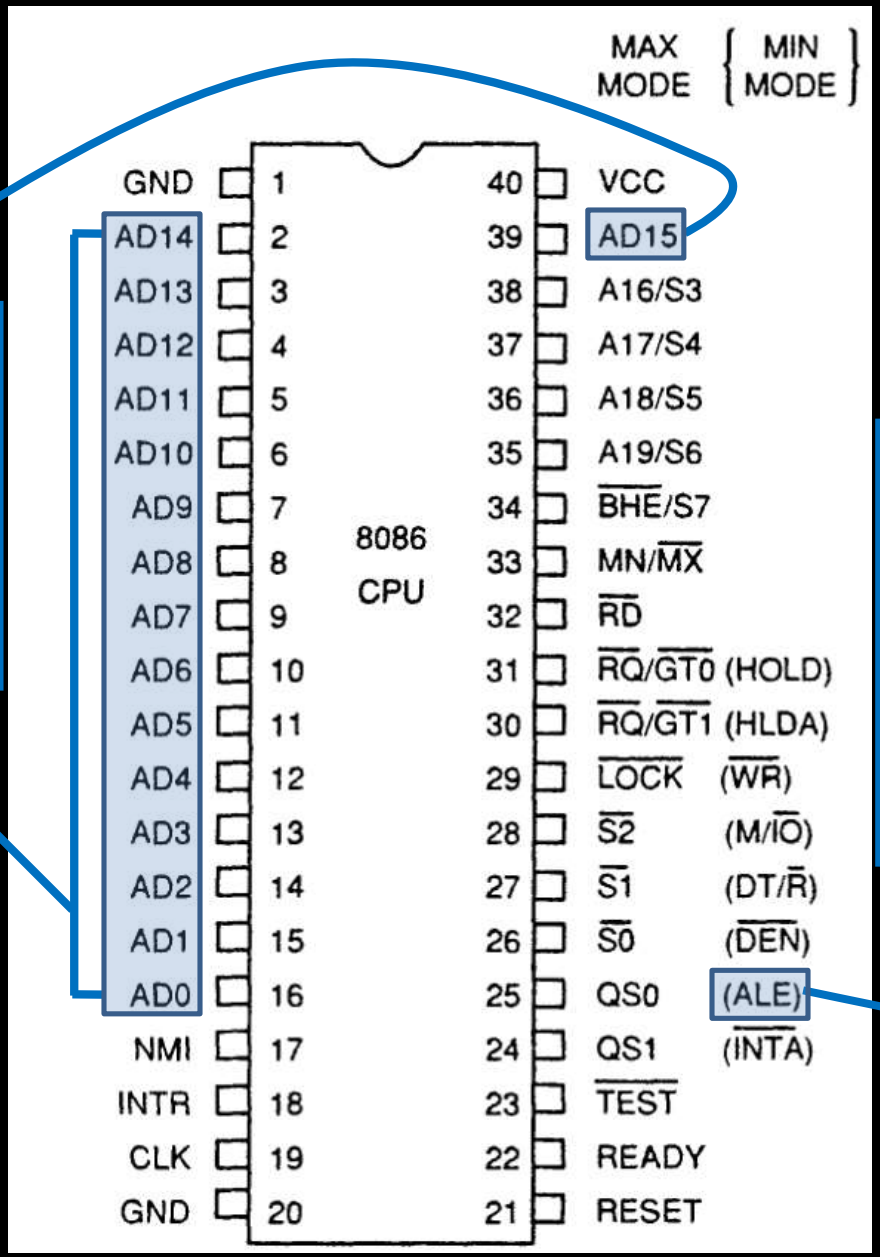
CS: FFFFH, IP: 0000H

If high for minimum 4 clks

INTEL 8086 - Pin Details

Address/Data Bus:

Contains address bits A_{15}-A_0 when ALE is 1 & data bits D_{15} – D_0 when ALE is 0.

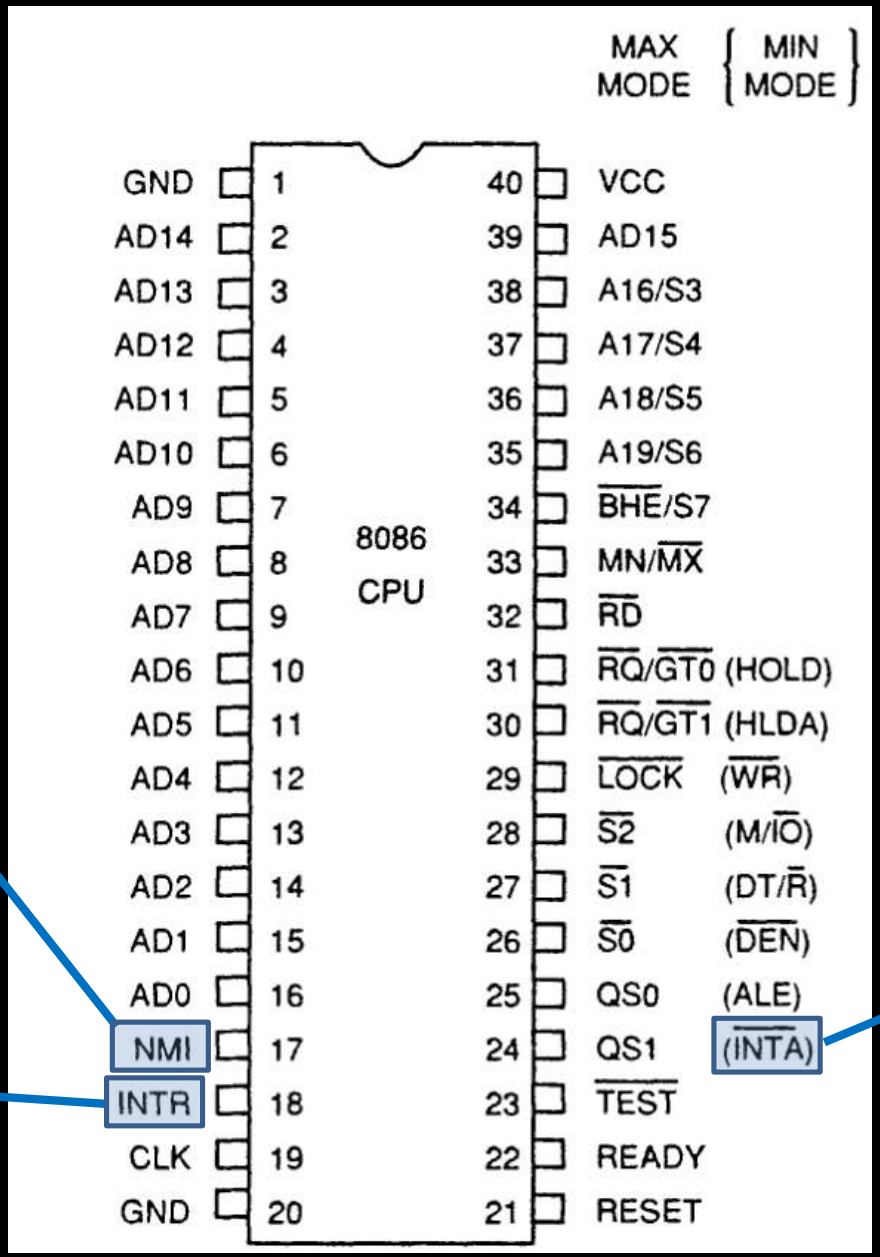


Address Latch Enable:

When high, multiplexed address/data bus contains address information.

INTEL 8086 - Pin Details

INTERRUPT

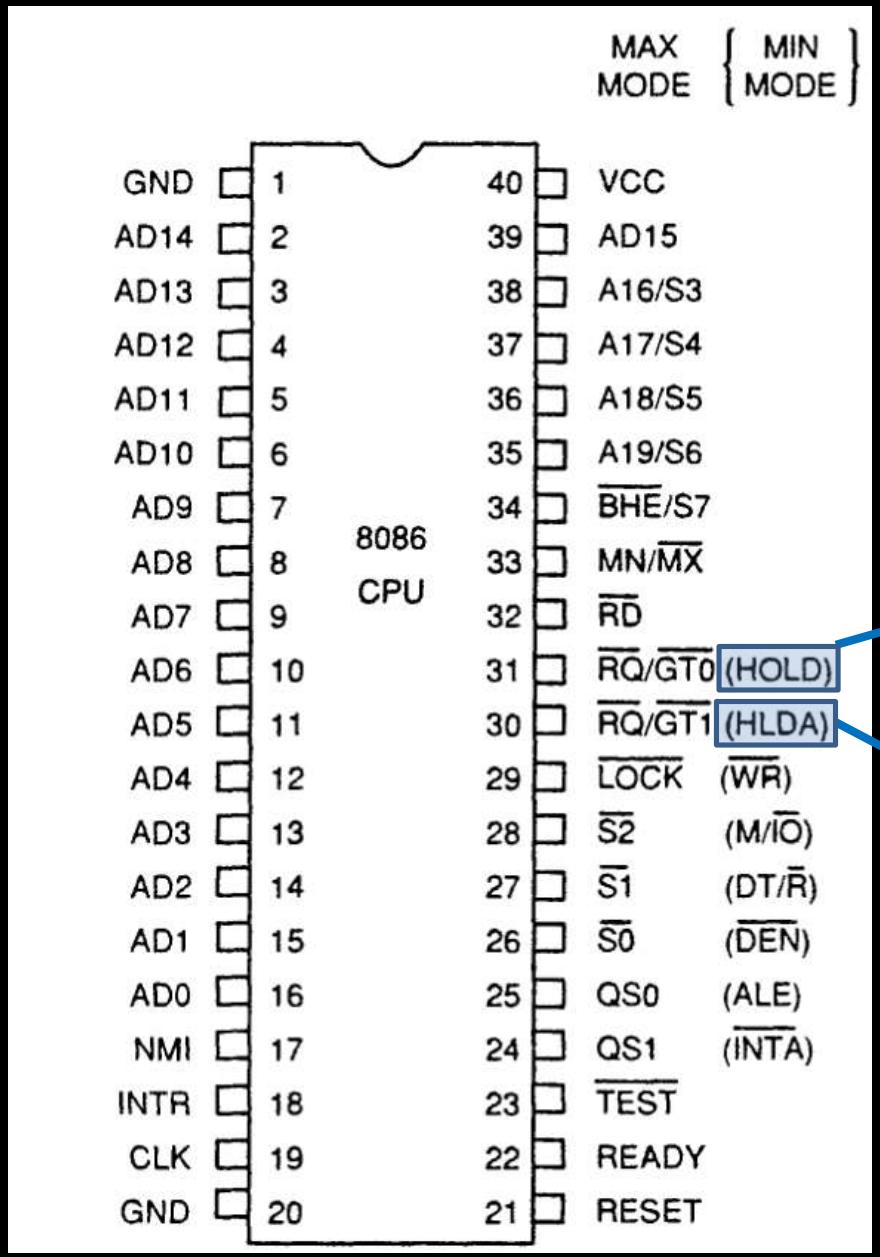


Non - maskable interrupt

Interrupt request

Interrupt acknowledge

INTEL 8086 - Pin Details



Direct Memory Access

Hold

Hold acknowledge

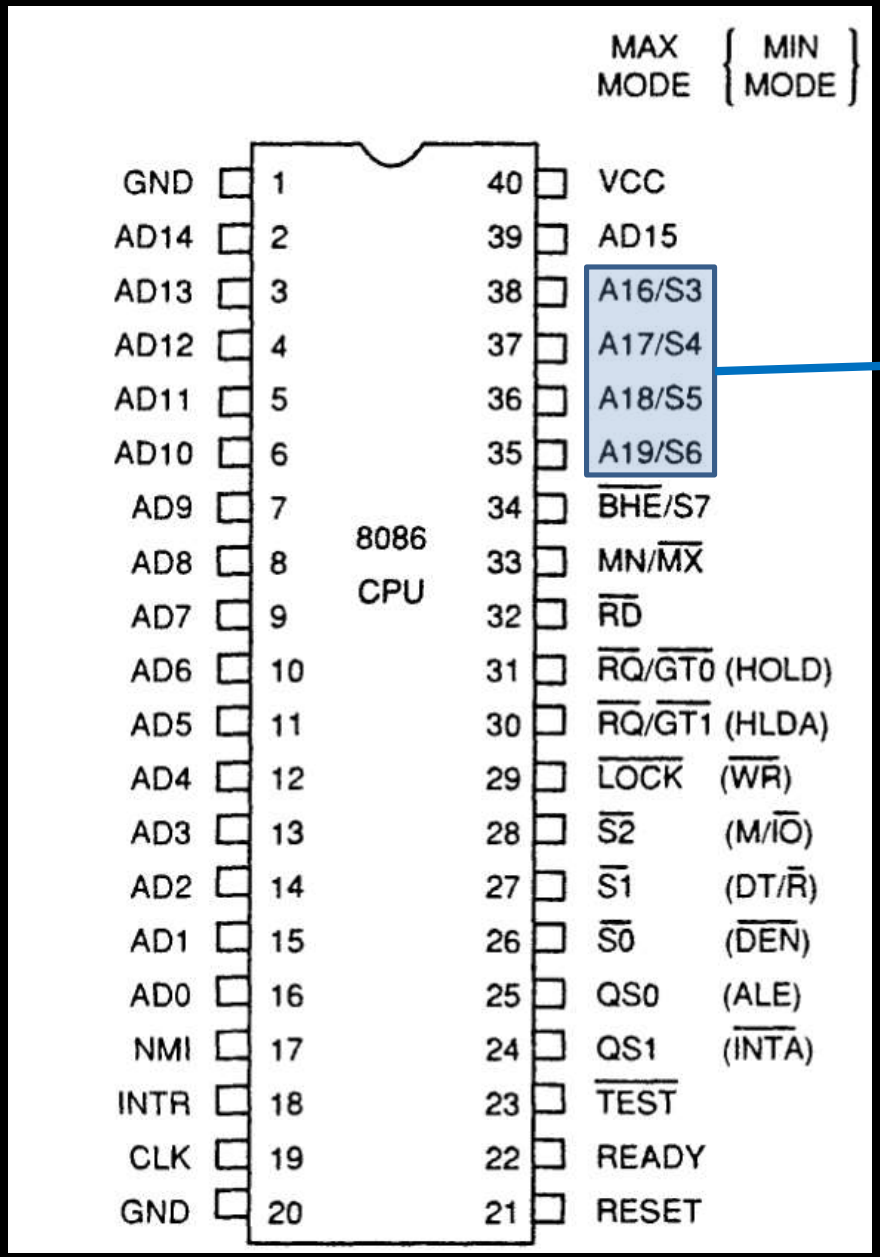
INTEL 8086 - Pin Details

S6: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	Function
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment



Address/Status Bus

Address bits A_{19} – A_{16} & Status bits S_6 – S_3

INTEL 8086 - Pin Details

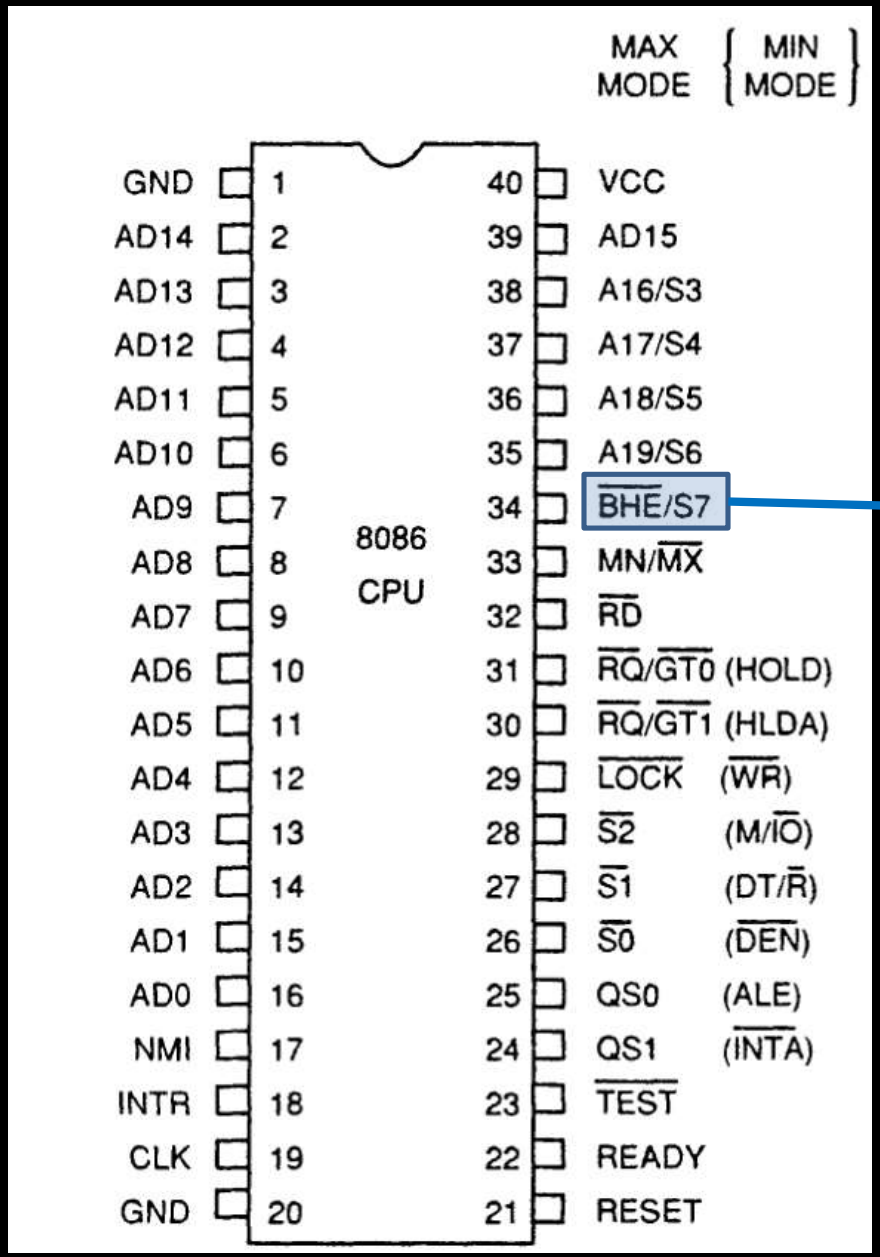
BHE#, A_0:

0,0: Whole word (16-bits)

0,1: High byte to/from odd address

1,0: Low byte to/from even address

1,1: No selection

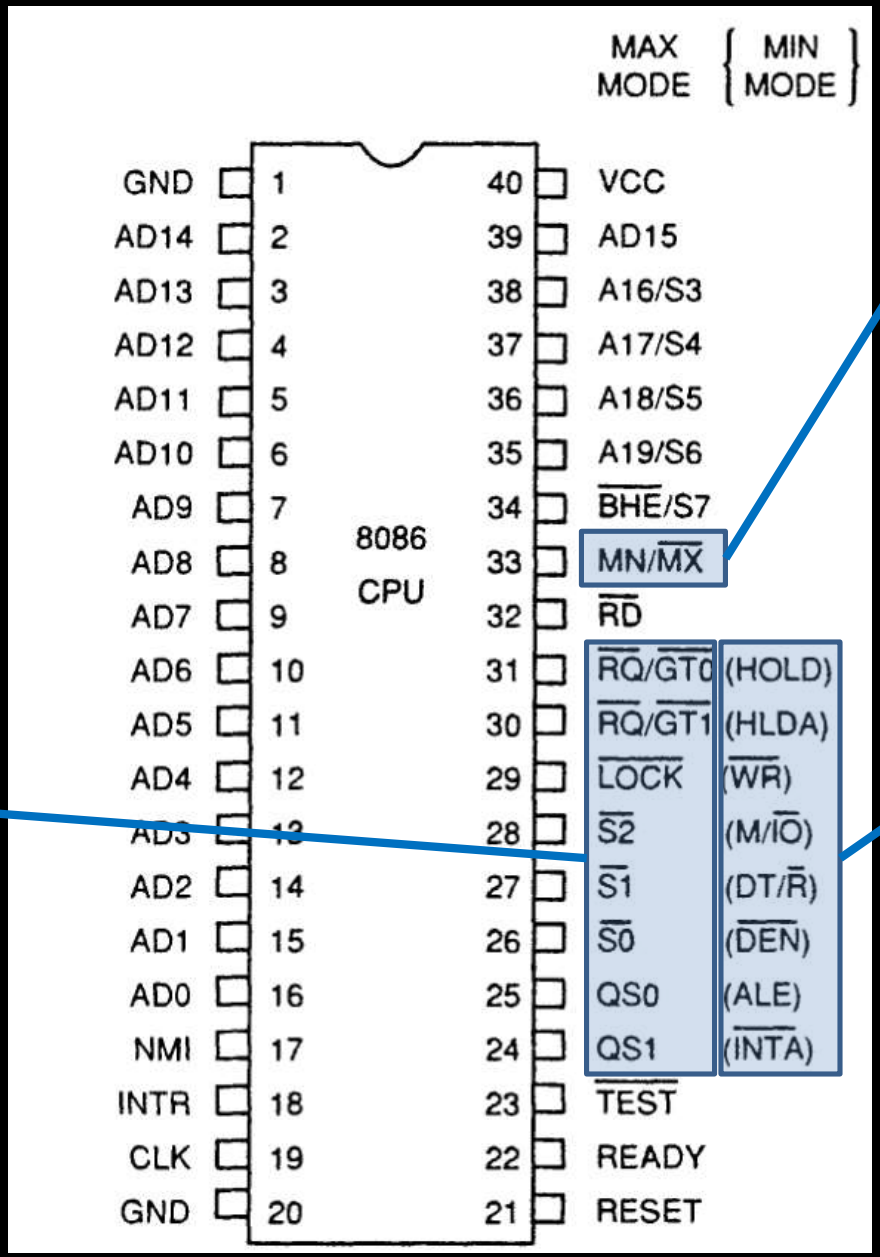


Bus High Enable/S7

Enables most significant data bits $D_{15} – D_8$ during read or write operation.

S_7: Always 1.

INTEL 8086 - Pin Details



Min/Max mode

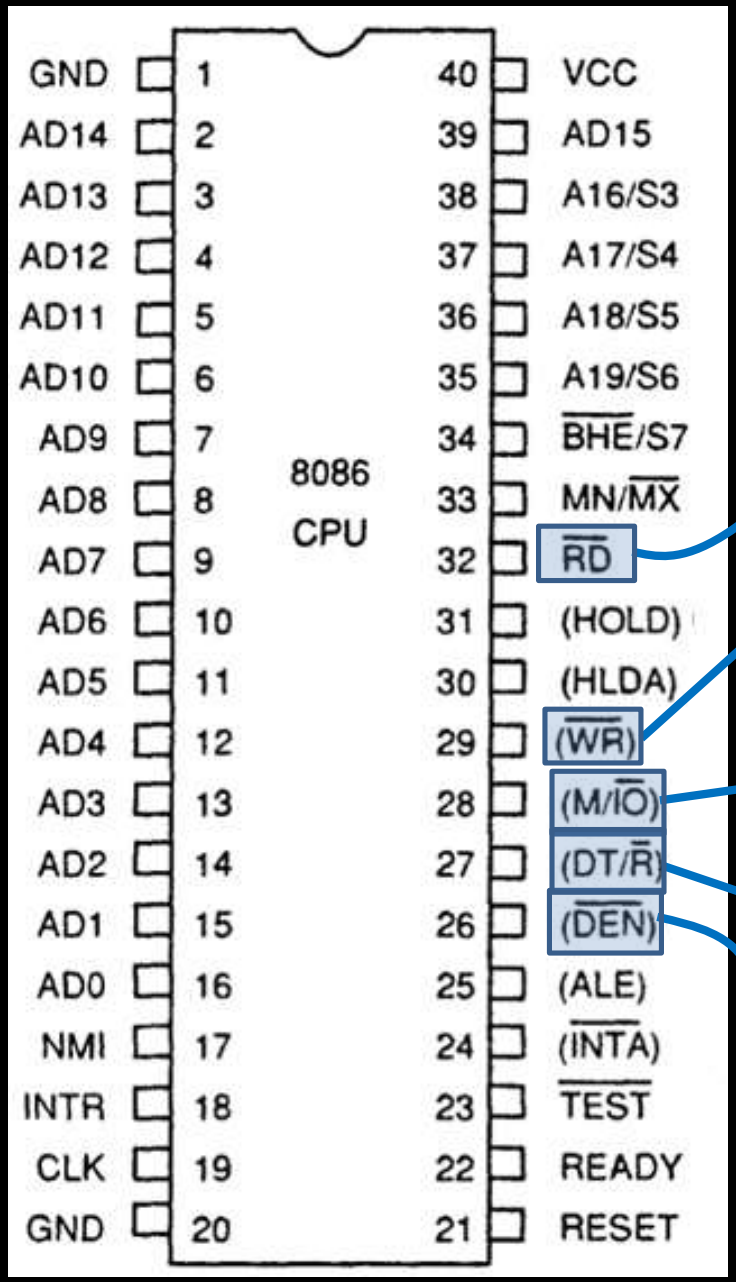
Minimum Mode: +5V

Maximum Mode: 0V

Minimum Mode Pins

Maximum Mode Pins

Minimum Mode- Pin Details



Read Signal

Write Signal

Memory or I/0

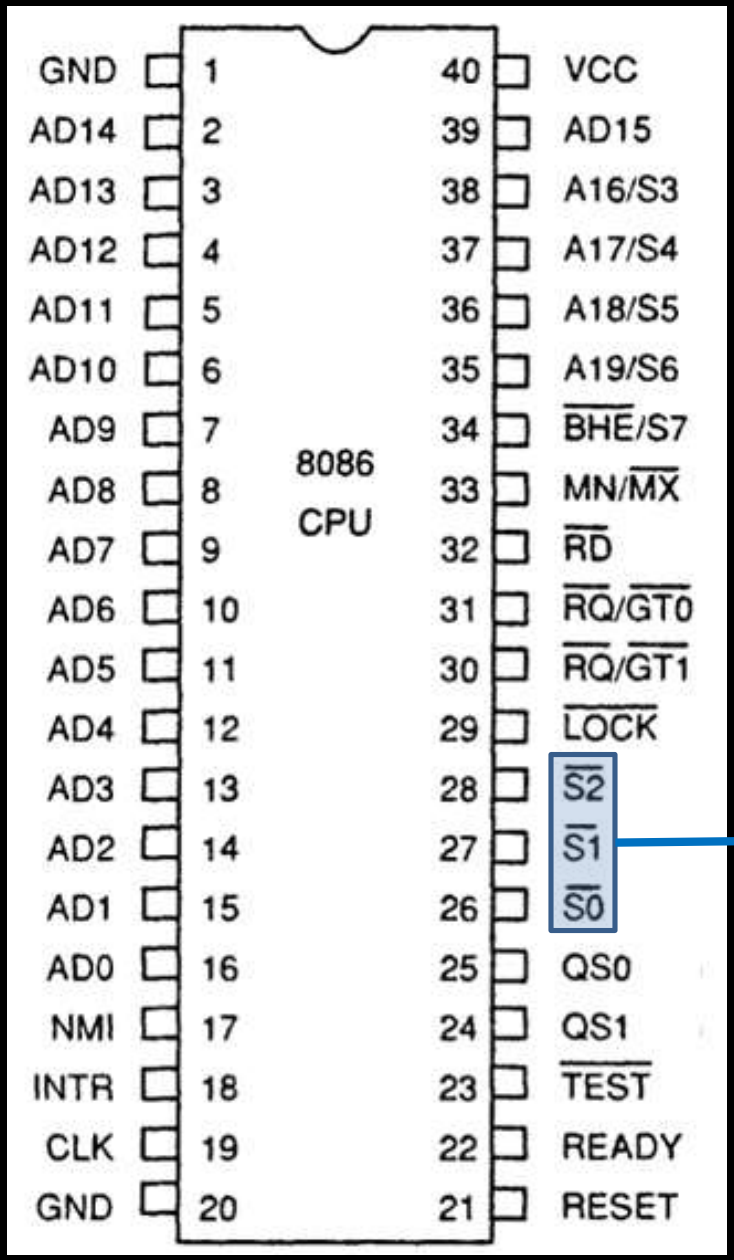
Data Transmit/Receive

Data Bus Enable

Maximum Mode - Pin Details

S2 S1 S0

000: INTA
001: read I/O port
010: write I/O port
011: halt
100: code access
101: read memory
110: write memory
111: none -passive



Status Signal

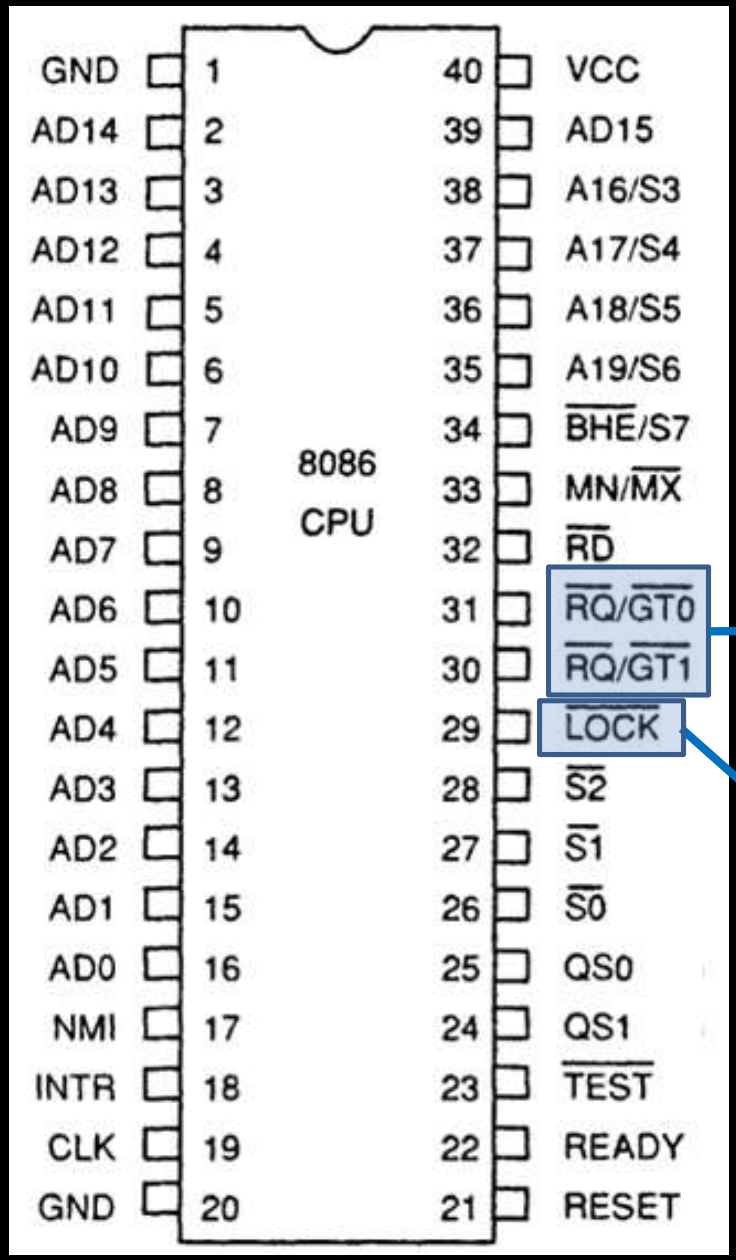
Inputs to 8288 to generate eliminated signals due to max mode.

Maximum Mode - Pin Details

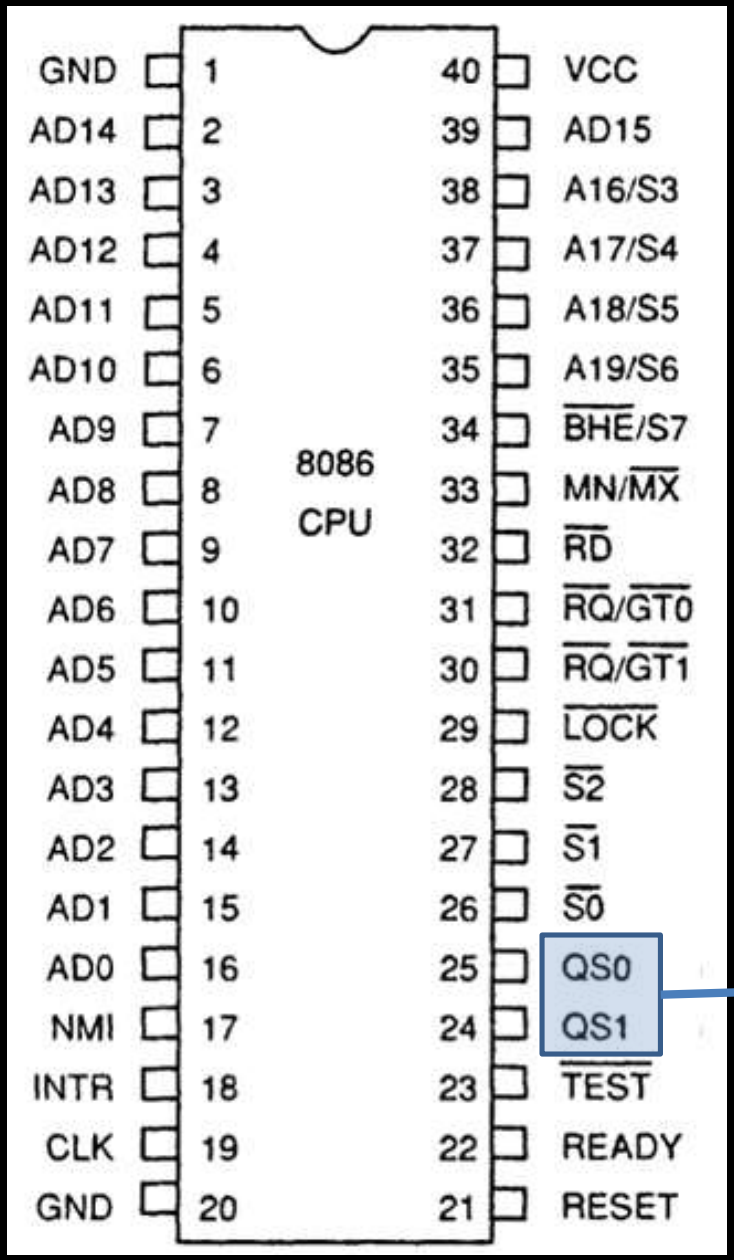
Lock Output

Used to lock peripherals off the system

Activated by using the LOCK: prefix on any instruction



Maximum Mode - Pin Details



QS1 QS0

00: Queue is idle

01: First byte of opcode

10: Queue is empty

11: Subsequent byte of opcode

Queue Status

Used by numeric coprocessor (8087)

Addressing Modes of 8086

Why study addressing modes?

Addressing modes help us to understand the types of operands and the way they are accessed while executing an instruction.

What are we going to study?

Addressing modes

- We will see the types of addressing modes present in 8086.
- We will study each addressing mode with example.

Types of addressing mode in 8086

1. Immediate addressing mode
2. Direct addressing mode
3. Register addressing mode
4. Register Indirect addressing mode
5. Indexed addressing mode
6. Register relative addressing mode
7. Base plus index addressing mode
8. Base relative plus index addressing mode

1: Immediate addressing mode

- In this type of mode, immediate data is part of instruction and appears in the form of successive byte or bytes

MOV AX,10AB$_H$

10 AB$_H$

AX

2: Direct addressing mode

- In this type of addressing mode a 16-bit memory address is directly specified in the instruction as a part of it.

MOV AX,[5000H]

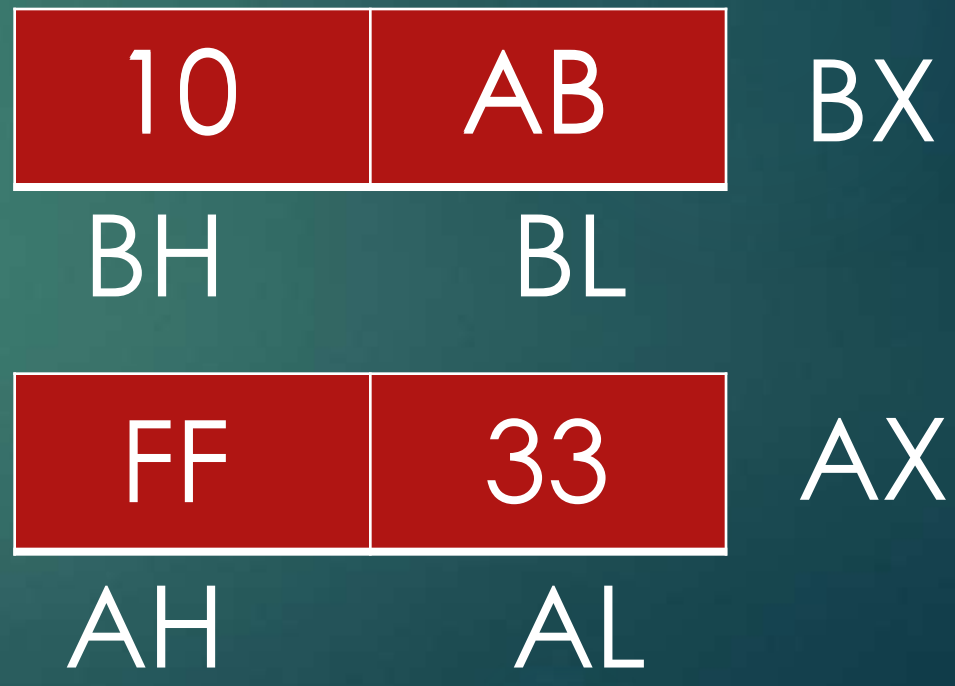
AX

3: Register addressing mode

- In this type of addressing mode, the data is stored in the register and it can be a 8-bit or 16-bit register. All the registers, except IP, may be used in this mode.

MOV AL,BLH

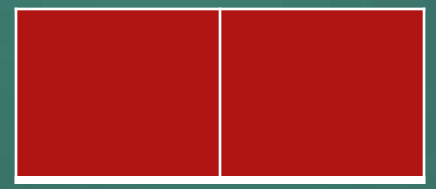
MOV AX,BXH



4: Register Indirect addressing mode

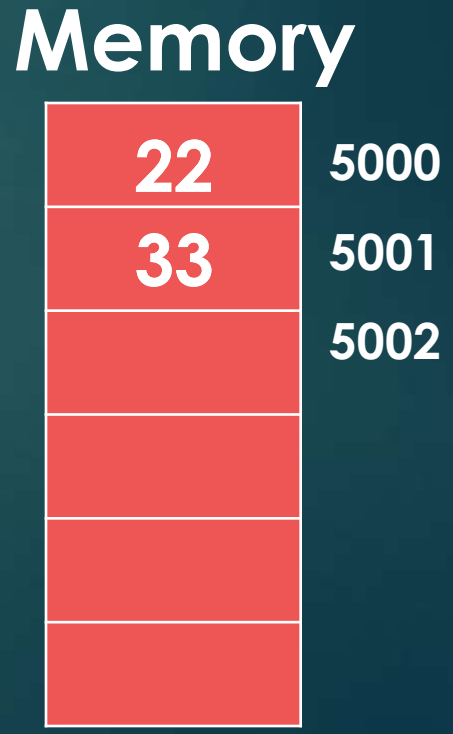
- The address of the memory location which contains data or operand is determined in a indirect way, using the offset register.

MOV AX,[BX]



AX

BX



Reflection Spot

MOV [7000H],CX

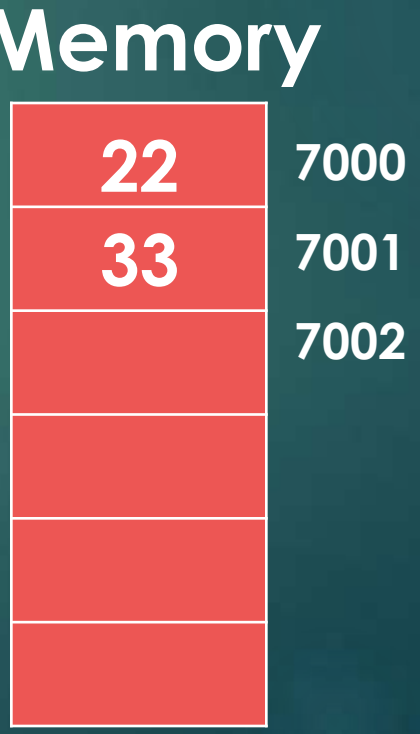
Q) Which addressing does instruction above belong, and why?

Reflection Spot

MOV [7000H],CX

Q) Which addressing does instruction above belonging and why?

Ans) Direct addressing mode



5: Indexed addressing mode

- In this addressing mode, offset of the operand is stored in one of the index registers. DS is the default segment for index register SI and DI.

MOV AX,[SI]

6: Register relative addressing mode

- In this mode, the data is available at an effective address formed by adding an 8-bit or 16-bit displacement with the content of any one of the registers BX, BP, SI and DI in the default (either DS or ES) segment.

MOV AX, 50H[BX]

AX

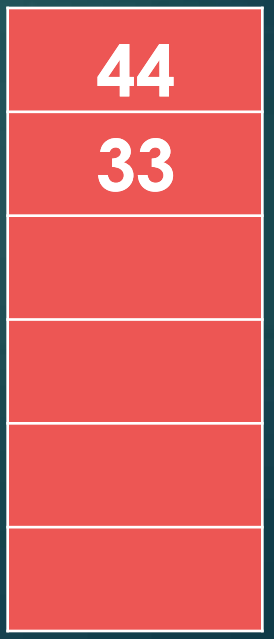
BX

+ 50H = 5050H

Offset

Final Index Address

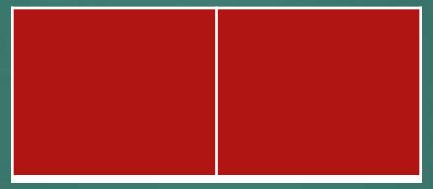
Memory



7: Base plus index addressing mode

- In this mode the effective address is formed by adding content of a base register (any one of BX or BP) to the content of an index register (SI or DI). Default segment register DS.

MOV AX, [BX] [SI]



AX

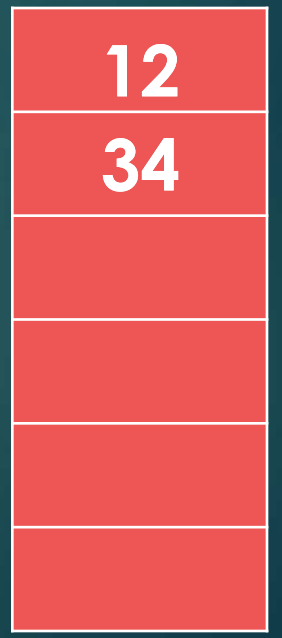
BX

+

SI

= 3000H

Final Index Address



8: Base relative plus index addressing mode

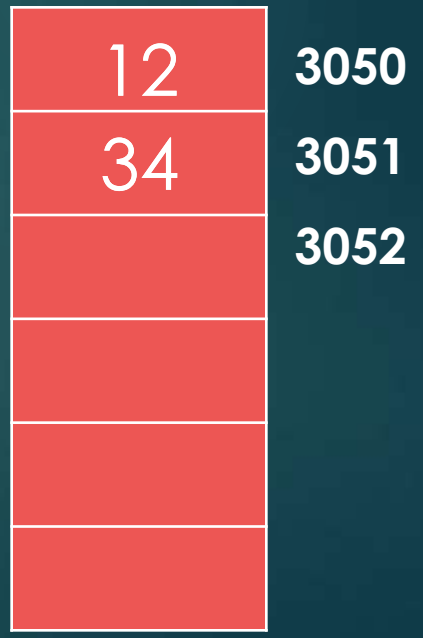
- In the effective address is formed by adding an 8 or 16-bit displacement with sum of contents of any one of the base registers (BX or BP) and any one of the index registers, in a default segment.

MOV AX,50H[BX][SI]

AX

50H + **10** **00** (BX) + **20** **00** (SI) = 3050H

Final Index Address



Summery

What we have learnt

- Different types of addressing modes present in 8086.
- Location of operands with respect to different addressing modes.