Problem 1

Model : $\frac{\text{average cycle}}{\text{word access}} = f_c \cdot \frac{\text{cache cycle}}{\text{word access}} + (1-f_c) \frac{\text{main mem. cycle}}{\text{word access}}$

a) $f_c = 99\% = 0.99$

$$\therefore \frac{\text{avg. cycle}}{\text{word access}} = 0.99 \times \frac{2 \text{ cycles}}{\text{word}} + (1-0.99)\, 100 \frac{\text{cycles}}{\text{word}}$$

$$\therefore \frac{\text{avg. cycle}}{\text{word}} = (1.98 + 1) \frac{\text{cycles}}{\text{word}}$$

$$\therefore \frac{\text{avg cycle}}{\text{word}} = 2.98 \frac{\text{cycles}}{\text{word}}$$

$$f_{WIM} = \frac{\text{floating point ops.}}{\text{memory access}} \quad ; \text{ processor} = 2 \text{ GHz} = 2 \times 10^9 \text{ cycles/sec.}$$

$$\therefore \text{Predicted Peak performance} = \frac{\text{processor speed} \times f_{WIM}}{\text{avg. cycle}}$$

$$= \frac{2 \times 10^9 \times 2}{2.98} = 1.34 \times 10^9 \text{ FLOPS}$$

$$= 1.34 \text{ giga FLOPS}$$

$f_c = 1\% = 0.01$

$$\Rightarrow \frac{\text{avg cycle}}{\text{word}} = 0.01 \times 2 + 0.99 \times 100 = 99.02 \frac{\text{cycles}}{\text{word}}$$

$$\therefore \text{Predicted Peak performance} = \frac{2 \times 10^9 \times 2}{99.02} = 0.04 \times 10^9 \text{ FLOPS}$$

$$= 40 \text{ mega FLOPS}$$

Problem 2

Sample Batch script:

```
#!/bin/sh
##SBATCH --partition=general-compute
#SBATCH --time=00:05:00
#SBATCH --nodes=1
#SBATCH --ntasks-per-node=1
#SBATCH --constraint=CPU-L5520
##SBATCH --mem=24000
# Memory per node specification is in MB. It is optional.
# The default limit is 3GB per core.
#SBATCH --job-name="hw1-8node"
#SBATCH --output=hw1-8-ibm.out
#SBATCH --mail-user=npaliwal@buffalo.edu
#SBATCH --mail-type=END
##SBATCH --requeue
#Specifies that the job will be requeued after a node failure.
#The default is that the job will not be requeued.


echo "SLURM_JOBID="$SLURM_JOBID
echo "SLURM_JOB_NODELIST"=$SLURM_JOB_NODELIST
echo "SLURM_NNODES"=$SLURM_NNODES
echo "SLURMTMPDIR="$SLURMTMPDIR

cd $SLURM_SUBMIT_DIR
echo "working directory = "$SLURM_SUBMIT_DIR


srun lstopo --whole-system topo-8nodes.pdf

echo "All Done!"
```

Output files:

8 Node

```
SLURM_JOBID=436866
SLURM_JOB_NODELIST=d07n40s01
SLURM_NNODES=1
SLURMTMPDIR=/scratch/436866
working directory = /ifs/user/npaliwal/hw1
All Done!
```

12 Node

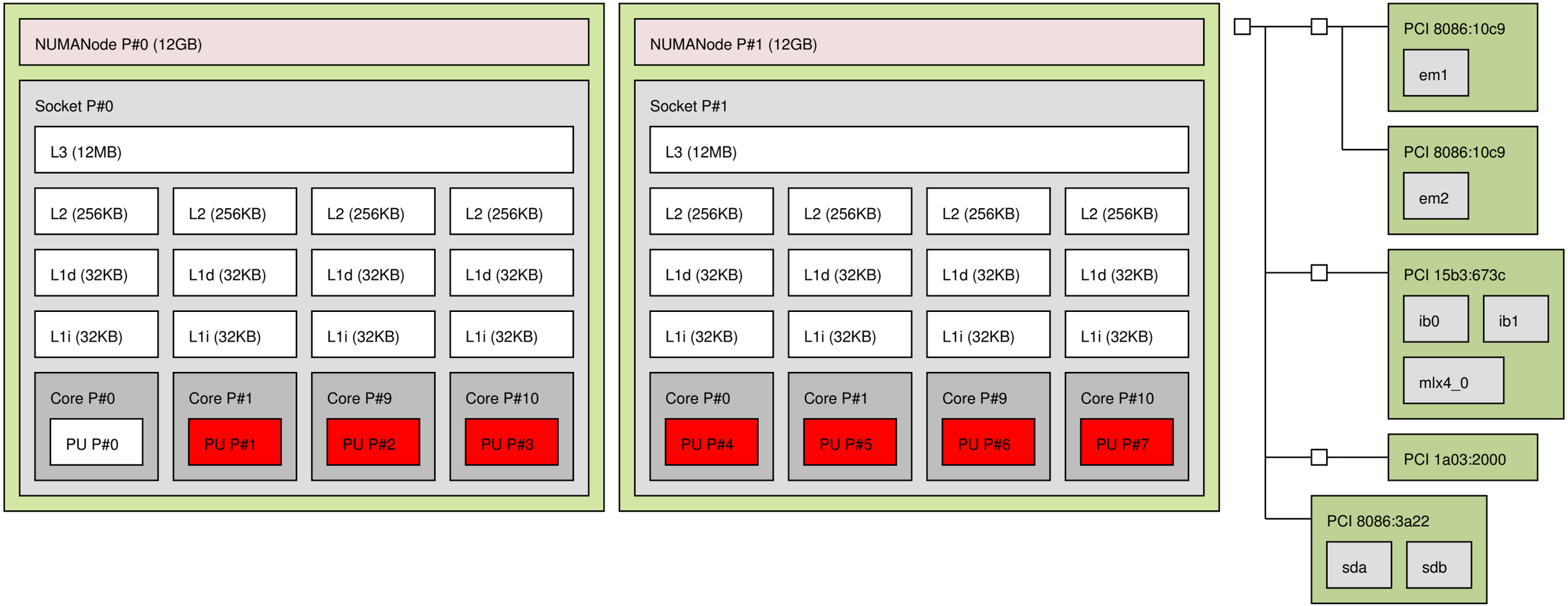
```
SLURM_JOBID=436825
SLURM_JOB_NODELIST=k08n16s02
SLURM_NNODES=1
SLURMTMPDIR=/scratch/436825
working directory = /ifs/user/npaliwal/hw1
All Done!
```

32 Node AMD

```
SLURM_JOBID=436823
SLURM_JOB_NODELIST=k07n28
SLURM_NNODES=1
SLURMTMPDIR=/scratch/436823
working directory = /ifs/user/npaliwal/hw1
All Done!
```

32 Node Intel

```
SLURM_JOBID=436824
SLURM_JOB_NODELIST=f07n13
SLURM_NNODES=1
SLURMTMPDIR=/scratch/436824
working directory = /ifs/user/npaliwal/hw1
All Done!
```



Host: d07n40s01

Indexes: physical

Date: Mon 16 Sep 2013 05:58:35 PM EDT

Machine (48GB)

NUMANode P#0 (24GB)

Socket P#0

L3 (12MB)

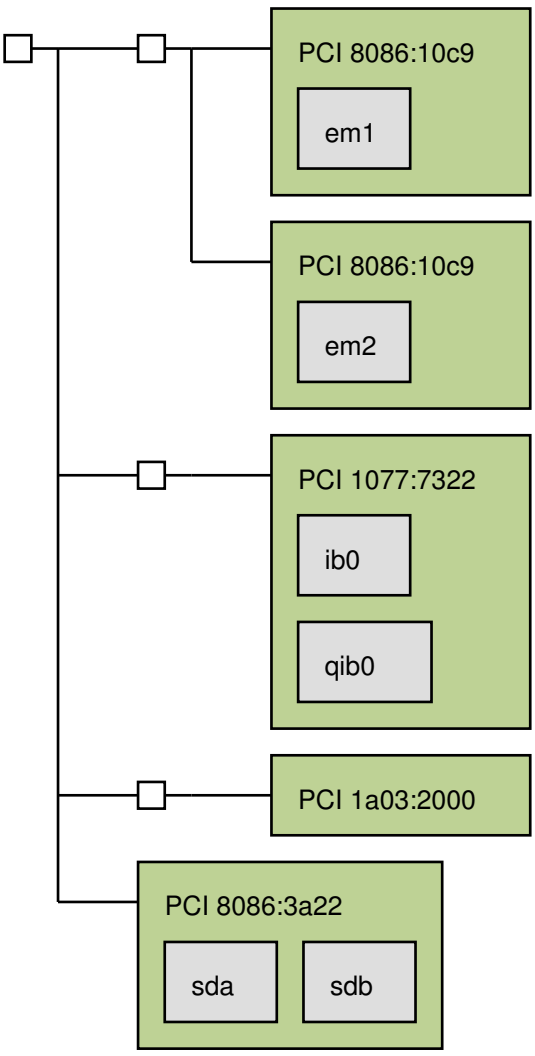
L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)
L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)
L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)
Core P#0	Core P#1	Core P#2	Core P#8	Core P#9	Core P#10
PU P#0	PU P#1	PU P#2	PU P#3	PU P#4	PU P#5

NUMANode P#1 (24GB)

Socket P#1

L3 (12MB)

L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)
L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)
L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)
Core P#0	Core P#1	Core P#2	Core P#8	Core P#9	Core P#10
PU P#6	PU P#7	PU P#8	PU P#9	PU P#10	PU P#11



Host: k08n16s02

Indexes: physical

Date: Mon 16 Sep 2013 05:58:36 PM EDT

Machine (256GB)

NUMANode P#0 (64GB)

Socket P#0

L3 (24MB)

L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)
L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)
L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)
Core P#0	Core P#1	Core P#2	Core P#8	Core P#17	Core P#18	Core P#24	Core P#25
PU P#0	PU P#4	PU P#8	PU P#12	PU P#16	PU P#20	PU P#24	PU P#28

NUMANode P#1 (64GB)

Socket P#1

L3 (24MB)

L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)
L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)
L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)
Core P#0	Core P#1	Core P#2	Core P#8	Core P#17	Core P#18	Core P#24	Core P#25
PU P#1	PU P#5	PU P#9	PU P#13	PU P#17	PU P#21	PU P#25	PU P#29

NUMANode P#2 (64GB)

Socket P#2

L3 (24MB)

L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)
L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)
L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)
Core P#0	Core P#1	Core P#2	Core P#8	Core P#17	Core P#18	Core P#24	Core P#25
PU P#2	PU P#6	PU P#10	PU P#14	PU P#18	PU P#22	PU P#26	PU P#30

NUMANode P#3 (64GB)

Socket P#3

L3 (24MB)

L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)	L2 (256KB)
L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)	L1d (32KB)
L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)
Core P#0	Core P#1	Core P#2	Core P#8	Core P#17	Core P#18	Core P#24	Core P#25
PU P#3	PU P#7	PU P#11	PU P#15	PU P#19	PU P#23	PU P#27	PU P#31

PCI 1000:0072

sda sdb sdc sdd

PCI 14e4:1639

em1

PCI 14e4:1639

em2

PCI 102b:0532

PCI 8086:3a20

sr0

PCI 1077:7322

ib0

qib0

Host: f07n13

Indexes: physical

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Machine (256GB)

Socket P#0 (64GB)

NUMANode P#0 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#0 | Core P#1 — PU P#1 | Core P#2 — PU P#2 | Core P#3 — PU P#3

PCI 1077:7322
- ib0
- qib0

PCI 8086:10c9
- em1

PCI 8086:10c9
- em2

PCI 1002:4390
- sda
- sdb
- sdc
- sdd

PCI 1002:439c

PCI 1a03:2000

NUMANode P#1 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#4 | Core P#1 — PU P#5 | Core P#2 — PU P#6 | Core P#3 — PU P#7

Socket P#1 (64GB)

NUMANode P#2 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#8 | Core P#1 — PU P#9 | Core P#2 — PU P#10 | Core P#3 — PU P#11

NUMANode P#3 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#12 | Core P#1 — PU P#13 | Core P#2 — PU P#14 | Core P#3 — PU P#15

Socket P#2 (64GB)

NUMANode P#4 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#16 | Core P#1 — PU P#17 | Core P#2 — PU P#18 | Core P#3 — PU P#19

NUMANode P#5 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#20 | Core P#1 — PU P#21 | Core P#2 — PU P#22 | Core P#3 — PU P#23

Socket P#3 (64GB)

NUMANode P#6 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#24 | Core P#1 — PU P#25 | Core P#2 — PU P#26 | Core P#3 — PU P#27

NUMANode P#7 (32GB)

L3 (5118KB)

L2 (512KB) | L2 (512KB) | L2 (512KB) | L2 (512KB)

L1d (64KB) | L1d (64KB) | L1d (64KB) | L1d (64KB)

L1i (64KB) | L1i (64KB) | L1i (64KB) | L1i (64KB)

Core P#0 — PU P#28 | Core P#1 — PU P#29 | Core P#2 — PU P#30 | Core P#3 — PU P#31

Host: k07n28

Indexes: physical

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2. (b)

Since all the nodes are represented as NUMA (non-uniform memory access) nodes, all the nodes have non-uniform shared memory

2. (c)

All the nodes have 2 L1 (L1i and L1d) cache partitions, which might be the most likely source for accessing memory