ASSIGNMENT 1
HPC1 Fall 2014

Due Date: ***Wednesday, September 17***
(please submit your report electronically to the instructor via email in one file, PDF preferred, named *hw1-yourUBITname.pdf*)

Problem 1: Consider a simplified model for a two-level memory system (say cache and main memory),

$$\frac{\text{average cycles}}{\text{word access}} = f_c \times \frac{\text{cache cycles}}{\text{word access}} + (1 - f_c) \times \frac{\text{main memory cycles}}{\text{word access}},$$

where f_c is the fraction of cache hits out of all of the memory accesses. This simple model can be used in conjunction with the "machine balance," ρ_{WM}, of the ratio of floating point operations to memory (in words, typically 8 Bytes) accesses, to predict performance (in Flop/s). Given a 2GHz processor (2×10^9 cycles/s), $\rho_{WM} = 2$, 2 cycles/word for cache and 100 cycles/word for main memory, what is the predicted performance for f_c of 99% and 1%?

Problem 2: Examine the hardware topology in the cluster at CCR. You can do this by using the **lstopo** command which is part of the OpenMPI **hwloc** project. Have a look at the man page ("**man lstopo**") and the **hwloc** project documentation to understand the details of the output from **lstopo** and what options you may need to use in combination with your slurm requests.

a) Run **lstopo** on the 8-core, 12-core, and both `INTEL` and `AMD` flavors of the 32-core nodes. Request the appropriate nodes through the batch queuing system (slurm). Record your slurm job number and graphical output from **lstopo** (note that you should be able to generate pdf and other graphical formats directly from lstopo).

b) Which node(s) have uniform shared memory, and which use non-uniform shared memory?

c) For each node type, identify the most likely sources for contention in terms of accessing memory from the processing cores.