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| --- | --- | --- | --- |
| SRAM -> low power / 6 transistor per bit  DRAM -> rewritten / refreshed. one transistor per bit  upper half **R**ow **A**ccess **S**trobe / one row at a time  lower half **C**ol **A**ccess **S**trobe / column  RAS related to latency CAS to BW.  DRAM periodically refreshed. | Three C miss category:  Compulsory  Capacity  Conflict - if the block placement strategy is not fully associative.  IF ID EX MEM WB | L1 4x48KB D 4x32KB I  L2 4x 1.25MB  L3 12MB  Fully associative: one set only  Direct-mapped: one block per set.  n-way set : n block per set.  Write through and write back | DEVOPS:  deploy->Jenkin, Splunk->log, Monitor->Nagios  code->build->test->integrate->deploy->operate->monitor->plan->code  CD  plan code build test  CI= add release success deploy failure bug\_file |
| TLP / ILP (thread /instruction level parallelism) |  | Cache Prefetch and register prefetch  HW prefetch and compiler controlled prefetch. |  |
| Virtual sensor policy/Active policy/Adaptive performance /critical policy  Throttling participant / fan control  Thermal design power |  |  |  |
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