Atin Jain

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Profile

Passionate Aerospace Electronics Engineer with more than 5 years of experience in designing high speed, mixed signal systems. Keen to advance my career with and contribute to an organization where I can learn, challenge and upgrade myself and share my knowledge and experience.

Professional Experience

Senior Electronics Design Engineer, Honeywell Aerospace, United Kingdom	May '18 – Till now
Senior Engineer, Sling Media (subsidiary of Dish Network, USA), Bengaluru, India	Sep '17 – Apr '18
Senior Engineer, VVDN Technologies, Gurgaon, India	Feb '16 – Sep '17
Senior Design Engineer, Bitmapper Integration Technologies, Pune, India	Jul '13 – Jan '16

- Experience in analysis, design, simulations and validation of circuits.
- Working with multi-disciplinary team and cross team coordination with mechanical and software/firmware teams to achieve design objectives.
- Design capture in schematic and layout. Design analysis and review – power delivery, functional, thermal and basic signal integrity.
- Good knowledge of high speed board interfaces and power layout guidelines including component placement, delay/length matching, return paths and timing.
- Experience in using industry protocols and technologies such as PoE, Ethernet, microprocessor, microcontroller, FPGAs, SRAMs, Flash, DDR3, SRIO, USB, UART, SPI, I2C, BT/BLE.

Skillset

System design	• Component Selection • Schematic Entry • Analysis & review targeted at Signal Integrity and timing • System bring up, testing, validation and debugging • Technical documentation
EDA and other software tools	• Schematic entry : Cadence Capture • Board layout review : Cadence Allegro Suite • SI and PDN analysis : Cadence Allegro Suite • Electrical simulation : PSpice, LTSpice, TINA
Test equipment and apparatus	• Oscilloscopes, Multi meter (DMM) • Multi-channel bench Power Supply, DAQs and loggers

Managerial skills	• Product / project management, team management • Resource planning, costing and allocation • Multinational and multi time zone client, fabrication and assembly house interaction and management • Fluent in global English, TOEFL score 106
Programming skills	• Introductory VHDL, C, Assembly Language (ARM)

Projects

Project name — RCA of a current leakage issue

Description

A camera adaptor ecosystem which can transmit video up to 4 videos at 1080p and 60fps over Wi-Fi with very low current showed higher currents in some units.

Complexity

- Difficult to pin-point the source of leakage
- Multiple angles of reasoning and possible sources in the same component
- Designing test cases to pinpoint the reason of the component failure.

Contribution

- Test case design to cover all the possibilities
- Rigorous testing
- Data collection, interpretation and analysis
- This led to a policy change is usage of components.

Project name — Smart cluster for Motorcycles in Indian Market

Description

Based on Qualcomm's APQ8009 (Snapdragon 212) this device is under testing and development. This device will enable a rider to be safer and still remain connected while riding. This device also features anti-theft and alerts along with tracking and navigation based on GPS. It will have a display which will replace the traditional needle dials and segment display to be more informative

Complexity

- Inexpensive and affordable solution for every segment of motorcycles
- MIPI Display interface, booting time for Android
- Protection from automotive noise and harsh environment
- Integration of numerous sensors and algorithm development for processing data collected thereof

Contribution

- Hardware design lead, lead team of 5 engineers.
- Design documents, component selection and BOM optimization
- Review of schematics, layout
- Successful in first prototype

Project name — Human System Interaction Board

Description

NXP's i.MX6 microprocessor based board for modernization of legacy fueling pumps with multiple displays, audio output. The primary requirement was to provide the user with easy and intuitive experience to ease fueling of vehicles. This device requires UL certification for Class I Division II also. This single design supports all Solo, Dual and Quad i.MX6 processors with up to 4GB DDR3 (16bit, 32bit and 64bit) memory configuration

Complexity

- Multilayer dense board, small form factor
- Gigabit Ethernet, LVDS Display Interface
- Power Over Ethernet (IEEE 802.3at with 802.3af compatibility)
- 10 Watt Audio Output, CAN, RS232, RS422, RS485, USB hub

Contribution

- Design documents, component selection and BOM optimization
- Analysis and design of 1G Ethernet, POE, audio output, LVDS interface sections
- Design to undergo and pass UL certification for Class 1 Div 2
- Schematic, layout guidelines and review

Project name — Analog Data and Video Capture Board

Description

This design was for a defense establishment in India. This was designed to capture analog sensors and video data from thermal imager through high speed and video ADCs respectively and process it as digital data inside FPGA.

Complexity

- For use in armored vehicle, therefore critical mechanical design
- Isolated power domains, critical power design, redundant supplies
- Two ADCs with 4 channel each with sampling rate of 40Msps
- Interfacing with thermal imager, analog S and VGA video output
- Virtex 4 FPGA, Video ADCs and DACs

Contribution

- Client meetings, understanding requirements and translating them to technically achievable goals
- Power generation and protection circuit design
- Component selection for wide temperature range and environmental tests for high vibrations and shock testing
- Design and layout review for MIL EMI/EMC standards certification
- Bring-up, validation and demonstration and acceptance testing at client site

Project name — Video processing and interface board for thermal imager

Description

Xilinx's Virtex 4 and i.MX6 quad core based image processing board, designed to act as a frame grabber application which can also process the images/videos captured using the OpenCV and OpenGL on Linux based distribution

Complexity	• Set of three foldable boards connected through a flex-PCB • Small sized dense boards with more than 16 BGA components • 32bit synchronous bus between processor and FPGA • 3 video input (2 analog, 1 HDMI), 4 video outputs (1VGA, 1HDMI, 1 analog, 1DVI), Gigabit Ethernet • Very wide operating temperature range -40°C to 125°C
Contribution	• Hardware design documents, component selection and BOM optimization • Schematic design, layout guidelines and review • Board bring-up and validation

Project name Video Processing and Storage Board

Description	Xilinx's Virtex 4, Kintex 7-325T, Kintex 7-70T and ADSP-BF561 dual core based image processing board, capable of H.264 encoding, frame by frame storage and transmission of compressed and uncompressed video over Ethernet and SRIOs
Complexity	• Set of two stacked (V4, K7-325T & ADSP-BF561) and one stand-alone (K7-70T) boards • Multilayer ultra-dense, high speed, mixed signal board with BB VIAs • Gigabit Ethernet, Serial Rocket IOs (3.125Gbps link) • Critical reset and power design. Current rating of 20A • SRAMs, DDR3, SPI NOR Flash, onboard NAND Flash for video storage • Very wide operating temperature range -40°C to 125°C
Contribution	• Customer interaction, requirement gathering, design documentation, component selection • Complete schematic design to address concerns of SI and simulations for PDN • Oversaw complete layout, drafted guidelines and reviewed the layout • Bring-up, interface validation & demonstration at customer site

Project name Multi-sensor Image Registration and Fusion

Description	This design consisted of three boards namely HMI, Fusion and Registration which when mounted on a motherboard could take input from a total of 5 image sensors/cameras, perform registration and fusion along with compressing the videos and images and storing them onboard and transmitting them.
Complexity	• Design for a defense laboratory, aluminum mechanical enclosure • Set of three designs connected on a motherboard. Total of 6 FPGAs, 2 DSPs and 1 multimedia processor • Mixed signal design, consisting of analog video inputs digital processing and finally analog output

- Gigabit Ethernet, Serial Rocket IOs (3.125Gbps link). SRAMs, DDR3, SPI NOR Flash, onboard NAND Flash for video storage.
- Critical reset and power design.

Contribution

- Requirement gathering and translation into technical requirements, component selection
- Schematic design, oversaw complete layout, drafted guidelines and reviewed the layout
- Bring-up, interface testing and validation

Education

Bachelor of Technology (Information and Communication Technology) 2009 – 2013

Dhirubhai Ambani Institute of Information and Communication Technology, India

Achievements

- IEEE Travel and Attendance grant for Sensors – 2012, 2014, 2015, 2017 and 2018
- IEEE Travel and Attendance grant for World Forum on IoT – 2015
- IEEE travel and Attendance grant for IUS – 2015
- IEEE Outstanding Service Award – 2012
- IEEE Gujarat Section Best Student Volunteer Award – 2012