Flip Flop

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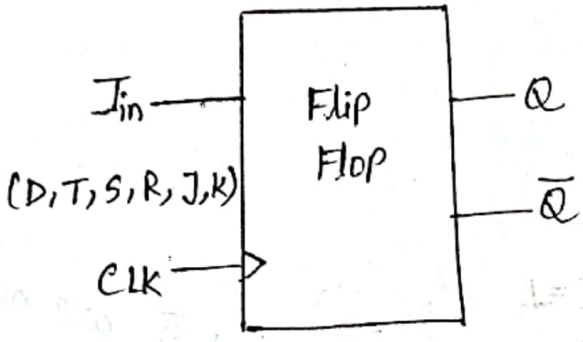
What is flip flop?

⇒ A flip flop is a sequential ~~circuit~~ digital electronic circuit having two stable states that can be used to store one bit of binary data.

Truth table, characteristics table and Excitation table of Flip Flop:-

* D FF → Jin এর পরিবর্তে D
  T FF → Jin এর পরিবর্তে T
  SR FF → Jin এর পরিবর্তে S and R
  JK FF → Jin এর পরিবর্তে J and K



Truth table:-

Inputs respect to outputs / Next state

CLK	Jin	Q	$\bar{Q}$

CLK	Jin	Q_{n+1}

Characteristics Table:-

Current state (Q_n) and Inputs (J_n) respect to next state (output) (Q_{n+1})

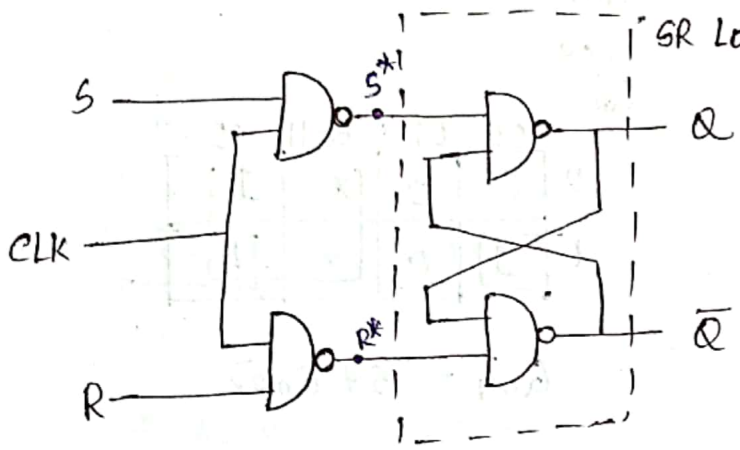
Q_n	Jin	Q_{n+1}

Excitation Table:

Current state (Q_n) and Next state (Q_{n+1}) w.r.to inputs (J_{in})

Q_n	Q_{n+1}	Jin

SR flip-flop:- SR flip flop is a gated set reset flip-flop. The S and R inputs control the state of the flip flop when the clock pulse goes from Low to high.



S*	R*	Q	$\bar{Q}$
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	Memory	

Here, $S^* = \overline{S.CLK} = \bar{S} + \overline{CLK}$

$R^* = \overline{R.CLK} = \bar{R} + \overline{CLK}$

when, CLK = 1

$S^* = \bar{S}$ and $R^* = \bar{R}$

For nand gate input = 0 then output = 1

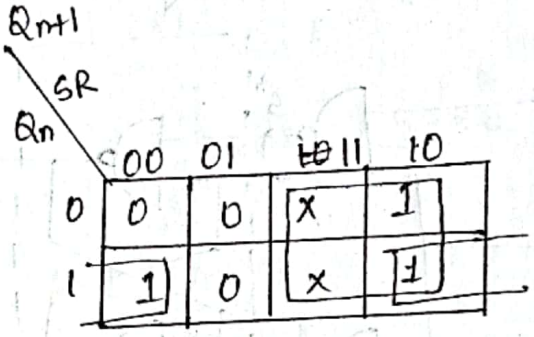
Truth Table:

CLK	S	R	Q	$\bar{Q}$
0	x	x	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	

CLK	S	R	Qn+1
0	x	x	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	Invalid

Characteristic Table:

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Invalid
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Invalid

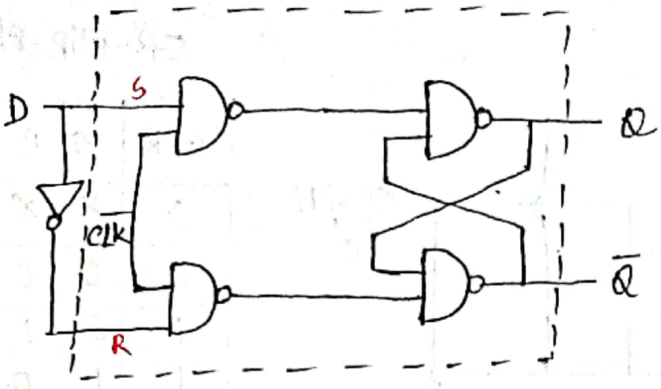


$Q_{n+1} = S + Q_n \cdot \overline{R}$

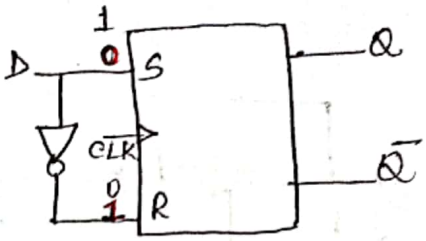
Excitation Table:

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip Flop (Data flip-flop)



SR Flip Flop



As per data flip-flop Input will get transferred to output in next state.

Truth table:

CLK	S	R	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid

CLK	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

Characteristic Table:

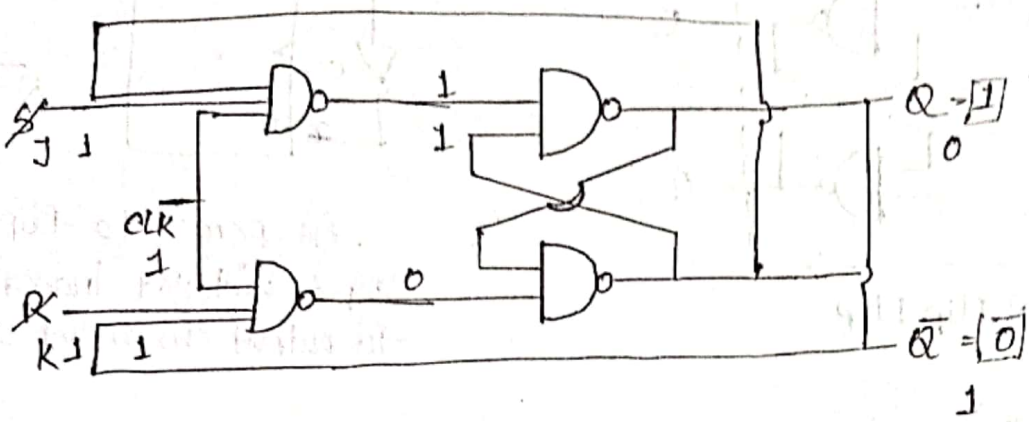
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$Q_{n+1} = D$

Excitation table:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Jk flip flop:



S-R flip-flop truth table

CLK	S	R	Q Q̄
0	x	x	memory
1	0	0	memory
1	0	1	0 1
1	1	0	1 0
1	1	1	Invalid

J-K flip flop truth table:

CLK	J	K	Q Q̄
0	x	x	Memory
1	0	0	Memory
1	0	1	0 1
1	1	0	1 0
1	1	1	Memory

Truth table

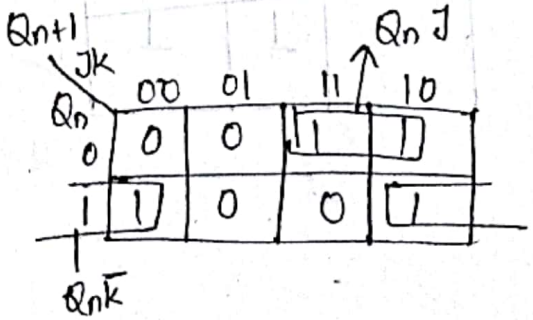
CLK	J	K	Qn+1
0	x	x	Qn
1	0	0	Qn
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

Q = 1 and Q̄ = 0

CLK = 1, J = 1, K = 1 ; Q = 0 and Q̄ = 1

Jk characteristic table

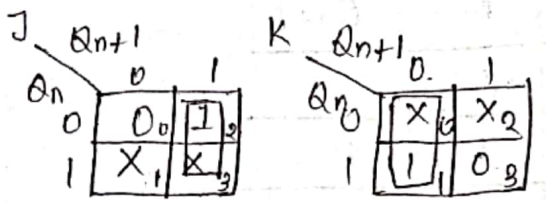
	Qn	J	K	Qn+1
0	0	0	0	0
2	0	0	1	0
4	0	1	0	1
6	0	1	1	1
1	1	0	0	1
3	1	0	1	0
5	1	1	0	1
7	1	1	1	0



$Q_{n+1} = \bar{Q}_n J + Q_n \bar{K}$

Excitation table

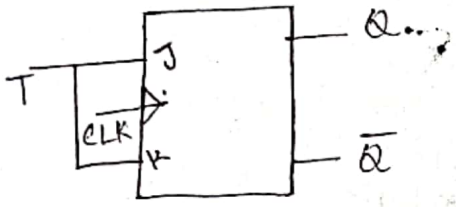
Q_n	Q_{n+1}	J	k
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

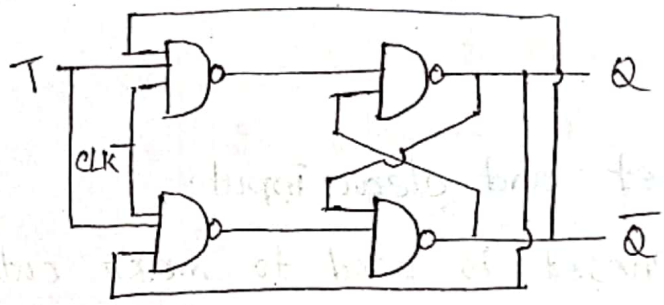


$J = Q_{n+1}$ $K = \overline{Q_{n+1}}$

T Flip Flop (Toggle flip flop)

Output will toggle (change) with respect to input along with clock signal.





Truth table of Jk Flip Flop

CLK	J	k	Q $\overline{Q}$
0	X	X	Memory
1	0	0	Memory
1	0	1	0 1
1	1	0	1 0
1	1	1	$\overline{\text{memory}}$

Truth table of D Flip Flop

CLK	T	Q $\overline{Q}$
0	X	Memory
1	0	Memory
1	1	$\overline{\text{Memory}}$

CLK	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	$\overline{Q_n}$

Characteristics table:

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$Q_{n+1} = \bar{Q}_n T + Q_n \bar{T}$

$= Q_n \oplus T$

Excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

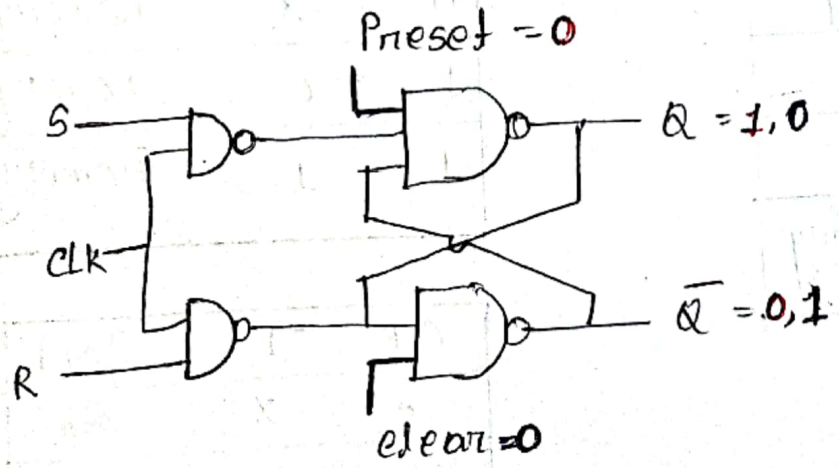
$T = \bar{Q}_n Q_{n+1} + Q_n \bar{Q}_{n+1}$

$= Q_n \oplus Q_{n+1}$

Preset and clear input:

1. Preset is used to make output $Q = 1$
2. clear input is used to make output $Q = 0$
3. Preset and clear input doesn't need synchronization.
4. It gives predefine output without bothering other inputs.

For nand, input = 0 ; output = 1



Preset = 0

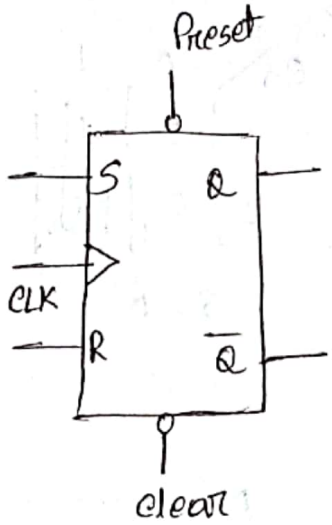
$Q = 1, \bar{Q} = 0$

clear = 0

$\bar{Q} = 1, Q = 0$

Truth table :

Preset	clear	Q_n
0	0	Not used
0	1	1
1	0	0
1	1	FF operation



SR to D Flip Flop conversion:

Steps: ① Note available flip flop and required flip flop
② Write characteristics table of required FF
③ Write Excitation table of available FF
④ Solve boolean expression
⑤ Draw circuit

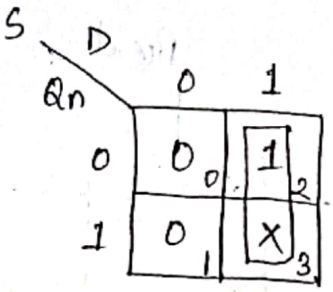
Here, Available Flip Flop → SR FF
Required Flip Flop → D FF

Characteristic table of required FF(DFF)

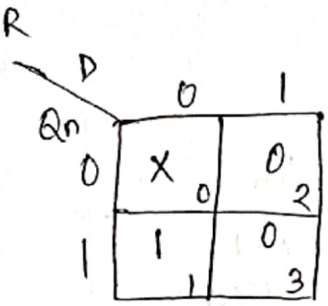
	Q_n	D	Q_{n+1}	S	R
0	0	0	0	0	X
2	0	1	1	1	0
1	1	0	0	0	1
3	1	1	1	X	0

Excitation table (SR)

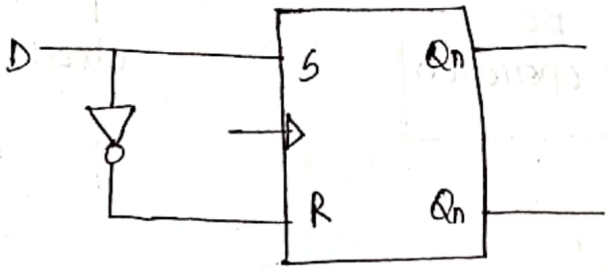
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



$S = D$



$R = \overline{D}$



SR to JK flip flop conversion:

① Note available FF and required FF

② characteristic table of required FF

③ Write excitation table of available FF

④ Solve Boolean expression

⑤ Draw circuit

Available Flip-flop = SR FF

Required Flip-flop = JK FF

characteristic-table of JK FF

JK Qn	Qn	J	K	Qn+1	S	R
0	0	0	0	0	0	X
2	0	0	1	0	0	X
4	0	1	0	1	1	0
6	0	1	1	1	1	0
1	1	0	0	1	X	0
3	1	0	1	0	0	1
5	1	1	0	1	X	0
7	1	1	1	0	0	1

characteristic-table ও SR ad এর Excitation Table এর

Excitation table of SR FF

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

S / Qn \ JK

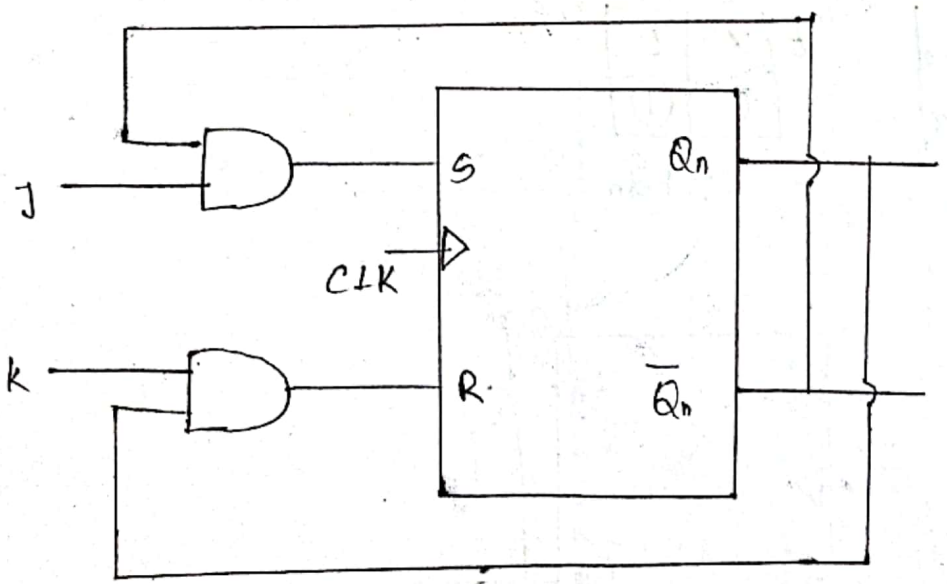
Qn	00	01	11	10
0	0 (0)	0 (2)	1 (6)	1 (4)
1	X (1)	0 (3)	0 (7)	X (5)

$S = \bar{Q}_n J$

R / Qn \ JK

Qn	00	01	11	10
0	X (0)	X (2)	0 (6)	0 (4)
1	0 (1)	1 (3)	1 (7)	0 (5)

$R = Q_n k$



SR to T flip flop conversion :

① Note available FF and required FF
② Write characteristics table of required FF
③ Write excitation table of available FF
④ Solve Boolean expression
⑤ Draw circuit.

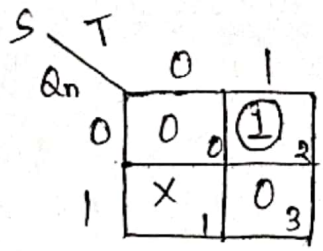
Here, Available FF = SR FF
Required FF = T FF

Characteristics table of T FF

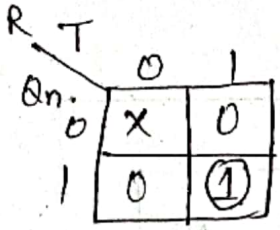
Q_n	T	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	1	0
1	0	1	X	0
1	1	0	0	1

Excitation table of SR FF

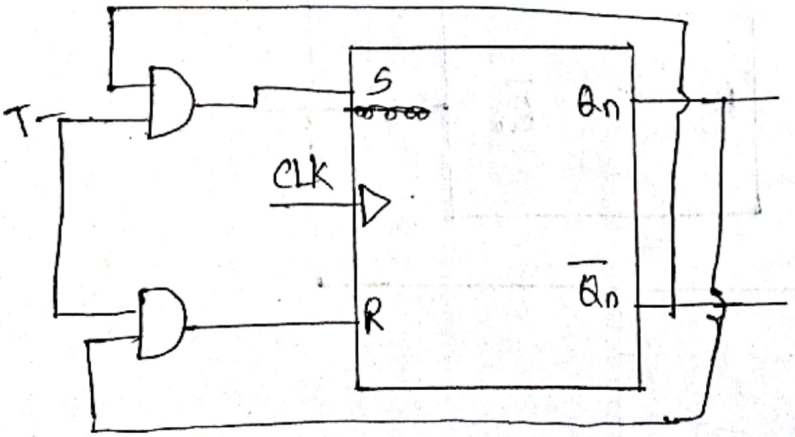
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



$S = T\bar{Q}_n$



$R = TQ_n$



Jk to D Flip Flop Conversion :

Steps – same as previous conversions.

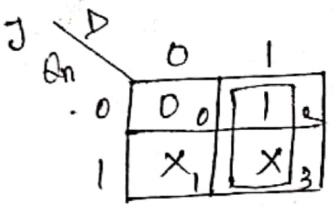
Here, Available FF = Jk FF
Required FF = D FF

Characteristic table of D FF

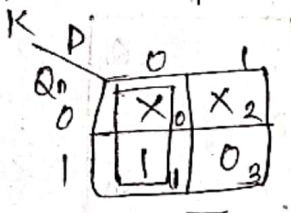
Qn	D	Qn+1	J	k
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

Excitation table of Jk FF

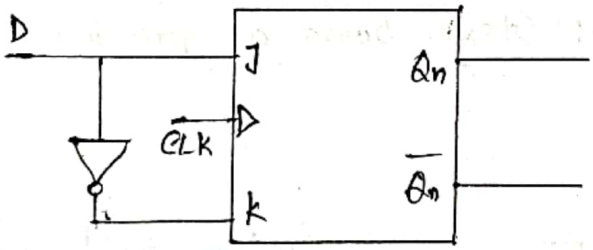
Qn	Qn+1	J	k
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



J = D



K = $\overline{D}$



Jk to T Flip Flop conversion: Steps – same as previous conversions

Here, Available Flip Flop = Jk FF
Required Flip Flop = T FF

Characteristic table T FF

Q_n	T	Q_{n+1}	J	k
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1

Excitation table of JK FF

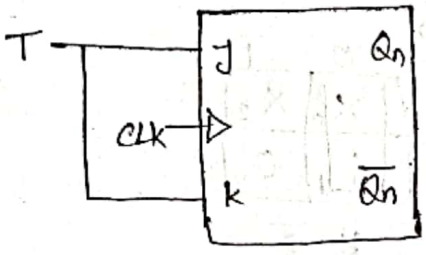
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J	T=0	T=1
Q_n=0	0 (0)	1 (2)
Q_n=1	X (1)	X (3)

$J = T$

K	T=0	T=1
Q_n=0	X (0)	X (2)
Q_n=1	0 (1)	1 (3)

$K = T$



D to T flip flop conversion: Steps: Same as previous conversion.

Available FF = D FF

Required FF = T FF

Characteristics table of T FF

Q_n	T	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Excitation table of D FF

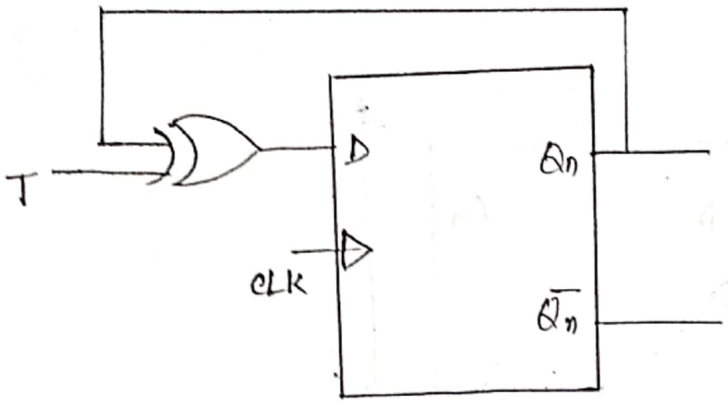
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

$Q_{n+1} = D$

D	T=0	T=1
Q_n=0	0 (0)	1 (2)
Q_n=1	1 (1)	0 (3)

$D = T\overline{Q_n} + \overline{T}Q_n$

$= T \oplus Q_n$



D To JK flip-flop conversion: Steps- Same as previous conversion

Here, Available FF = D FF

Required FF = JK FF

Characteristic table of JK FF

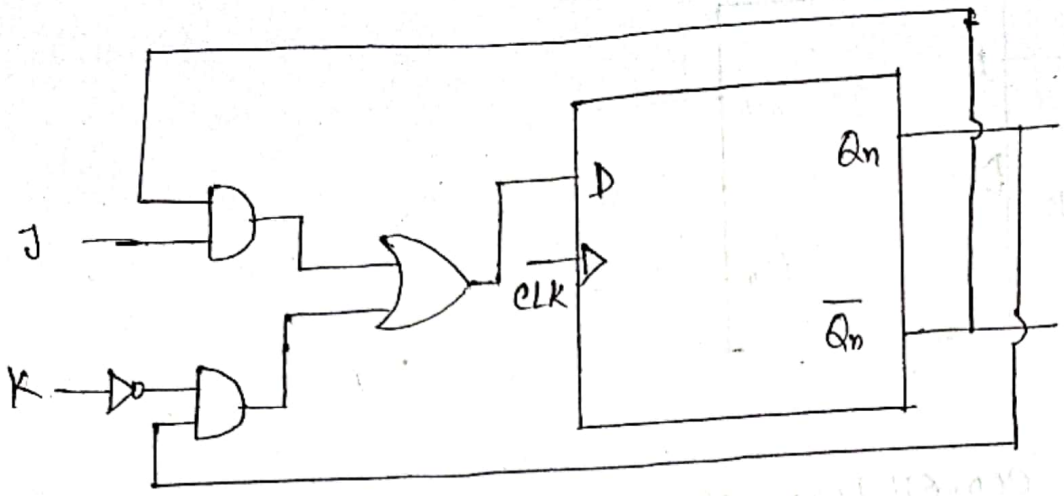
Q_n	J	K	Q_{n+1}	D
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0

Excitation table of D FF

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D / Q_n \ JK	00	01	11	10
0	0 (0)	0 (2)	1 (6)	1 (4)
1	1 (1)	0 (3)	0 (7)	1 (5)

$D = Q_n\overline{K} + \overline{Q_n}J$



T to D flip flop conversion: Steps- Same as previous conversion

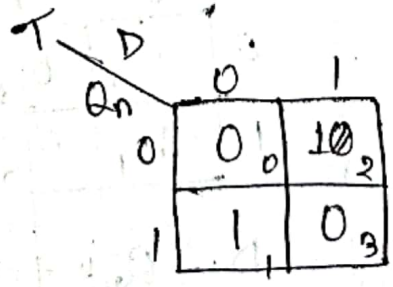
Here, Available FF = T FF
Required FF = D FF

Characteristic table of D FF

Qn	D	Qn+1	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

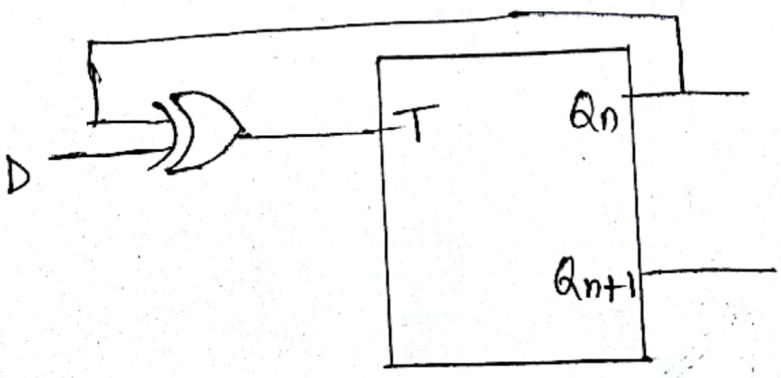
Excitation table of T FF

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0



$T = D\overline{Q_n} + \overline{D}Q_n$

$= D \oplus Q_n$



T to Jk flip-flop conversion: Steps- Same as previous conversion

Here, Available FF = T FF

Required FF = Jk FF

Characteristic table of Jk FF

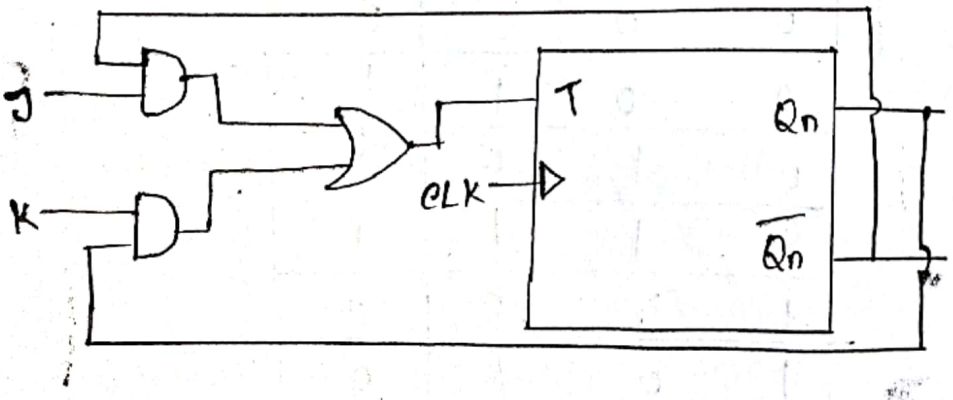
Q_n	J	K	Q_{n+1}	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

Excitation table of T FF

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T (JK) / Q_n	00	01	11	10
0	0_0	0_2	1_6	1_4
1	0_1	1_3	1_7	0_5

$T = Q_nK + \bar{Q}_nJ$



JK to SR, T to SR and D to SR Flip Flop conversion.

⇒ when S = 1 and R = 1 then Q_{n+1} = Invalid. But for JK, T and D, Q_{n+1} = It will never go in invalid state. So we cannot form JK to SR, T to SR and D to SR Flip Flop.

Examples on Flip Flop

① A New FF is having behaviour as described below. It has two inputs X and Y and when both inputs are same and they are 1,1. The FF is going to set else FF resets. If both inputs are ~~getting~~ different and they are 0,1 the FF complements itself otherwise it is going to retain the last state which of the following expression is the characteristics expression of the new FF?

(A) $X\bar{Q} + Y\bar{Q}$ (B) $X\bar{Q} + YQ$ (C) $X\bar{Q} + Y\bar{Q}$ (D) None

(Truth table)

Inputs		Output
X	Y	
0	0	0
0	1	$\bar{Q}$
1	0	Q
1	1	1

(characteristic table)

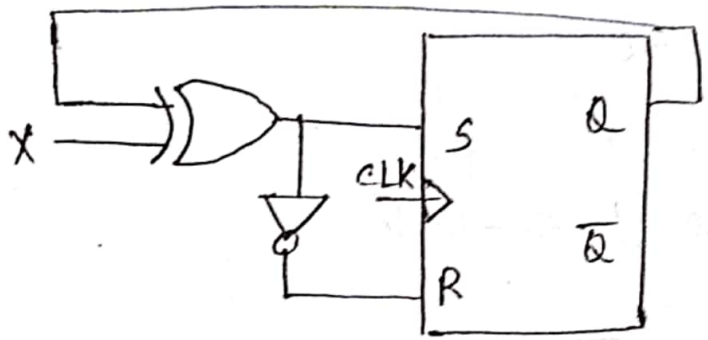
Q_n	X	Y	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Q_{n+1} / Q_n \ XY	00	01	11	10
0	0	1	1	0
1	0	0	1	1

$Q_{n+1} = \bar{Q}_n Y + Q_n X$

Ans A

② Make expression of Q^+ for given circuit.



A. XQ
B. $X\bar{Q}$
C. $X \oplus Q$
D. $X \odot Q$

X	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

$Q^+ = \bar{X}Q + X\bar{Q}$

$= X \oplus Q$