sequential cincuit

- Basics of sequential cincuit
- sequential cincuit vs combinational cincuit
- clock and thiggening by clock in requestial cincuitr.
- Difference between Latch and Flip Flopis
- SR Latch using NOR gaters
- SR Latch using NAND gotero
- D Latch
- 8. Example on Latch

Sequential cinemit

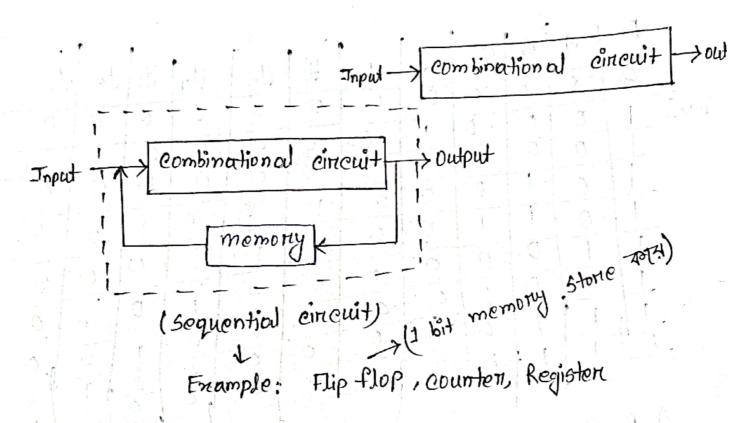
<u>Sequential cincuit</u>: It is a combinational cincuit and

memony.

Sequential

In combinational cinemit proceed output is only depends

on proceed input and past output.

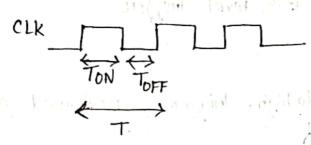


classification of sequential cincuit:

- D synchronous sequential cincuit: All memony elements work with same clock pulse.
- 2 Asynchronous sequential cincuit: Hemony elements one working with different clock pulse.

Vs combinational circuit Sequential cincuit combinational cincult cincuit Sequential 1) output depends on the present input O output depends on present input and past output @ Hemony alement is absent Memory element is priesent 3) No clock signal is Clock signal nequined applied. 4) Houlf Adder, Full Adder, Flip Flop, Counterro, Registers (H) Multiplexen Combinational cirreuit Combinational cinew+ memory

i clock' and 'triggering by clock' in requestial circuits clock is a signal, used in digital cincuit.

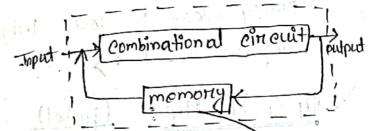


$$\Rightarrow$$
 Duty cycle, $D = \frac{T_{ON}}{T} = \frac{T_{/2}}{T} = \frac{1}{2} = 0.5$

as out as boundon napports of the state prince 田 operational speed and transition of state is defined by clock in sequential cinewit

> Output of a cincuit is defined as state.

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> output state will change with respect to clock.

772

clock is used to control the operational speed and transition of state.

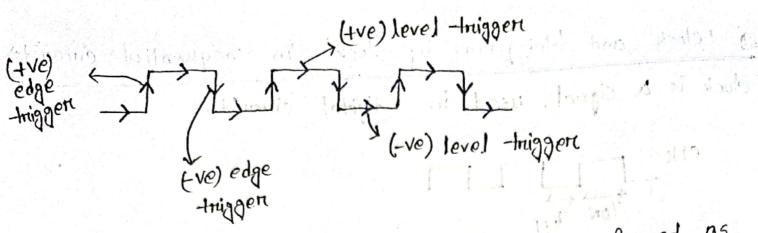
Typen of clock this gening:

not int lived (3) H

There are two types of clock triggering

D Edge tniggen clock: the Edge tniggen -ve Edge trigger

@ Level thiggen clock: the level thiggen -ve level thigger



- → clock naise from low to high, triggene meterned as
- > clock falls from high to low, thiggen neferred as -ve edge tniggen. T
- > Duning clock is high, thiggen nefermed as the level
- ⇒ Duning clock is low, triggen neferned as -ve level La thing gen transferred the trager of this is a to finish to

西 SR Flip flop: (Symbol)

S-SR-Q.
FF Q

transition of right

CHK — D (+ve) Foge triggen CLK -OD (-ve) Edge triggen CLK - (+ve) Level triggen CLK — 0 (-ve) level triggett

to south any and susul choose mindlensial a second when some : The Egille . Pills in

-Ve Edge Auggere C Level thigger clock: the level thiggers

ruppink hovel av-

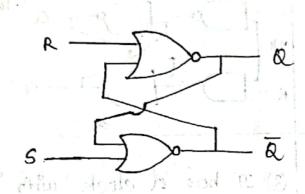
/	· . L. a. as at Gardo d
Latch	Flip-flop
D Hade by logic gators only. 1 It is structured based on logic gates block. R R D R	D Hade by Jogie gottos and latch. This structured based on blocks of latch and logic gates.
3 To doesn't have clock in its intermal cincuit.	2) It has a clock with its internal cincuit.
	1 It is edge Iniggen.
(9) It cannot be used as megiston.	
5 It is Asynchronous Cincuit.	1) It is Synchronous cincuit
6 7 nequiness less power.	6 It requires more power.
1) It is factor.	1) It is slower.
Designing is less complex.	(8) Deroigining is more complex.
The is sensitive to input	17 is sensitive to imput
signal only.	and clock signal.
d & & b	6-1, R-0, R-1, av
R = C - 1 Rapha like	6=0, R=0, S=1 cm
A Section of the sect	

5R Latch using NOR gators:

- 1 Cinemit of SR Latch writing NOR goto
- 1 Working of SR Latch using NOR gate
- 1 Thuth table of SR Latch using wor gate

g = set R = Renet

Cincuit:



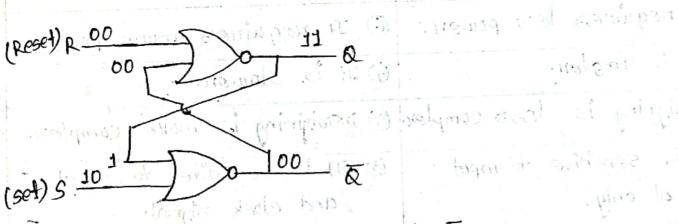
$$R \rightarrow Q$$
 $5 \rightarrow \overline{R}$

R and & should be complement of each other for Proper openiation of sk Latch

If Q=Q' then that's an invalid state.

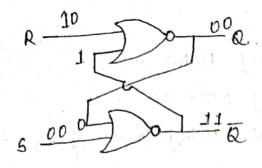
Working: susandanya of the thronis among

Non GA 1910 Resolt Was

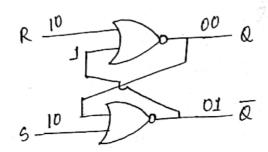


$$5=1$$
, $R=0$, $Q=1$, and $\overline{Q}=0$

$$6=0$$
, $R=0$, $Q=1$ and $\overline{Q}=0$ — It actso like memory.



G=0, R>1, Q=0 and $\bar{Q}=1$ 6 = 0, R = 0, Q = 0 and Q = 1 It acts like memory



6=1, R=1, Q=0 and $\overline{Q}=0$ Invalid case I condition Violation

$$5=0$$
, $R=0$, $Q=0$ and $\overline{Q}=1$ } undersined ease on, $Q=1$ and $\overline{Q}=0$

Truth table:

h table:				to the book of the state
	5	R	100	
	0	0	Hemory 0 1	Acts as memorry
	0	1	0 1	
	1	0	1 0	
	1	1	Invalid	

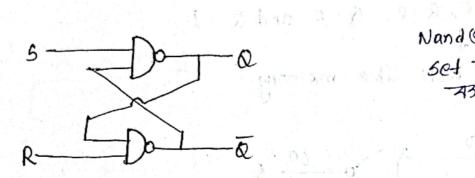
@ Values of Q and Q will always be complements of each other. Otherwise it's an invalid case.

Soll Red Red and . Red

5R Latch using NAND gaters.

- 1) Cinemit of GR Ladeb wring NAND goders
- @ WOHKing of SR Ladeb using NAND godos
- 3 Thuth table of SR Latch using NAND gotters

Cincuit:



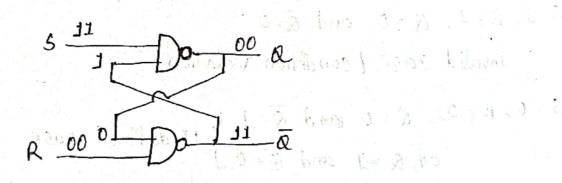
Nand 97 10013 Set जाता

ralant divin

C Hemony

to Both on Or Both of

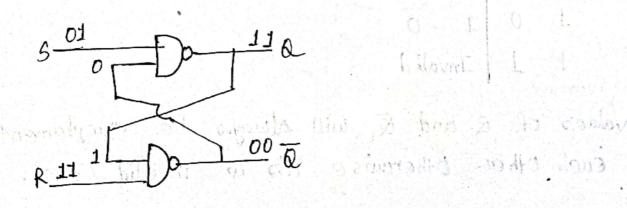
Working:



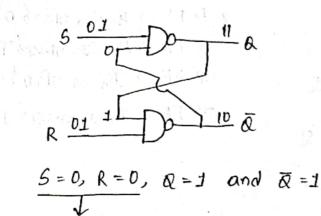
S=1, R=0, Q=0 and
$$\overline{Q}=1$$

S=1, R=1, Q=0, and $\overline{Q}=1$

Acts as memory



5=0, R=+, Q=1 and Q=0 5=1, R=1, Q=1 and R=0



Invalid case / condition violation

$$S=1$$
, $R=1$, $Q=1$ and $\overline{Q}=0$ undefined on $Q=0$ and $\overline{Q}=1$

Truth Table

5	R	la ā	S. S. S. S. S. S. Santo Symmetry
0	0.	Invalid	situation best whater therefore
0	1	1 0	
1	0	0 1	Libragat book whater from the
1	1	Hemory	

@ In NAND gate, output will always be I if one of me inputo is Beno. [WE THAN 02]

to plade in all agreeds Block Collection

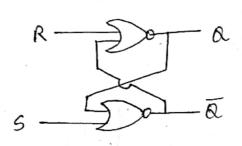
Characteristiques : Malera

EwoHalless Fleship

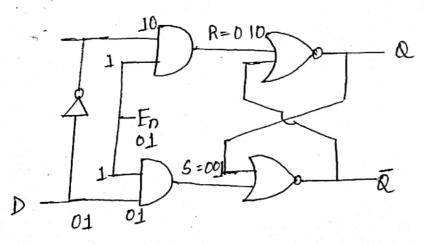
D latch: D latch does not have clock input and D-flip-flop has clock input.

output = Input when Enable = 1 output = memorry when En =0

SP Latch using non gate - Inuth -table

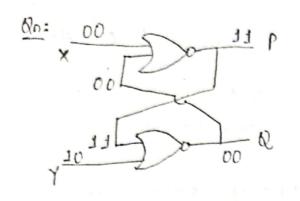


6	R.	Q Q
0	0	memony
0	1	0 1
1	0	10
1	1	Invalid



En	D	Q
0	X	mem
1	O	0
1	1	1

Frample on Latch



If input my changes from 04 to 00 then output po will change from ? to ?

when my is 01 PR will be 10

If input my changes from 01 to 00 then output PR

will changes from 10 to 10.

χ 01 10 P

If input my changes from 01 to 11.

Then PR will changes from ___ to __.

From 11 to 01

If input my changes from 11 to 00

then PR will changer from _ to _

[Initially PR is 00]

If input my changes from 11 to 00 then po will changes from 01 to 01.