

GROUP-A

Q1 What is Multivibrator? Write down its applications.

A multivibrator is an electric circuit used to implement a variety of simple two-state devices such as relaxation oscillators, timers and flip-flops. It consists of two amplifying devices (transistor, vacuum tubes or other devices) cross coupled by resistors or capacitors.

Applications :

1. As frequency dividers
2. As saw-tooth generator
3. As square wave and pulse generator
4. As memory elements in computers.

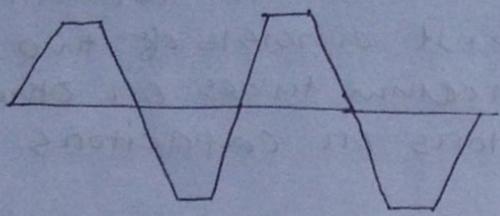
Q2 Why a Bistable MV is called flip-flop? What are applications of Bistable MV?

Bistable MV has two stable states and maintains a given output state indefinitely unless an external trigger is applied forcing it to change state. As Bistable MV has two states (stable), they are more commonly known as latches and flip-flops for using in sequential circuits. It can be flipped from one state to other by an external trigger pulse. So Bistable MV is also known as a flip-flop.

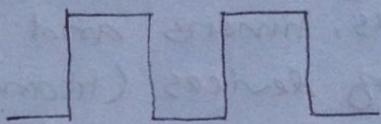
Application :

1. In digital operation in computers, digital communications.
2. For reversing the supply to a given ckt or change supply to two cks at regular intervals.

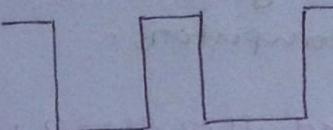
Q1 Draw the output wave form of Astable, Monostable & Bistable MV.



(a) Astable



(b) Monostable



(c) Bistable

Q2 Describe the operation of Astable MV in state machine

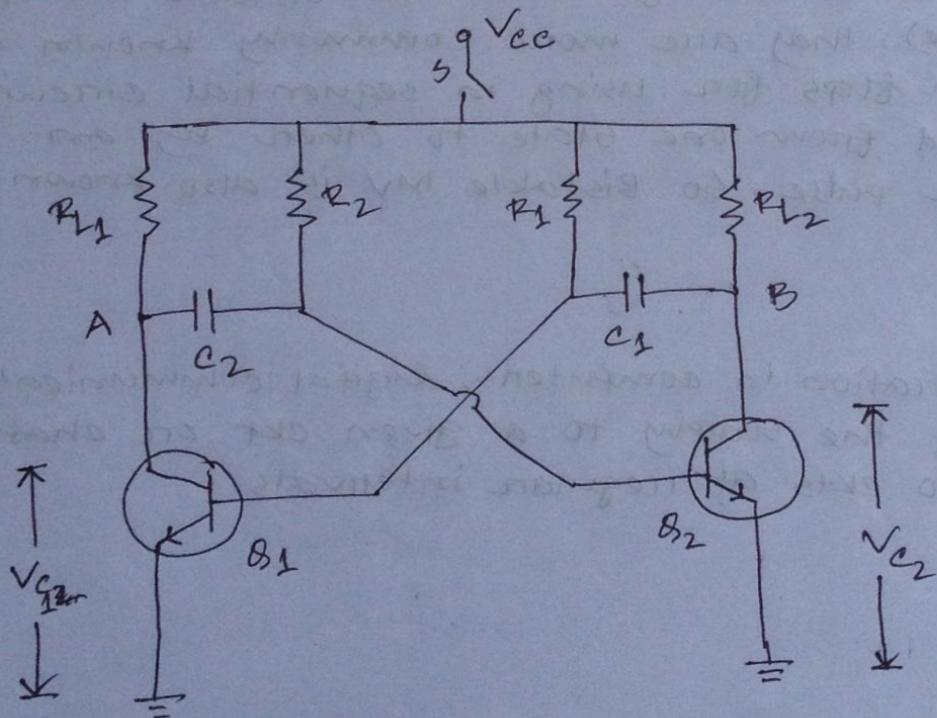


Fig: Circ diagram of Astable MV

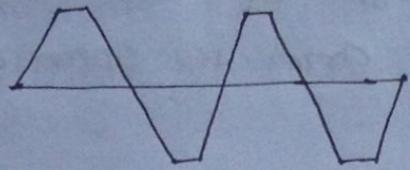


Fig: Output wave form of Astable MV

Operation:

i) When B_1 is on, B_2 is off.

ii) When B_2 is on, B_1 is off.

When the power is switched on by closing S, one of the transistors will start conducting before the other. It is so because characteristics of two similar transistors can't be exactly alike. Let us assume B_1 starts conducting before B_2 does. The feedback system is such that B_1 will be very rapidly driven to saturation and B_2 to cut-off. The following sequence of events will occur:

- ① since B_1 is in saturation, whole V_{ce} drops across R_{L1} . Hence $V_{c1} = 0$ and point A is at zero or ground potential.
- ② since B_2 is in cut-off i.e. it conducts no current, there is no drop across R_{L2} . Hence Point B is at V_{ce} .
- ③ since A is at OV, C_2 starts charging through R_2 towards V_{ce} .
- ④ when voltage across C_2 rises sufficiently (more than 0.7V), it biases B_2 in the forward direction so that it starts conducting and is soon driven to saturation.
- ⑤ V_{c2} decreases and becomes almost OV when B_2 gets saturated. The potential of Point B decreases from V_{ce} to almost OV. This potential decreasing is applied

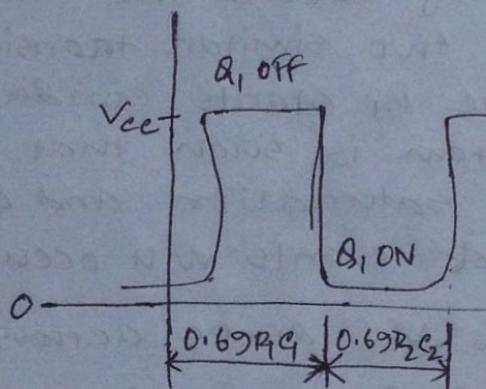
to the base of B_1 through C_1 . consequently B_1 is pulled out of saturation and is soon driven to cut-off.

6. Since point B is at OV now, C_1 starts charging through R_1 towards V_{cc} .

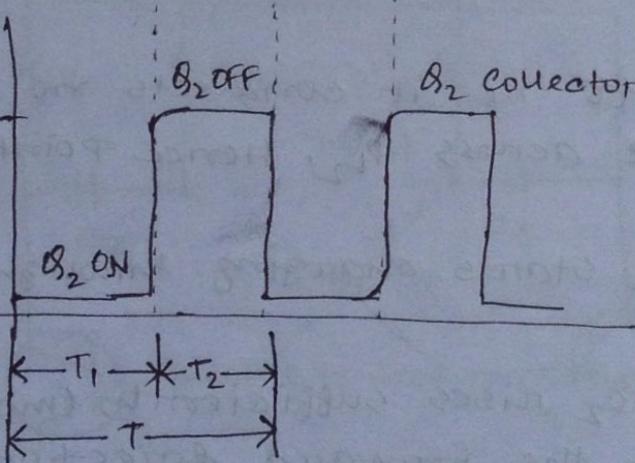
Q1 How can you generate square wave form from Astable MV?

ANSWER

[Operations (1-4) from previous question]



B_1 Collector



B_2 Collector

Q1 Determine the value of capacitors to be used in an astable multivibrator to provide a train of 1ms rise at a repetition rate of 100kHz. Given $R_1 = R_2 = 10k$.

Solⁿ

Given,

$$f = 100 \text{ kHz}$$

$$R_1 = R_2 = 10k\Omega$$

$$\tau_1 = 1\text{ms}$$

We know,

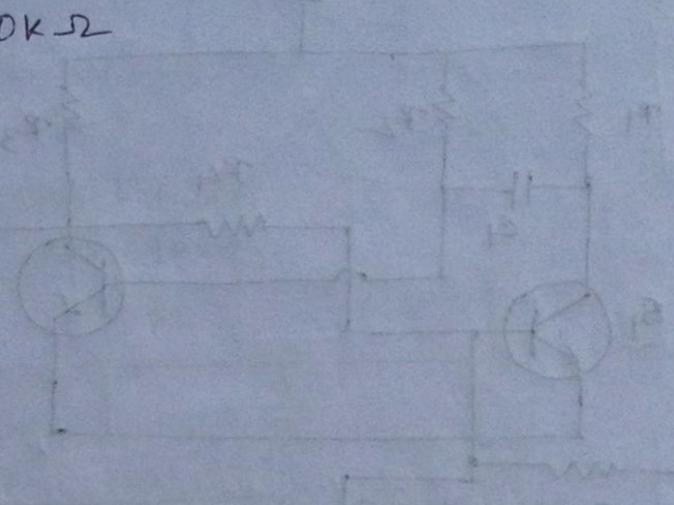
$$T = \frac{1}{f}$$

$$= \frac{1}{100k}$$

$$= 10^{-5} \text{ s}$$

$$= 10 \times 10^{-6} \text{ s}$$

$$= 10 \text{ ms}$$



$$\text{Again, } T = \tau_1 + \tau_2$$

$$\therefore \tau_2 = T - \tau_1$$

$$= 10 - 1$$

$$= 9 \text{ ms}$$

$$\text{So, } \tau_1 = 0.69 R_1 C_1$$

$$\text{and, } \tau_2 = 0.69 R_2 C_2$$

$$\Rightarrow C_1 = \frac{\tau_1}{0.69 R_1}$$

$$\Rightarrow C_2 = \frac{\tau_2}{0.69 R_2}$$

$$= \frac{1 \text{ ms}}{0.69 \times 10k}$$

$$= \frac{9 \text{ ms}}{0.69 \times 10k}$$

$$= 1.45 \times 10^{-10} \text{ F}$$

$$= 1.3 \times 10^{-9} \text{ F}$$

(Ans)

Q1 Describe the operation of a Monostable MV.

A MV in which one transistor is always conducting and the other is non-conducting ~~is~~ is called Monostable MV.

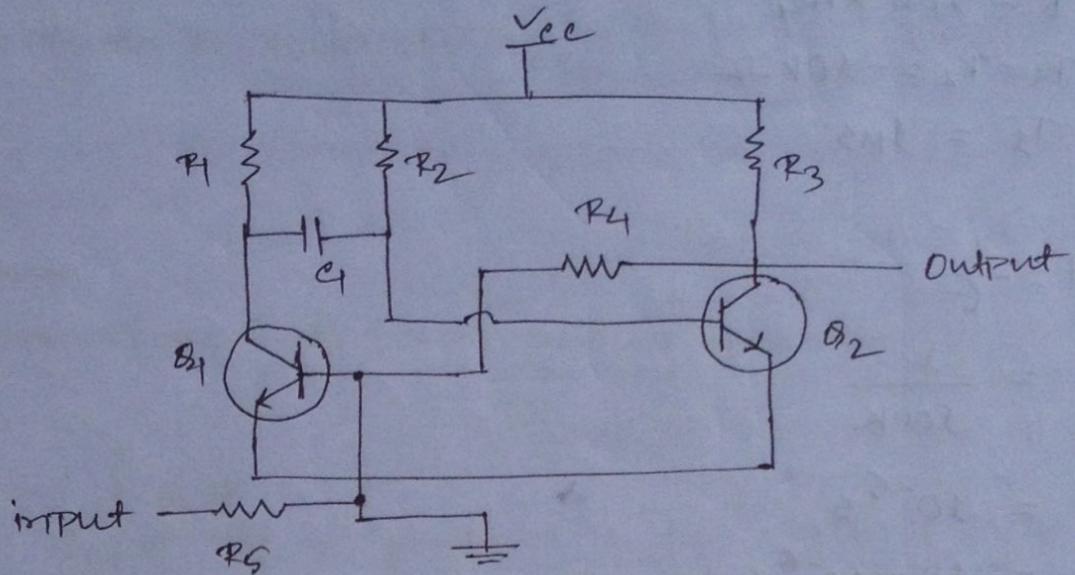


Fig: Monostable MV

Ckt Operation

1. When there is no external trigger to the ckt, the one transistor will be in saturation state and the other will be in cut off state. β_1 is in cut off mode and put at negative potential until the external trigger to operate, β_2 is in saturation mode.
2. Once the external trigger is given to the input, β_1 will get turn on and when β_2 & β_1 reaches the saturation, β_1 will make β_2 turn off. This is called quasi state.
3. When β_1 changes to V_{cc} , β_2 will turn on again and automatically β_1 will be turned off. So, the time

period for charging of capacitor through the resistor is directly proportional to the quasi state when an external trigger occurred ($t = 0.69 RC$)

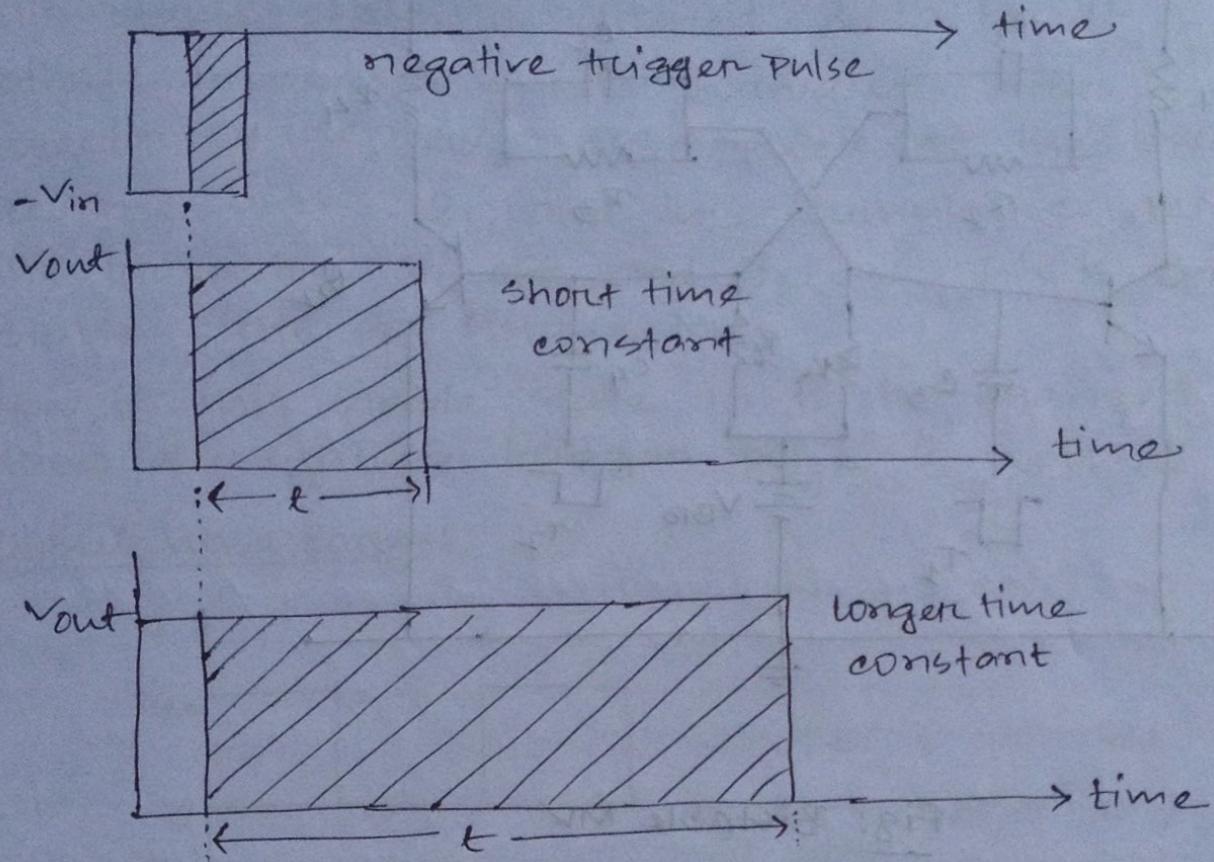


Fig: Monostable waveform

Describe the operation of a Bistable MV.

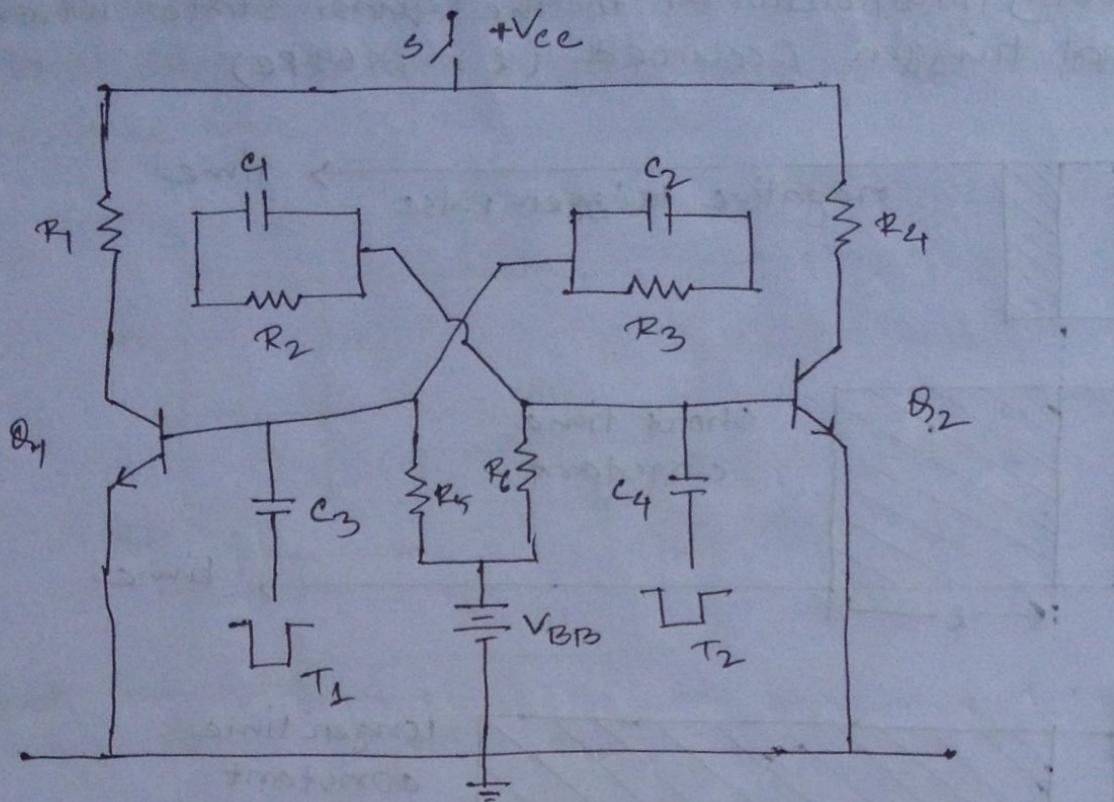


Fig: Bistable MV

Operation:

The Bistable MV can be switched over from one stable state to the other by the application of an external trigger pulse. Thus it requires two external trigger pulses before it returns back to the original state.

The Bistable MV ckt above is stable in both sides, either with one transistor OFF and the other ON or vice versa.

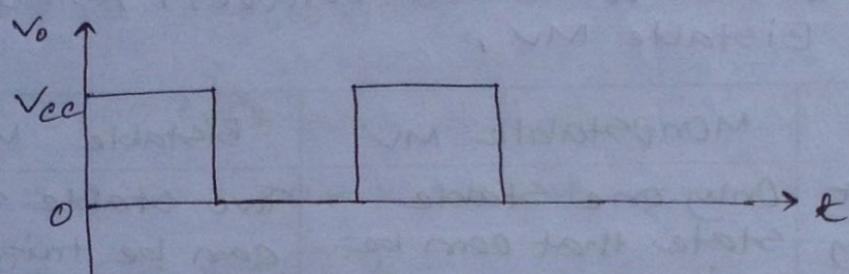
When the ckt is switched ON, one the transistors say Q_1 gets switched ON while the other Q_2 gets switched OFF. due to different doping levels of the

transistors. This is a stable state of the Bistable MV.

By applying a negative trigger at the base of B_1 , this stable state is altered. As a result the collector voltage increases which forward biases B_2 . The collector current of B_2 as applied at the base of B_1 , reverse biases B_1 , and this cumulative action makes the transistors B_1 OFF and B_2 ON. This is another stable state of Bistable MV.

Now, if this stable state is to be changed again, then a negative trigger pulse is applied at B_2 .

Output Waveform:



Q1 Classify MV. Explain each of them.

An MV is a circuit that oscillates between a High state and a Low state producing a continuous output. There are 3 types of MV.

1. Astable MV: This is a circuit with an oscillating output. It doesn't need any external trigger and it has got no stable state. It is a type of regenerative oscillator.

It is used in applications where low clock frequency pulse train is required.

2. Monostable MV: It is a ckt where output is ~~not~~ in only one stable state. It is also known as one-shot MV. In a monostable MV, the output pulse duration is determined by the RC time constant. It is used as pulse generator, also used to produce time delay in circuits.

3. Bi-stable MV: It is a ckt with two stable states: High and Low. Generally a switch is required for toggling between the high and low state of the output. It is used in counting ckt's and in memory storage units.

Mention the major differences between Astable, Monostable and Bistable MV.

Astable MV	Monostable MV	Bistable MV
No astable state but switches continuously between between two states.	Only one stable state that can be switched from stable state to a quasi stable state by an external trigger.	Two stable states, can be triggered from one to the other by an external signal.
It is also called free running relaxation oscillator.	It is also known as single-shot or one-shot MV.	It is also known as flip flop-MV.
It is used as square wave frequency generator.	It is used as delay and timing ckt's	It is used to force reversing supply to a given ckt.
It has two energy storing capacitors.	It has one capacitor as energy storage element.	It has no energy storing element.
Used for blazing blasing lights, switching and power supply ckt's.	Used for temporary memories.	Used for digital operations in computers, digital communications.

Q1 In an Astable MV circuit, $R_1 = R_2 = 10\text{ k}\Omega$, $R_{34} = R_{56} = 1\text{ k}\Omega$ and $C_1 = C_2 = 0.01\text{ }\mu\text{F}$. calculate frequency of pulse.

Soln:

Given,

$$R_1 = R_4 = 1\text{ k}\Omega$$

$$R_2 = R_3 = 10\text{ k}\Omega$$

$$C_1 = C_2 = 0.01\text{ }\mu\text{F}$$

$$f = ?$$

$$\begin{aligned} T_1 &= 0.69 R_1 C_1 \\ &= 0.69 \times 1\text{ k} \times 0.01\text{ }\mu\text{F} \\ &= 6.9 \times 10^{-6}\text{ s} \end{aligned}$$

$$\therefore f_1 = \frac{1}{T_1} = \frac{1}{6.9 \times 10^{-6}} = 144.93\text{ kHz} \quad (\text{Ans})$$

$$\begin{aligned} T_2 &= 0.69 R_2 C_2 \\ &= 0.69 \times 10\text{ k} \times 0.01\text{ }\mu\text{F} \\ &= 6.9 \times 10^{-5}\text{ s} \\ \therefore f_2 &= \frac{1}{T_2} = \frac{1}{6.9 \times 10^{-5}} = 144.9\text{ kHz} \quad (\text{Ans}) \end{aligned}$$

Q2 What is the difference between Multivibrator & Oscillator?

MV	Oscillator
It is a two-stage RC coupled amplifier ckt.	It is an electronic ckt.
It can generate square signal without ac input.	It can generate sine signal without oscillating input with the use of positive feedback.

Pulse Transformer

The transformer which handles voltage & current in the form of pulses ~~are~~ is called pulse transformer.

Importance of Pulse Transformer

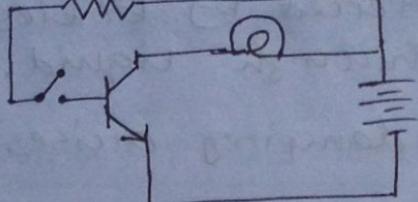
1. For changing the amplitude of a voltage pulse.
2. For inverting polarity of a pulse.
3. For affecting the isolation between source & load.
4. For coupling different stage of pulse amplifier.

Features of an ideal pulse transformer

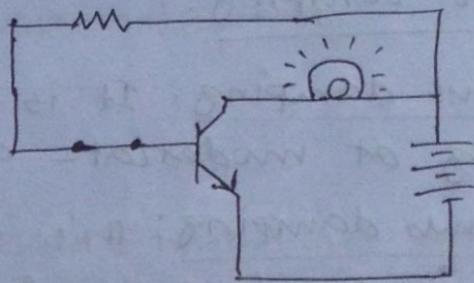
1. $n \rightarrow$ Primary to secondary turns ratio
2. $Vt \rightarrow$ minimum voltage \times time area
3. $L_p \rightarrow$ Primary winding inductance
4. $L_s \rightarrow$ Primary Leaking inductance
5. $R_p \rightarrow$ Primary winding resistance
6. $R_s \rightarrow$ Secondary winding resistance
7. $t_r \rightarrow$ rise time
8. $C_k \rightarrow$ coupling capacity between windings
9. $I_{max} \rightarrow$ Maximum secondary current
10. $I_p \rightarrow$ Thermal current
11. $f_o \rightarrow$ optimum frequency range

Switching behavior of a transistor

One of the most common uses of transistors in an electronic circuit is as simple switches. In short, a transistor conducts current across the collector-emitter path only when a voltage is applied to the base. When no base voltage is present, the switch is OFF, ON otherwise.



(a)



(b)

Figure: An NPN Transistor : (a) Cut-off, Lamp OFF
(b) Saturated, Lamp ON

In an ideal switch, the transistor should be in only one of the two states: OFF or ON.

- 1) The transistor is OFF when there is no bias voltage or when the bias voltage is less than 0.7V.
- 2) The switch is ON when the base is saturated so that collector current can flow without restriction.



against triode

Q1 Define co-efficient of coupling. Explain different types of damping.

Co-efficient of Coupling: The function of magnetic flux produced by the current in one coil that links with the other coil is called co-efficient of coupling between the two coils. It is denoted by k .

Types of Damping:

1. Viscous damping: It is encountered by bodies moving at moderate speed through liquid.
2. Coulomb damping: This type of damping arises from sliding of dry surfaces.
3. Solid/ Structured damping: This is due to internal friction within the material itself.
4. Slip damping: Energy of vibration is dissipated by microscopic slip on the interfaces of machine parts in contact under fluctuating loads.

Q2 Describe the operation of a Schmitt trigger. How do you use this as a triggering pulse generator?

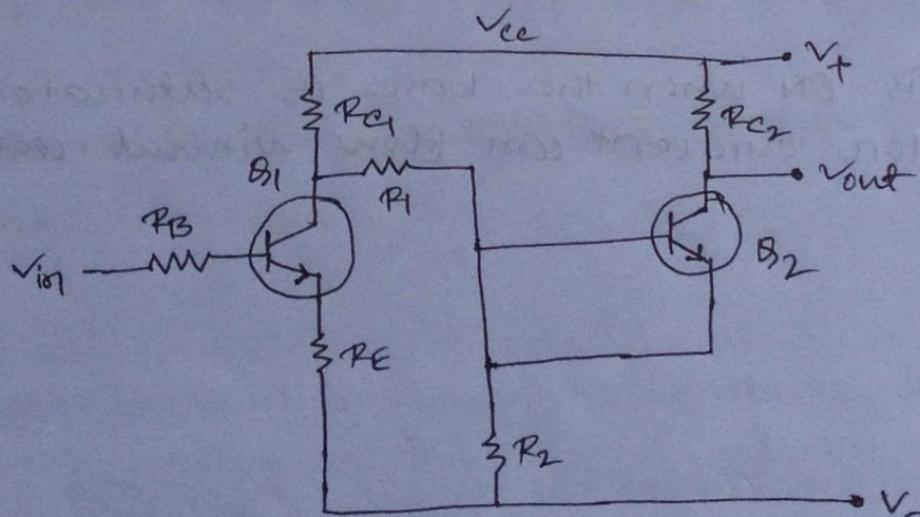


Fig: Schmitt Trigger

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Operation:

1. Initial State: For the npn transistor the input voltage is below the shared emitter voltage. So that β_1 base-emitter junction is reverse biased and β_2 doesn't conduct. The β_2 base is determined by the mentioned divider. So that β_2 is conducting and the trigger output is in low state.

The high threshold value is approximately

$$V_{HT} = \frac{R_E}{R_E + R_{C2}} \times V_T$$

2. Crossing up the high threshold: When the input voltage rises up slightly above the voltage across the emitter resistor R_E , β_1 begins conducting. Its collector voltage goes down and β_2 begins going cut-off because the voltage divider now provides lower β_2 base voltage.

The low threshold value is approximately

$$V_{LT} = \frac{R_E}{R_E + R_{C1}} \times V_T$$

3. Crossing down the low threshold: With the trigger now in the high state, if the input voltage lowers enough, β_1 begins cut-off. Its collector current reduces, as a result output voltage becomes low.

The operation is cumulative and ends up with

- (a) β_1 conducting at saturation with its collector voltage almost zero.
- (b) β_2 becoming cut off with its collector voltage nearly V_{cc} .

In this way, we use Schmitt as triggering pulse generator.

Q1 How can you generate square wave from Astable MV?

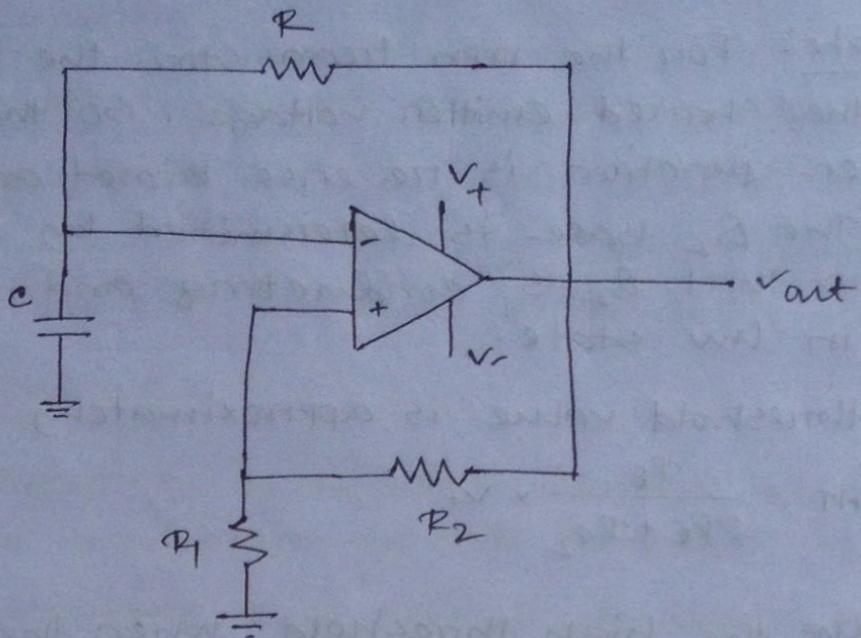


Fig: Astable MV

The time period of square wave

$$T = 2 \times RC \times \ln\left(\frac{1+\beta}{1-\beta}\right)$$

Let us assume $R_1 = R_2$, then $T = 2C \ln(3)$

Ckt Analysis:

The output of OPAMP is $+V_{cc}$ if $V_2 \gg V_1$ and
is $-V_{cc}$ if $V_2 \ll V_1$

Let us assume that the output is initially $+V_{cc}$. By voltage divider rule at non-inverting terminal of OPAMP,
voltage is $V_{cc} \times \frac{R_1}{R_1 + R_2}$

Now the capacitor starts charging through R with
time constant RC and the voltage across capacitor
is

$$V_C = V_{cc} \times (1 - \exp(-R \times C \times t))$$

Now,

$V_C = -V_{CC} \times \frac{R_1}{R_1 + R_2}$, when the voltage across the capacitor just more than $V_{CC} \times \frac{R_1}{R_1 + R_2}$ at the instant when

$V_1 \ll -V_{CC} \times \frac{R_1}{R_1 + R_2}$, output will be $+V_{CC}$.

Hence the voltage across capacitor switches between $-V_{CC} \times \frac{R_1}{R_1 + R_2}$ and $+V_{CC} \times \frac{R_1}{R_1 + R_2}$ and the output switches between $+V_{CC}$ and $-V_{CC}$.

The voltage across the capacitor during charging time is given by

$$V_C = V_{CC} \times \left\{ 1 - (1+\beta) \exp(-t/(2RC)) \right\} \quad \text{--- (1)}$$

where $\beta = \frac{R_1}{R_1 + R_2}$

at $t = \frac{T}{2}$, $V_C = \beta \times V_{CC}$

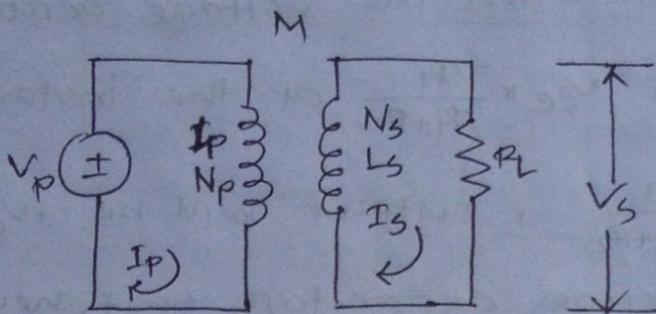
Hence from (1),

$$\beta \times V_{CC} = V_{CC} \times \left\{ 1 - (1+\beta) \exp(-T/(2RC)) \right\}$$

$$\therefore T = 2RC \ln \left(\frac{1+\beta}{1-\beta} \right)$$

which is the time period of a square wave.

Draw the transformer model of a pulse transformer.



L_p → Primary inductance

N_p → Primary turns

I_p → Primary current

V_p → Primary voltage

Coefficient of coupling between secondary & primary is denoted by k where

$$k = \frac{M}{\sqrt{L_p L_s}}$$

For ideal transformer, L_p is infinite and $k=1$.
In this case, output V_s is same as input.

$$\text{So, } \frac{V_s}{V_p} = \frac{I_p}{I_s} = \frac{N_s}{N_p} = \sqrt{\frac{L_s}{L_p}} = n$$

E Draw the equivalent circuit of an ideal transformer, then write the mesh equations and draw the circuit for the condition $\alpha = k\sqrt{L_P/L_S}$

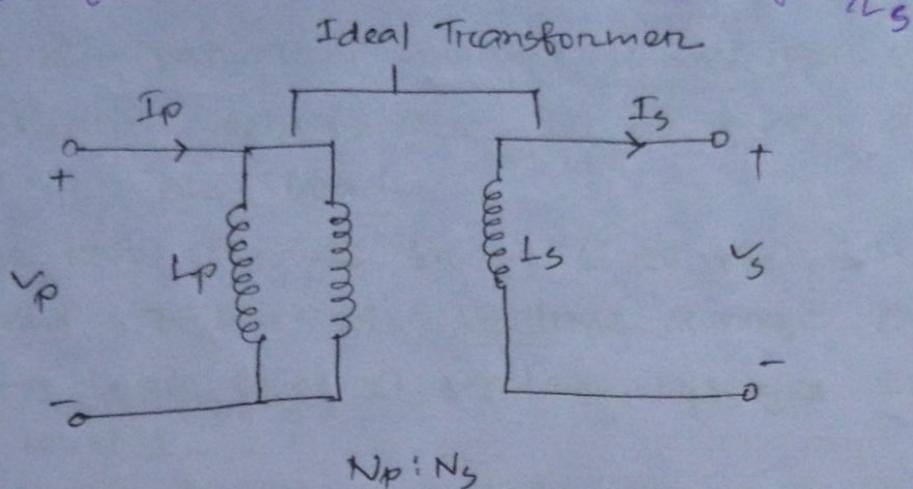


Fig: Equivalent ckt of an ideal transformer

Mesh Eqn: Mesh analysis is a method that is used to solve planar circuits for the currents at any place in the electrical circuit.

$$\text{For mesh 1: } V_p = j\omega L_P I_P - j\omega M I_S$$

$$\text{For mesh 2: } V_S = j\omega M I_P - j\omega L_S I_S$$

Uses of Schmitt trigger

1. Schmitt triggers are typically used in open loop configurations for noise immunity and closed loop configurations to implement function generators.
2. Squaring circuit
3. Amplitude comparator
4. Sine to square comparator
5. Flip-flops.

GROUP-B

Common features / characteristics of TTL logic gates

1. Power dissipation is usually 10 mW per gate.
2. Propagation delays are 10 ns when driving a 15 pF/400 ohm load.
3. Voltage level ranges from 0 to V_{cc} where V_{cc} is typically 4.75 V - 5.25 V. Voltage range 0V - 0.8V creates logic level 0. Voltage range 2V - V_{cc} creates logic level 1.

Working principle of 2-input NAND gate with totem pole output

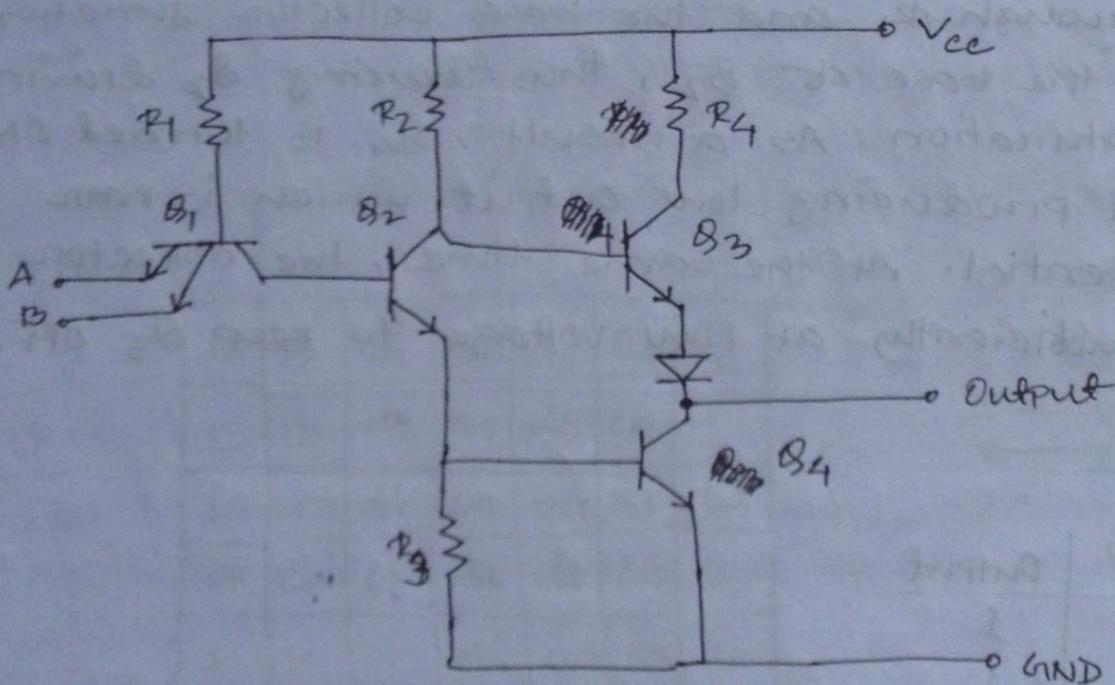


Fig: 2-input TTL NAND gate with totem pole output

If A or B is low, the base-emitter junction of Q_1 is forward biased and then its base collector junction is reverse biased.

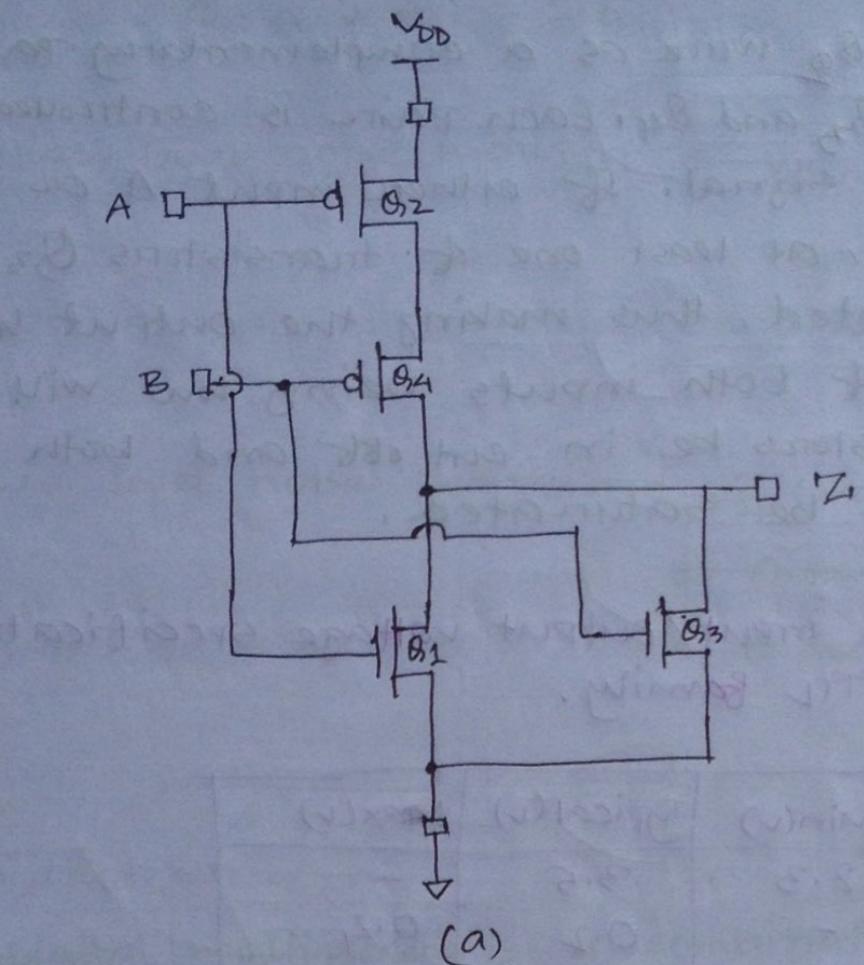
Then there is a current from V_{cc} through R_1 to the base-emitter junction of Q_1 , and into the low input. Hence there is no current into the base of Q_2 and making it into cut off. The collector of Q_2 is high and turns Q_3 into saturation. At the same time emitter of Q_2 is at ground potential, keeping Q_4 off.

When A and B are high, the two input base-emitter junctions of Q_1 are reverse biased and its base-collector junction is forward biased. This permits current through R_1 and the base-collector junction of Q_1 into the base of Q_2 , thus driving Q_2 into saturation. As a result, Q_4 is turned ON by Q_2 and producing low output which is near ground potential. At the same time, the collector of Q_2 is sufficiently at low voltage to keep Q_3 off.

Truth Table:

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Two input NOR Gate using CMOS



A	B	Q ₁	Q ₂	Q ₃	Q ₄	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(b)

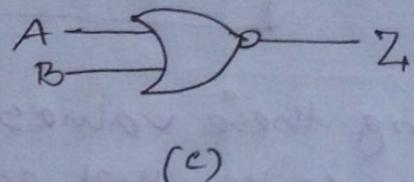


Fig: CMOS 2-input NOR gate

- (a) circuit diagram
- (b) Function table
- (c) Logic symbol

Operation: A CMOS NOR gate ckt uses 4 MOSFET.

Transistors Q_1 and Q_2 work as a complementary pair as do transistors Q_3 and Q_4 . Each pair is controlled by a single input signal. If either input A or input B are high, at least one of transistors Q_3 or Q_4 will be saturated, thus making the output low. Only in the event of both inputs being low will both lower transistors be in cut off and both upper transistors be saturated.

Table below shows input/output voltage specification for the standard TTL family.

Parameter	Min(v)	Typical(v)	Max(v)
V_{OH}	2.3	3.5	-
V_{OL}	-	0.2	0.4
V_{IH}	2.0	-	-
V_{IL}	-	-	0.8

Using these values, find (a) the maximum value of noise spike that can be tolerated when a HIGH output is driving an input.

(b) the maximum value of noise spike when a Low output is driving an input.

Soln:

Given,

$$V_{OH}(\text{min}) = 2.3 \text{V}$$

$$V_{IH}(\text{min}) = 2.0 \text{V}$$

$$V_{OL}(\text{max}) = 0.4$$

$$\bullet V_{IL}(\text{max}) = 0.8$$

(a) High level noise margin = $V_{OH}(\text{min}) - V_{IH}(\text{min})$
= $2.3V - 2.0V$
= $0.3V$ Ans.

(b) Low level noise margin = $V_{IL}(\text{max}) - V_{OL}(\text{max})$
= $0.8V - 0.4V$
= $0.4V$ Ans.

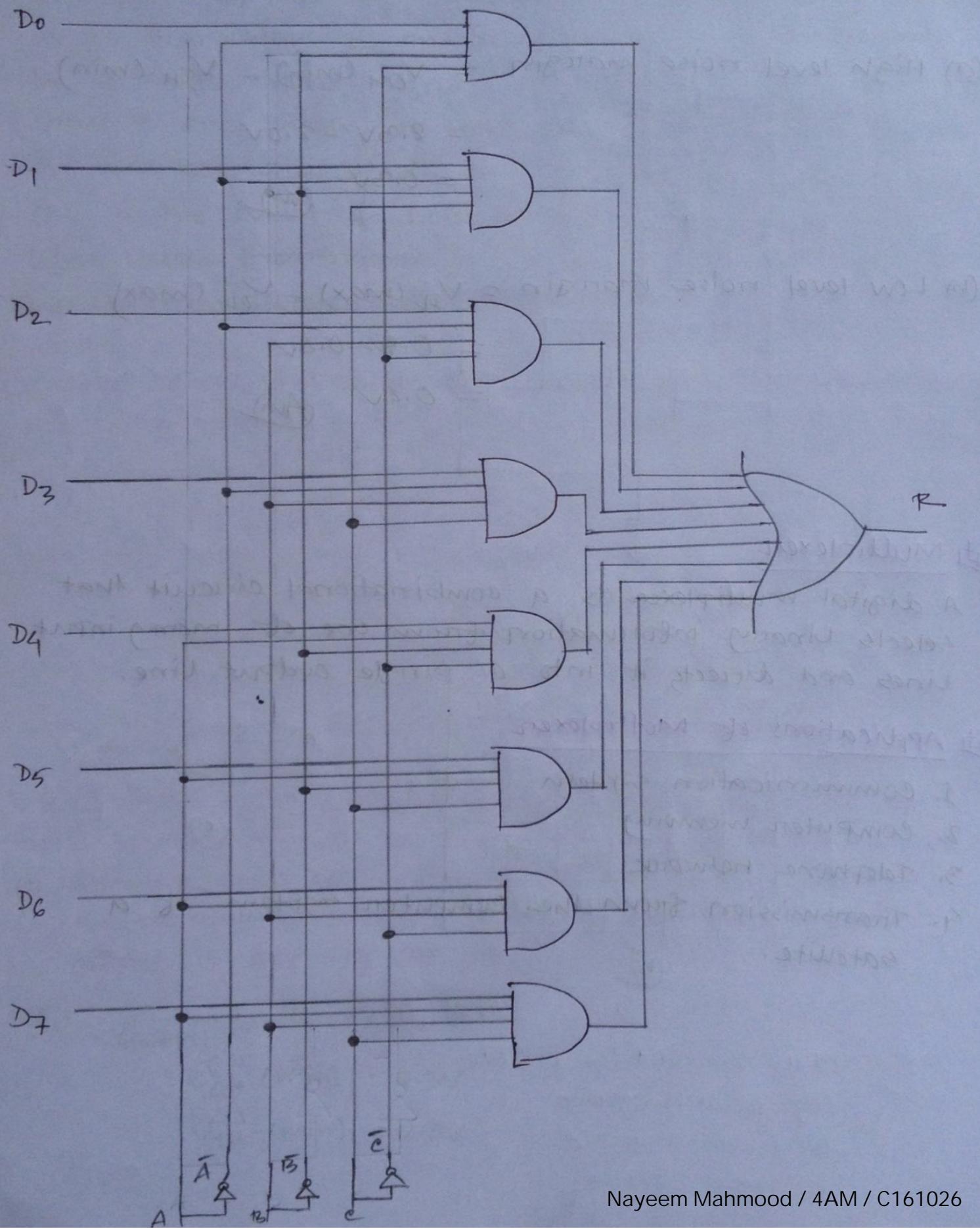
Multiplexer

A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it into a single output line.

Applications of Multiplexer

1. communication system
2. computer memory
3. telephone network
4. Transmission from the computer system of a satellite.

Logic circuitry of an 8-input MUX



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Draw the ckt diagram and describe the operation of a 4bit shift register.

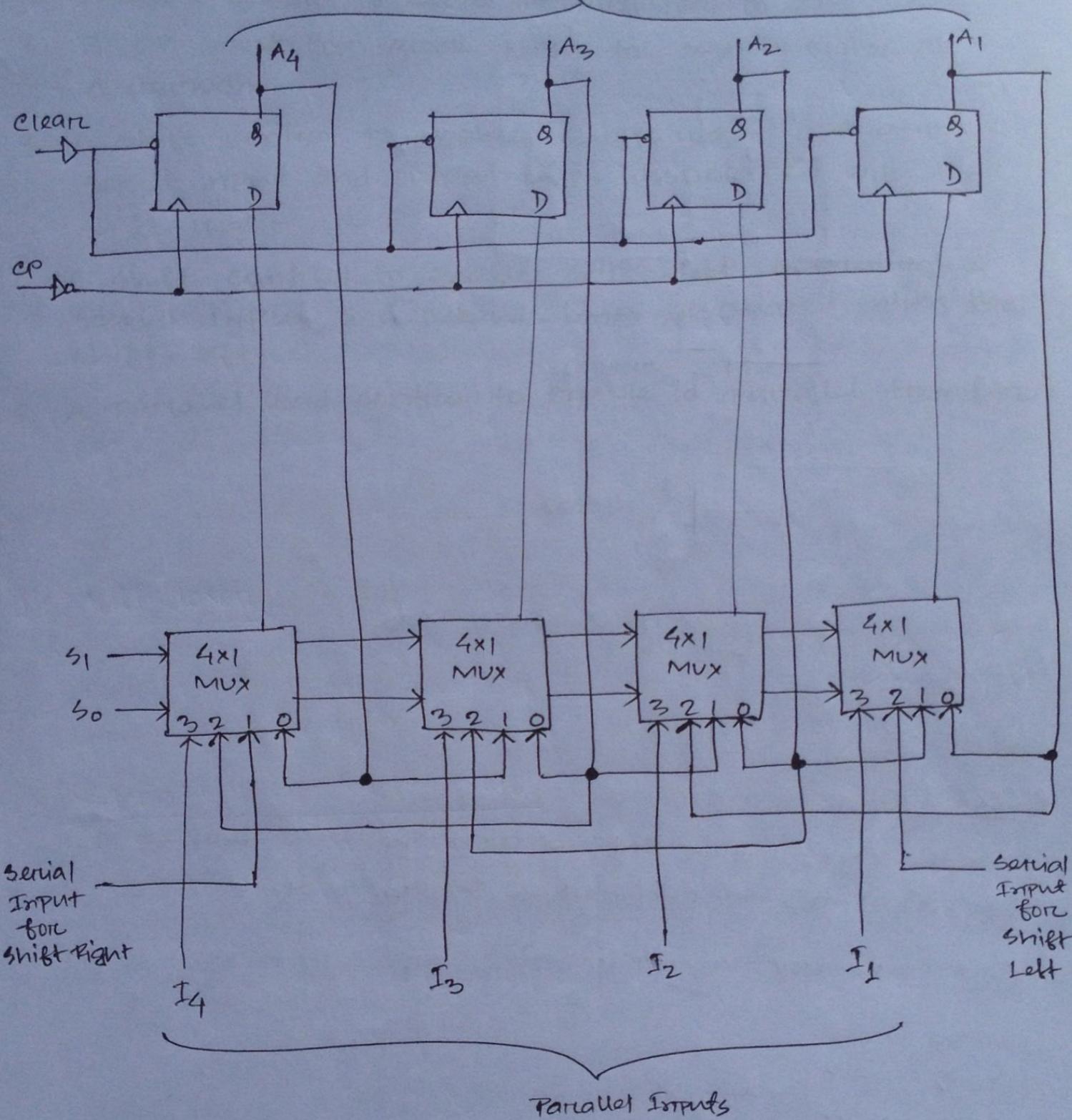


Fig: 4-bit Bidirectional shift Register with parallel load.

Operation:

1. A clear control to clear the register to 0.
2. A CP input for clock pulses to synchronize all operations.
3. A shift control to enable shift-right operation & serial input and output lines associated with the shift-right.
4. A shift control to enable shift-left operation & serial input and output lines associated with the shift-left.
5. A parallel load control to enable a parallel transfer.

CMOS NAND Gate

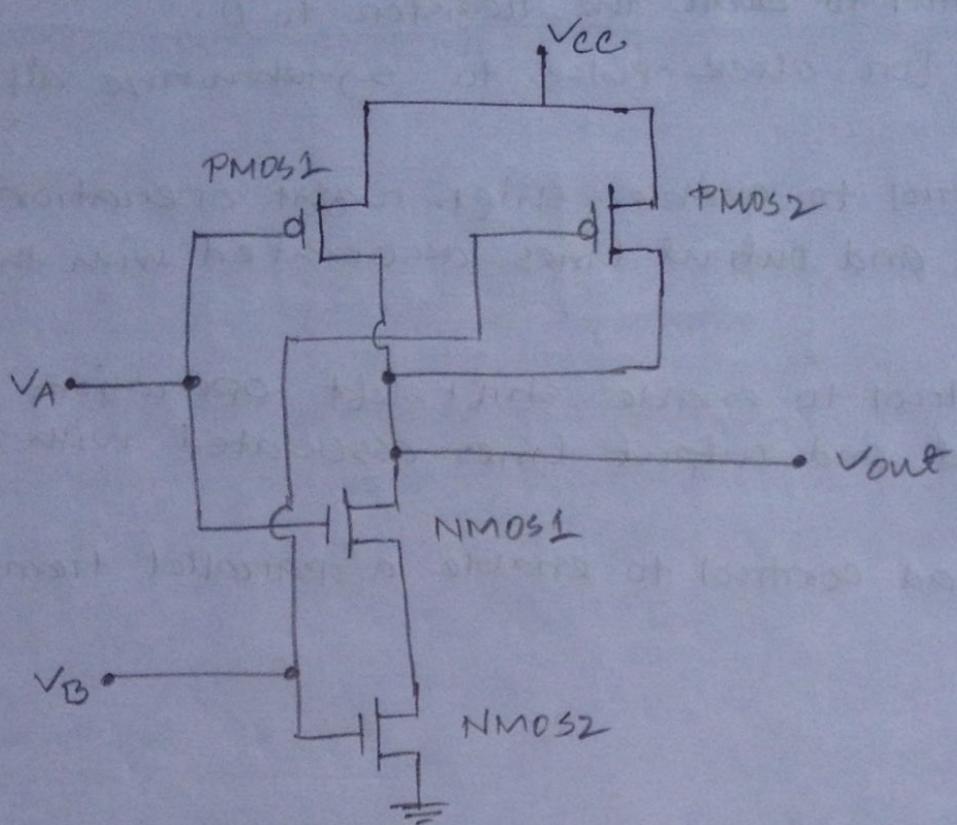


Fig: CMOS NAND Gate

Operation:

1) Case 1: V_A -Low, V_B -Low

Both the PMOS will be ON and both the NMOS will be OFF. The output will be charged to the V_{CC} level.

2) Case 2: V_A -Low, V_B -High

PMOS1 → ON

PMOS2 → OFF

NMOS1 → OFF

NMOS2 → ON

Though PMOS2 is OFF, still the output line gets a path through PMOS1 to get connected with Vcc because PMOS1 & PMOS2 are in parallel. NMOS1 & NMOS2 are in series. As NMOS1 is OFF, so Vout will not be able to find a path to GND to get discharged.

3) Case 3: VA - High, VB - Low

PMOS1 → OFF		PMOS2 → ON
NMOS1 → ON		NMOS2 → OFF

Similar as Case 2.

4) Case 4: VA - High, VB - High

PMOS1 → OFF
PMOS2 → OFF
NMOS1 → ON
NMOS2 → ON

In this case, Vout will not find any path to get connected with Vcc. As both NMOS are ON, Vout will find a path to GND and be discharged.

Integrated Circuit

An IC, sometimes called a chip or microchip, is a semi-conductor wafer on which thousands to millions of tiny resistors, capacitors and transistors are fabricated.

Different scale of Integration

1. SSI (Small Scale Integration) : It has less than 100 components (about 10 gates).
2. MSI (Medium Scale Integration) : It contains less than 500 components.
3. LSI (Large Scale Integration) : Number of components lies between 500 and 300000.
4. VLSI (Very Large Scale Integration) : It contains more than 300000 components per chip.
5. VVLSI (Very Very LSI) : It contains more than 1500000 components per chip.

Advantages of ICs

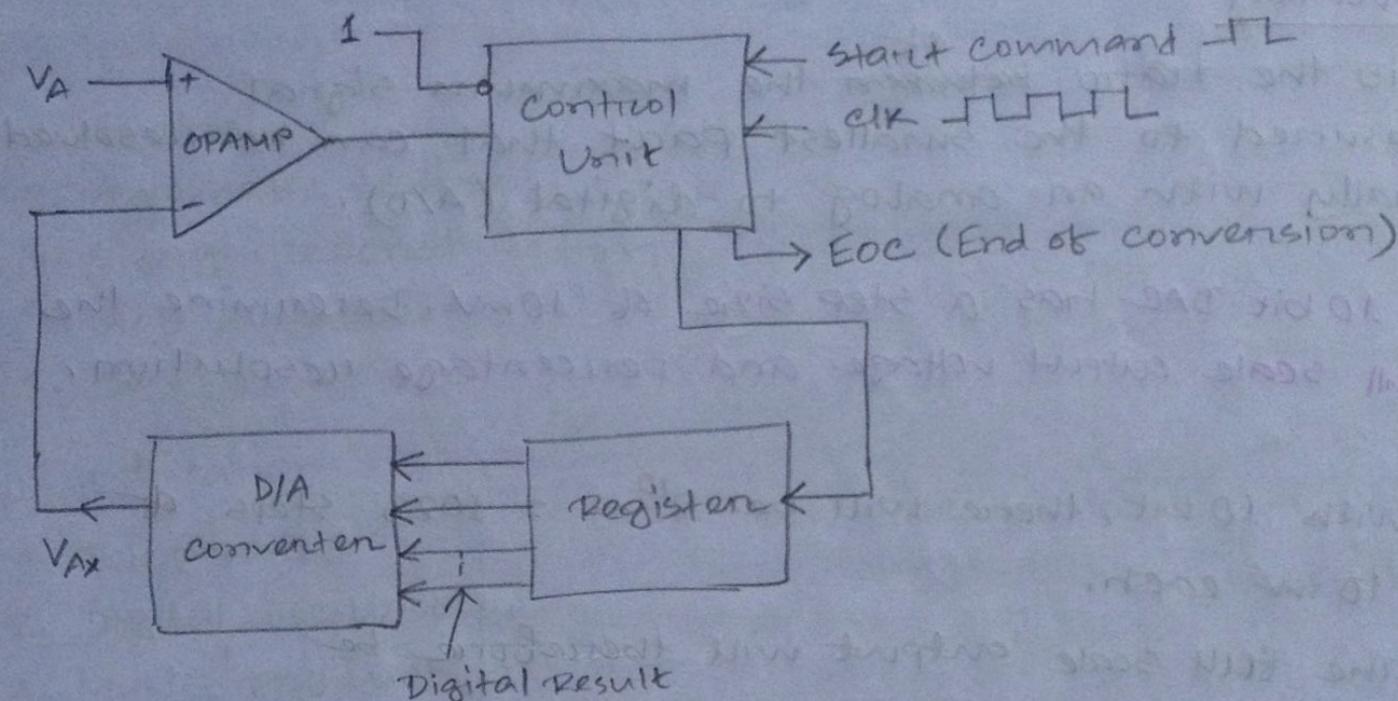
1. The entire physical size of IC is extremely small.
2. The mass of an IC is very light.
3. More reliable.
4. Lower power consumption.
5. Easy replacement.
6. Suitable for small signal operation.

Advantages of Digital Technology over Analogue

1. Digital technology can be simply reprogrammed for other applications ported to different hardware. Recomfiguration of an analogue technology usually implies a redesign of hardware.
2. Digital technology provides better control of accuracy.
3. Analog signals are not easily transportable.

4. In digital technology, more sophisticated signal processing algorithms can be implemented. It is difficult to perform precise mathematical operations in analog form.

Q) Draw the block diagram of an ADC and explain its operation.



Operation:

1. The start command pulse initiates the operation.
2. At a rate determined by the clock, the control unit continually modifies the binary number stored in the register.
3. The binary number in the register is converted to an analog voltage, V_{Ax} by the DAC.
4. The comparator compares V_{Ax} with the analog input V_A . As long as $V_{Ax} < V_A$, the comparator output stays high.

When V_{AX} exceeds V_A by at least an amount equal to V_T , the comparator output goes low and stops the process of modifying the number. At this point, V_{AX} is also approximation of V_A .

5. The control logic activates the EOC when the conversion is complete.

Resolution

It is the ratio of the maximum signal measured to the smallest part that can be resolved usually with an analog to digital (A/D).

A 10 bit DAC has a step size of 10mV. Determine the full scale output voltage and percentage resolution.

Soln:

With 10 bit, there will be $2^{10}-1 = 1023$ steps of 10mV each.

The full scale output will therefore be

$$10\text{mV} \times 1023 = 10.23\text{V}$$

$$\% \text{ resolution} = \frac{10\text{mV}}{10.23\text{V}} \times 100\% \\ = 0.1\%$$

Advantages of R/2R ladder in the design of DAC

1. The virtual ground is eliminated and the circuit is therefore easier to understand and troubleshoot.
2. It is much easier to analyze its operation.
3. It only uses two different resistor values.
4. It has fewer parts for the same number of inputs.

Applications of DAC

1. Control
2. Automatic testing
3. Signal reconstruction
4. A/D conversion
5. Serial DACs

Applications of ADC

1. Telephone
2. Digital oscilloscope
3. Music production
4. Scientific instruments
5. Digital signal processing

E1 Draw the logic diagram, graphic symbol and develop the truth table for JK flip-flop.

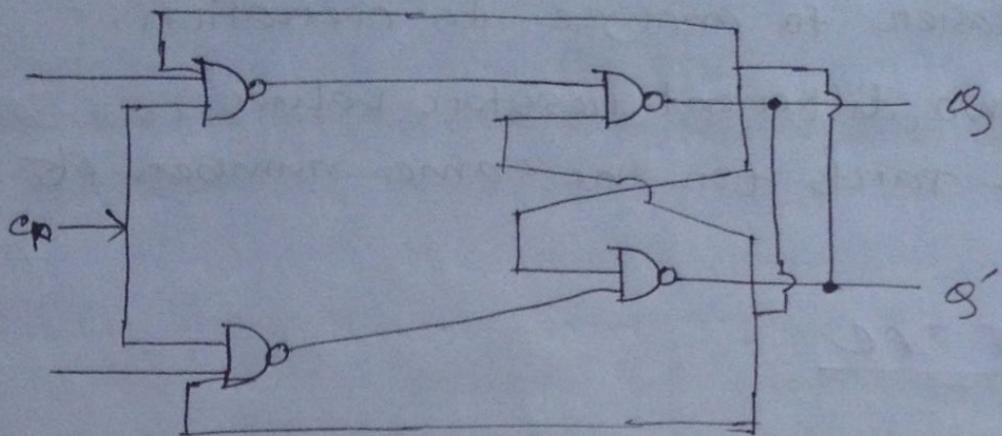


Fig: Logic diagram of JK FF

Truth Table:

Q	J	K	Q_{t+1}
0	0	0	0 (Memory)
0	0	1	0 (Reset)
0	1	0	1 (Set)
0	1	1	1 (Toggle)
1	0	0	1 (Memory)
1	0	1	0 (Reset)
1	1	0	1 (Set)
1	1	1	0 (Toggle)

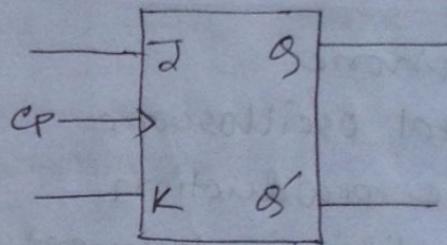
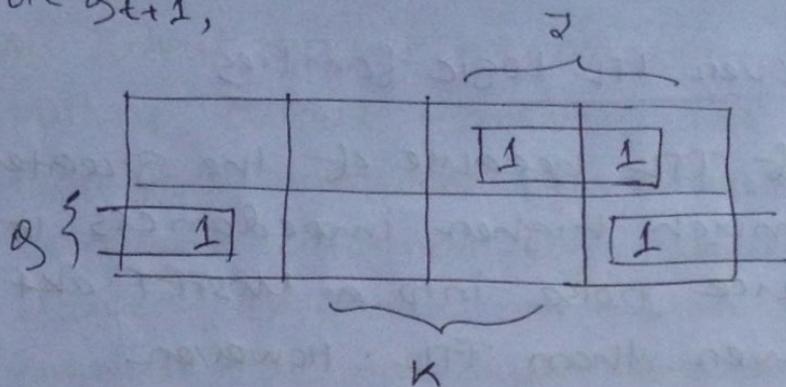


Fig: Graphical symbol of JK FF

Characteristics Eqn of JK FF

For S_{t+1} ,



$$\therefore S_{t+1} = JS' + KS$$

Noise Immunity

Circuit noise immunity is the ability of a device or component to operate in the presence of noise disturbance. For good noise immunity, the signal swing (i.e. the difference between V_{OL} and V_{OH}) and the noise margin have to be large enough to overpower the impact of fixed sources of noise. To the circuit, this is a rapid high voltage, low current situation.

High Level Noise Margin, $V_{NLH} = V_{OH}(\text{min}) - V_{IH}(\text{min})$

Low Level Noise Margin, $V_{NLL} = V_{IL}(\text{max}) - V_{OL}(\text{max})$

Propagation Delay

In digital electronics, the propagation delay or gate delay is the length of time which starts when the input to a logic gate becomes stable & valid to change, to the time that the output of that logic gate is stable and valid to change. Propagation delay is caused by:

1. Electron speed in the medium
2. Capacitance.

Advantages of MOSFET over TTL logic families

MOSFET is used instead of TTL because of the greater noise immunity. Due to much higher impedances, it is much easier to induce noise into a MOSFET ckt. MOSFET consumes less power than TTL. However, MOSFETs are slower than TTLs.

Rising Time

It refers to the time it takes for the leading edge of a pulse (voltage or current) to rise from its minimum to its maximum value. Rising time is typically measured from 10% to 90% of the value.

Falling Time

It is the measurement of time it takes for the pulse to move from the highest value to the lowest.

Pulse width

It is a modulation process or technique used in most communication system for encoding the amplitude of a signal right into a pulse width or duration of another signal, usually a carrier signal for transmission.

Q1 Why is a diode used between the two transistors in totem-pole output configuration?

An output circuit having the output taken between a pull-up output transistor and a pull-down output transistor connected in series for conducting current alternatively. Separate pull-up and pull-down driver ckt's are controlled by a common input signal. The pull-down driver ckt is supplied by a pull-down current source, and a diode is connected from the point between the pull-down driver transistor and pull-down current source to the output node. The effect of a large node capacitance is reduced by the diode, which conducts current from the pull-down current source to any output load capacitance to raise the output voltage more rapidly when the pull-down driver ckt is cut off.

That's why a diode is used between the two transistors in totem-pole output configuration.

Q2 Draw the logic diagram of a positive-edge clocked SR FF. Also draw its response at Q.

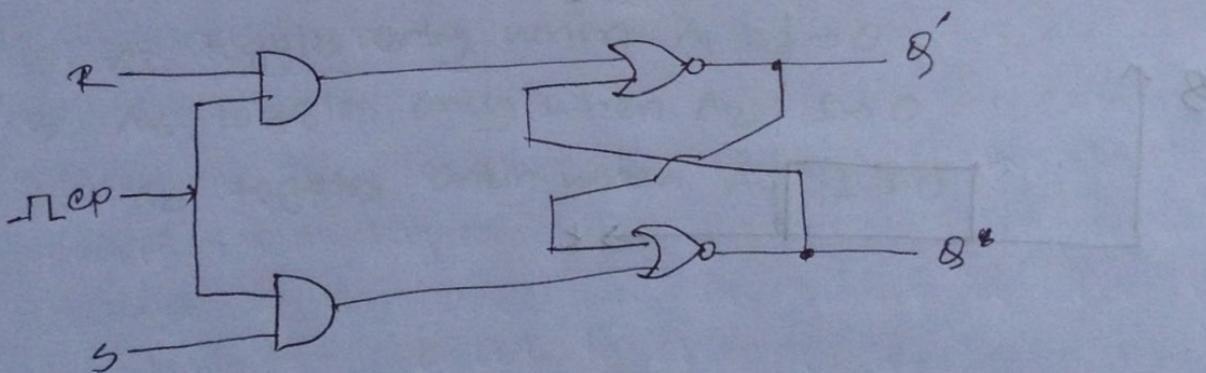


Fig: Logic Diagram of SR FF

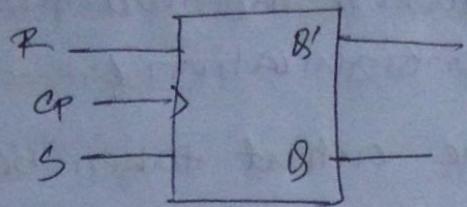
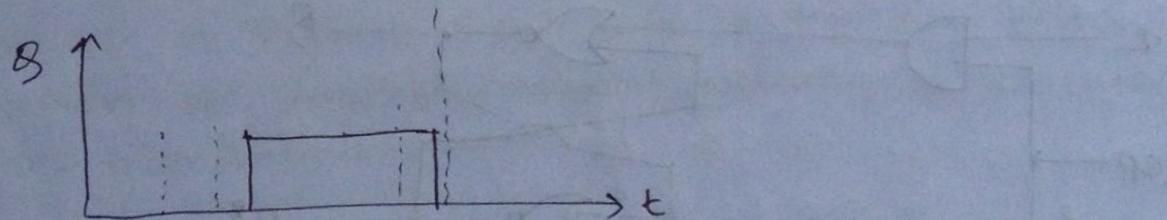
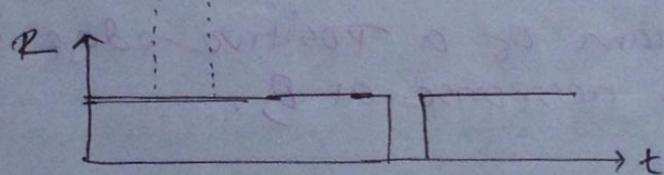
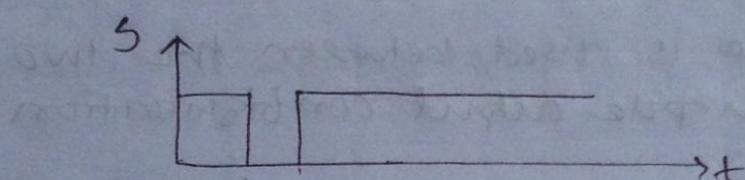
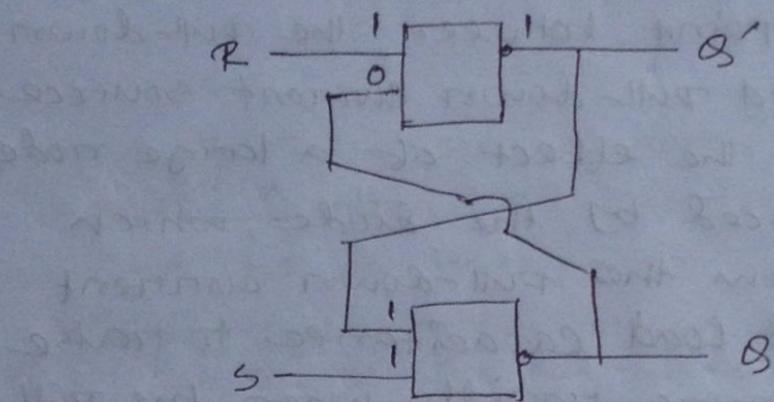


Fig: Graphical Symbol

Response at Q



Explain the operation of a 4-bit ripple counter.

Count sequence for a 4-bit binary ripple counter with
JK FF:

A_4	A_3	A_2	A_1	
0	0	0	0) complement A_1
0	0	0	1) complement A_1 , if $A_1 : 1 \rightarrow 0$, then
0	0	1	0	$A_2 : 0 \rightarrow 1$
0	0	1	1) complement A_1
0	1	0	0) complement A_1 , if $A_1 : 1 \rightarrow 0$, then
0	1	0	1	$A_2 : 1 \rightarrow 0$, then
0	1	1	0	A_3 complement
0	1	1	1	
1	0	0	0	$A_2 : 1 \rightarrow 0$, A_3 complement and
1	0	0	1	$A_3 : 1 \rightarrow 0$, A_4 complement

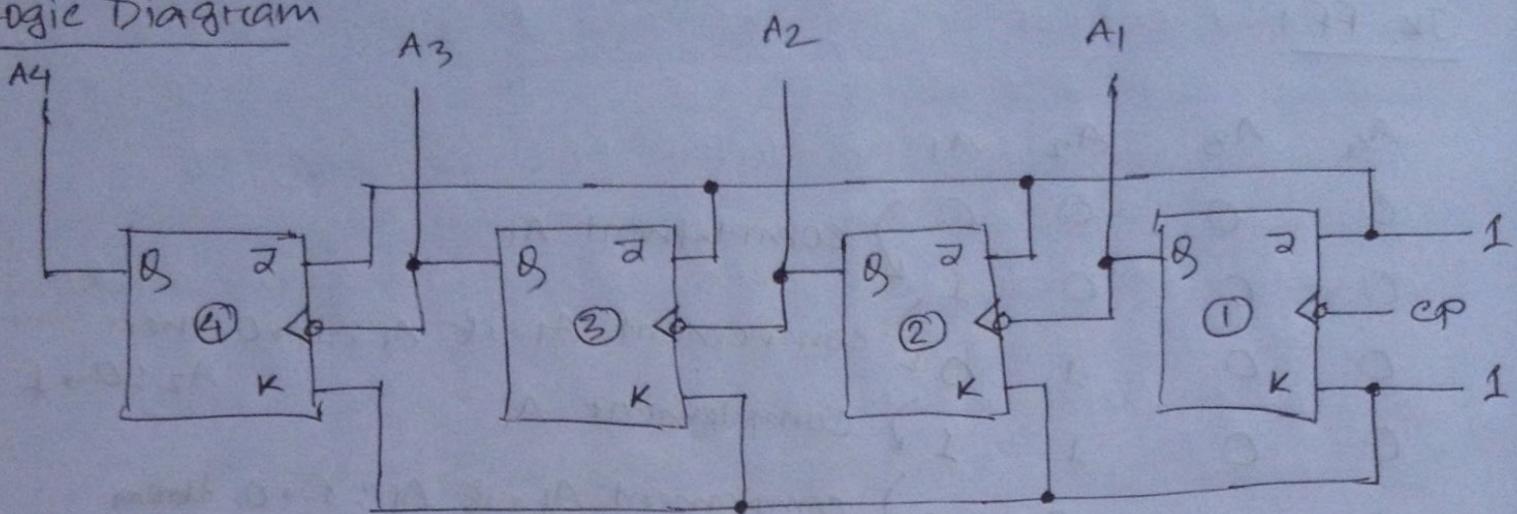
and so on..

From the count sequence, we can say,

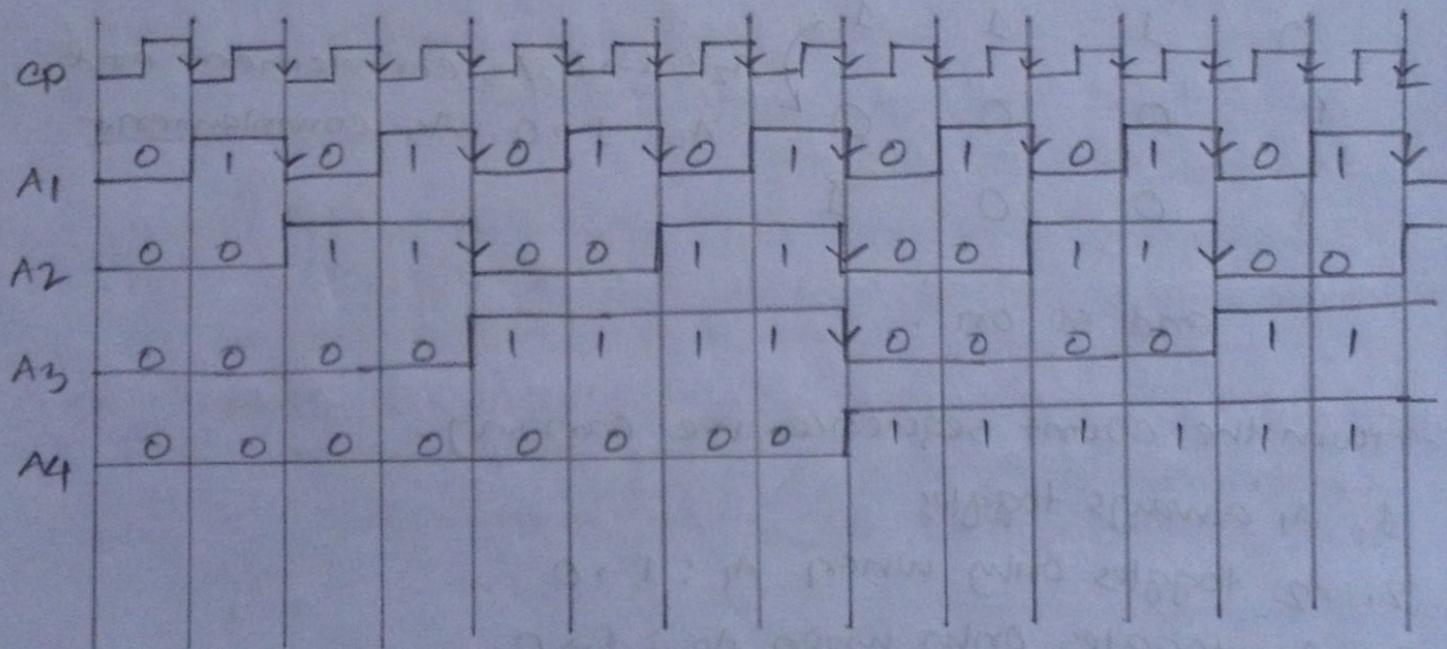
1. A_1 always toggles
2. A_2 toggles only when $A_1 : 1 \rightarrow 0$
3. A_3 toggles only when $A_2 : 1 \rightarrow 0$
4. A_4 toggles only when $A_3 : 1 \rightarrow 0$

So we have to trigger A_3, A_2, A_1 at negative edges of previous bits.

Logic Diagram



Timing Diagram



Q1 Implement the following function with an 8×1 MUX.

$$F(A, B, C, D) = \sum (0, 2, 4, 7, 9, 10, 13, 14, 15)$$

Truth Table:

A - B - C - D - Min Terms - F

0 0 0 0 - 0 - 1

0 0 0 1 - 1 - 0

0 0 1 0 - 2 - 1

0 0 1 1 - 3 - 0

0 1 0 0 - 4 - 1

0 1 0 1 - 5 - 0

0 1 1 0 - 6 - 0

0 1 1 1 - 7 - 1

1 0 0 0 - 8 - 1

1 0 0 1 - 9 - 1

1 0 1 0 - 10 - 1

1 0 1 1 - 11 - 0

1 1 0 0 - 12 - 0

1 1 0 1 - 13 - 1

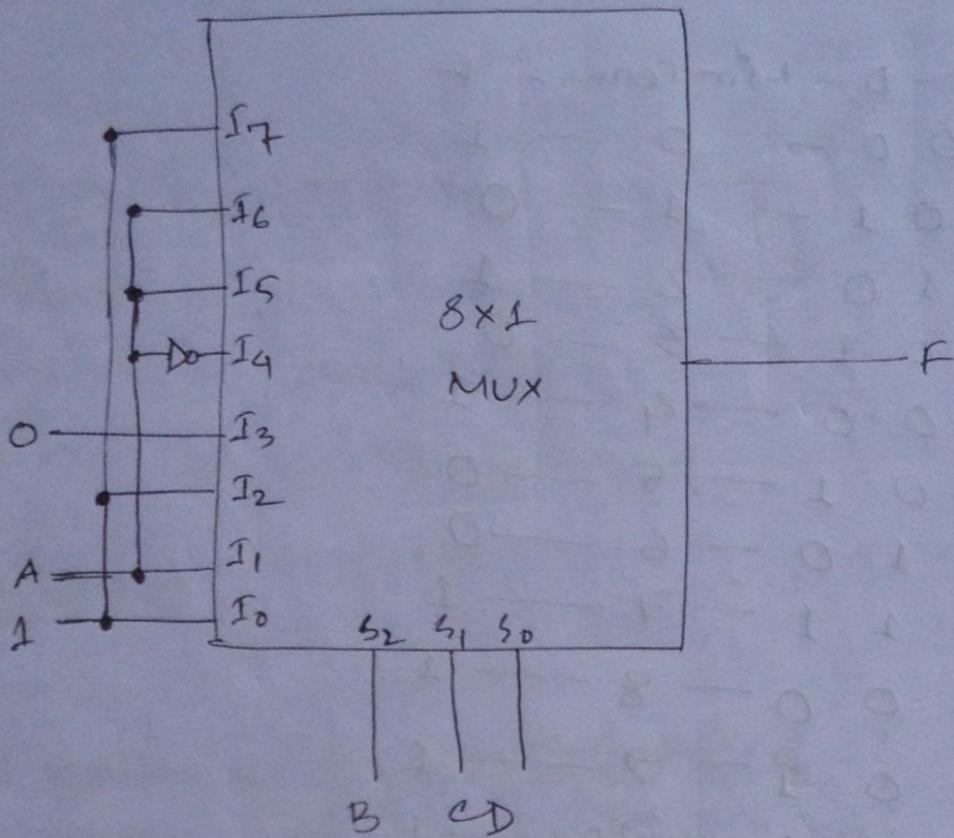
1 1 1 0 - 14 - 1

1 1 1 1 - 15 - 1

Implementation Table:

	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇
A'	⑥	1	②	3	④	5	6	⑦
A	⑧	⑨	⑩	11	12	⑬	⑭	⑮

MUX Implementation



Resolution of a DAC

It is defined as the smallest change that can occur in the analog output as a result of change in the digital input.

It indicates the amount of V_{out} will change from one step to the next.

For N-bits DAC, the number of levels = 2^N
number of steps = $2^N - 1$

$$\therefore \text{Resolution} = K = \frac{A_{fs}}{2^N - 1}; A_{fs} = \text{Analog Full scale output}$$

Q An 8-bit DAC produces 1.0V for an input 00110010. Find its resolution.

Here,

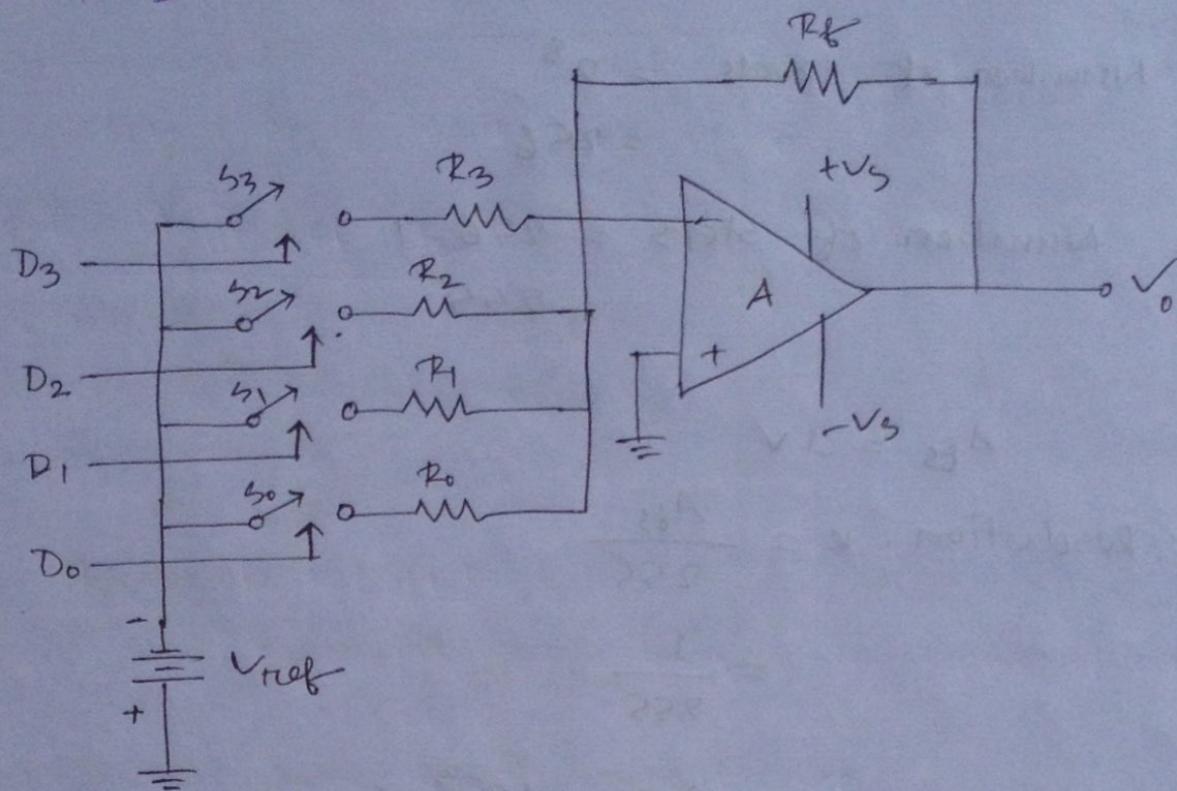
$$\text{Number of levels} = 2^8 \\ = 256$$

$$\text{Number of steps} = 256 - 1 \\ = 255$$

$$A_{fs} = 1V$$

$$\therefore \text{Resolution, } R = \frac{A_{fs}}{255} \\ = \frac{1}{255} \\ = 3.92 \times 10^{-3} V \quad (\text{Ans})$$

Explain the operation of a 4-bit DAC using OP-AMP summing amplifier with binary-weighted resistors.



(Required Figure)

The circuit consists of transistor switches (shown by the upward arrows) which turn on the switch when the digital input is "1" and if digital input becomes "0", it will open the switch. When switch gets closed, current flows through the weighted resistors due to the reference voltage as shown in ckt diagram.

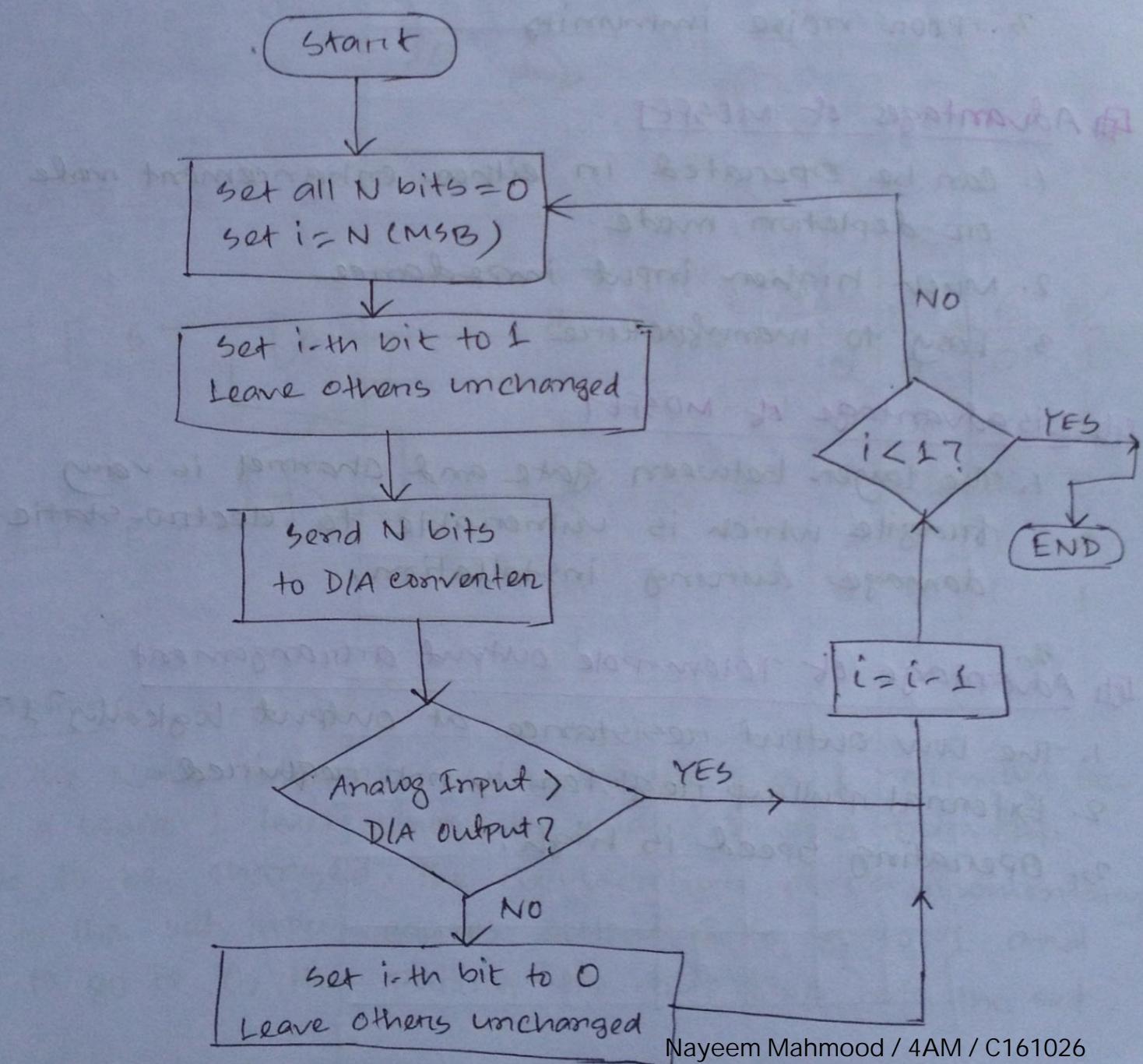
When all such currents from different weighted resistors get added at summing point of the OPAMP, it will produce a proportional voltage to its input.

For a 4-bit DAC, the output V_o is

$$V_o = -V_{ref} \left(S_3 \times \frac{R_f}{R_3} + S_2 \times \frac{R_f}{R_2} + S_1 \times \frac{R_f}{R_1} + S_0 \times \frac{R_f}{R_0} \right)$$

where S_3, S_2, S_1, S_0 represent the status of the switches i.e. ON(1) or OFF(0).

Operational flow chart of successive approximation ADC.



Nayeem Mahmood / 4AM / C161026

Advantages of TTL

1. Fast
2. Less propagation delay
3. Power dissipation is not dependent on frequency
4. Latch ups do not take place.

Disadvantages of TTL

1. Much power dissipation
2. Less component density
3. Poor noise immunity

Advantages of MOSFET

1. Can be operated in either enhancement mode or depletion mode.
2. Much higher input impedance
3. Easy to manufacture

Disadvantage of MOSFET

1. The layer between gate and channel is very fragile which is vulnerable to electro-static damage during installation.

Advantage of Totem-pole output arrangement

1. The low output resistance at output logically "1".
2. External pull-up register is not required.
3. Operating speed is high.

E For standard TTL logic family, $I_{OH} = 400\text{mA}$ and $I_{IH} = 40\text{mA}$. Find fan-out.

Solⁿ: Given,

$$I_{OH} = 400\text{mA}$$

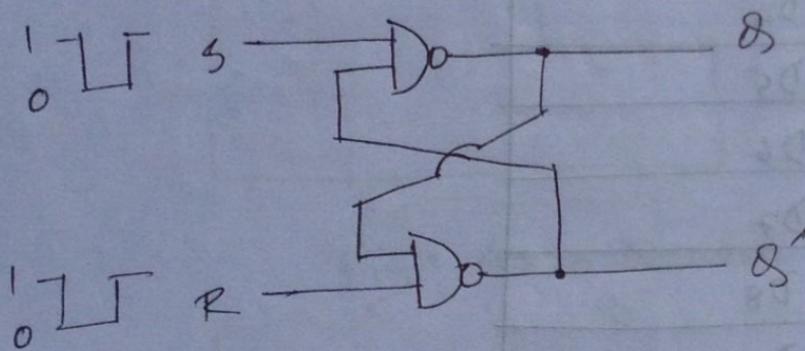
$$I_{IH} = 40\text{mA}$$

$$\text{fan-out} = \frac{I_{OH}}{I_{IH}}$$

$$= \frac{400\text{mA}}{40\text{mA}}$$

$$= 10 \quad (\text{Ans})$$

NAND gate Latch



S	R	Q	Q'
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	0
0	0	1	1

Operation:

For the NAND latch ckt, both inputs should normally be at a logic 1 level. Unless the state of the flip-flop has to be changed. The application of a momentary 0 to the set input causes output Q to go to 1 and Q' to go to 0, thus putting the flip-flop into the set

State. After the set input returns to 1, a momentary 0 to the reset input causes a transition to the clear state. When both inputs go to 0, both outputs go to 1, a condition which is avoided in normal flip-flop operation.

E Design a 4×16 decoder with the 3×8 decoders with enable inputs.

Input				Output
E	A	B	C	
0	0	0	0	D ₀
0	0	0	1	D ₁
0	0	1	0	D ₂
0	0	1	1	D ₃
0	1	0	0	D ₄
0	1	0	1	D ₅
0	1	1	0	D ₆
0	1	1	1	D ₇
1	0	0	0	D ₈
1	0	0	1	D ₉
1	0	1	0	D ₁₀
1	0	1	1	D ₁₁
1	1	0	0	D ₁₂
1	1	0	1	D ₁₃
1	1	1	0	D ₁₄
1	1	1	1	D ₁₅

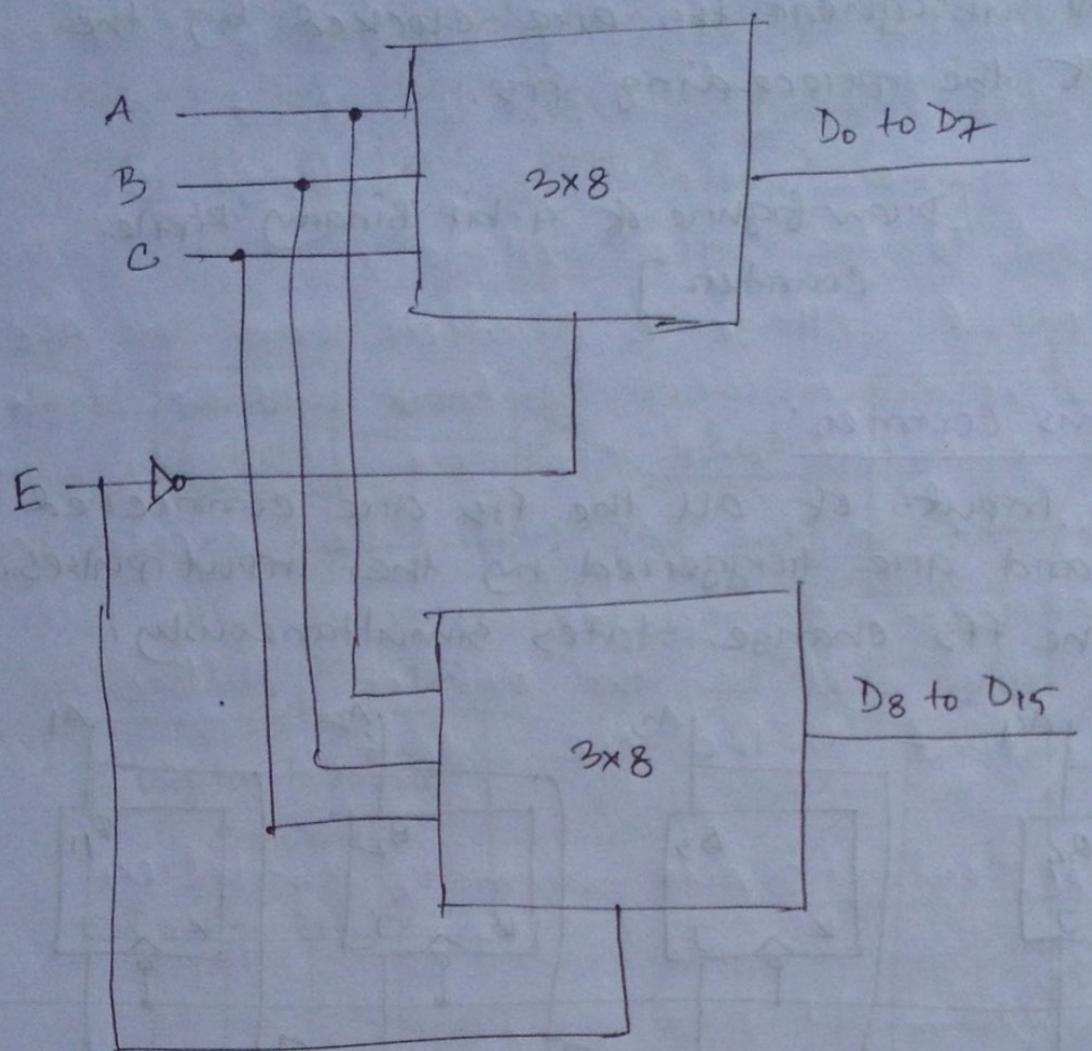


Fig: 4x16 Decoder using 2 3x8 decoders.

MOD Number

The number of states of counting sequences through which a particular counter advances before returning once again back to its original first state is called the MOD number.

The MOD number of a counter consisted of 4 FFs is MOD-10.

Asynchronous / Ripple counter

Hence only the first FF is clocked by an external clock. All subsequent FFs are clocked by the output of the preceding FFs.

Example:

[Draw figure of 4-bit Binary Ripple counter]

Synchronous counter:

The clock inputs of all the FFs are connected together and are triggered by the input pulses. Thus all the FFs change states simultaneously.

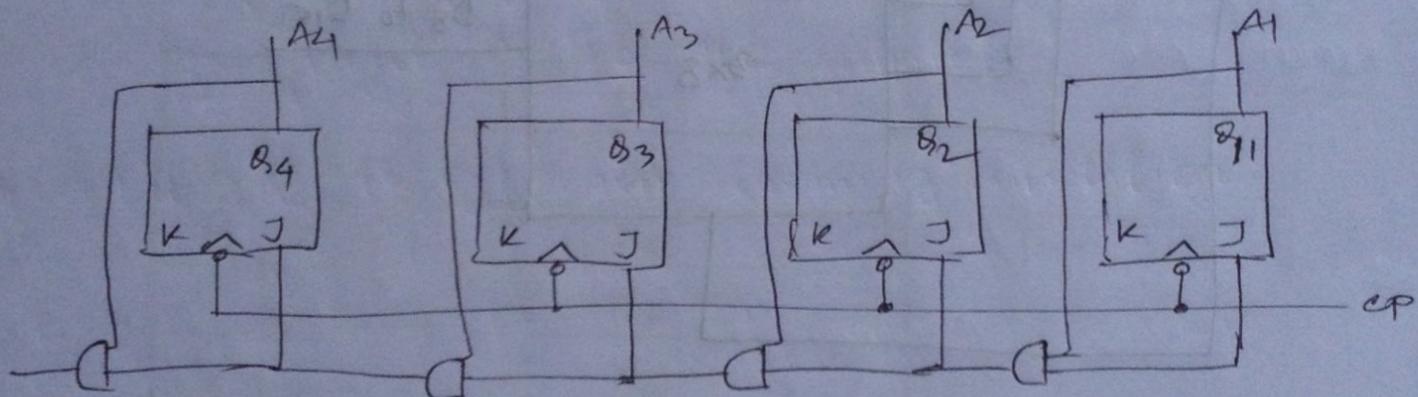


Fig: Synchronous Binary counter.

Digital ramp ADC

The digital ramp ADC is also known as a counter-type ADC. It uses a binary counter as the register and allows the clock to increment the counter one step at a time until $V_o > V_t$.

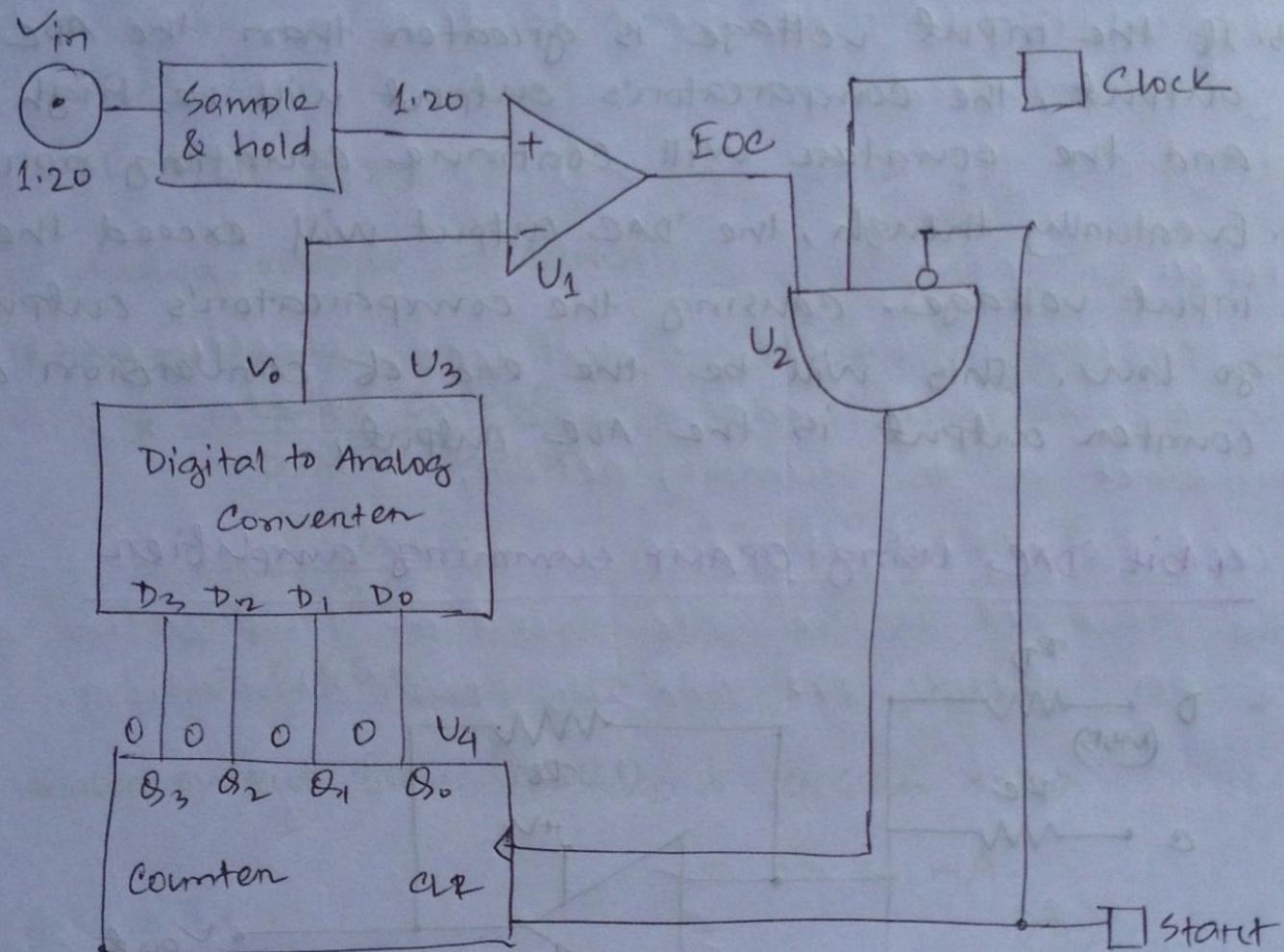
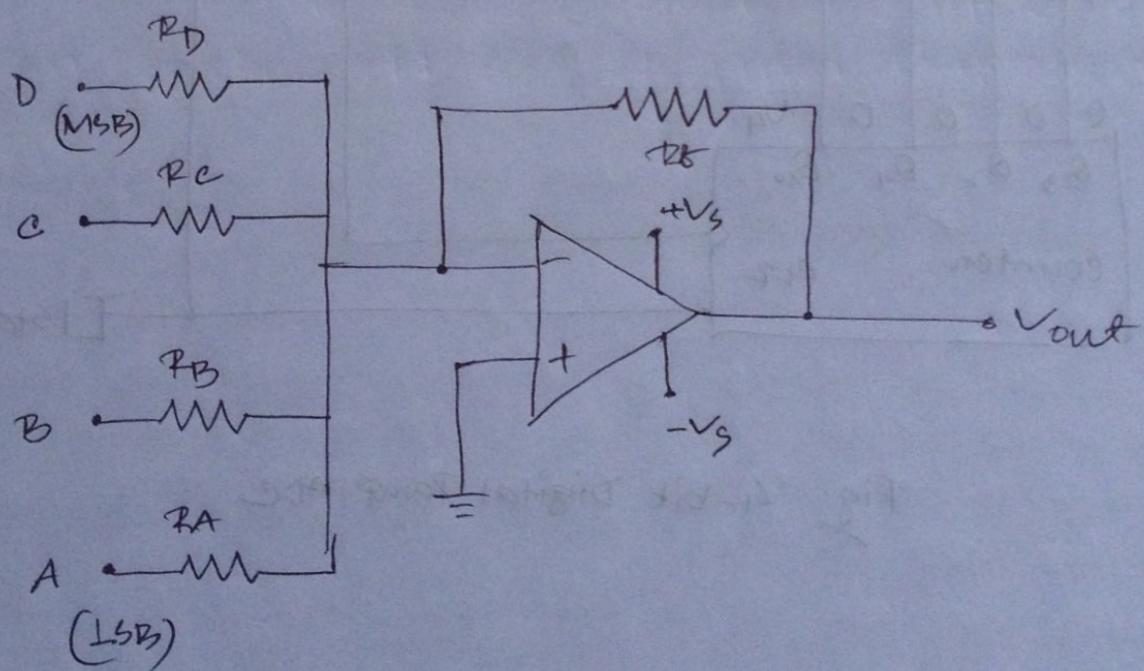


Fig: 4-bit Digital Ramp ADC

Operation:

1. At the start, the counter is cleared to 0.
2. As the counter counts up with each clock pulse, the digital analog converter outputs a slightly higher voltage. This voltage is compared to the input voltage.
3. If the input voltage is greater than the ADC output, the comparator's output will be high and the counter will continue counting normally.
4. Eventually though, the DAC output will exceed the input voltage, causing the comparator's output to go low. This will be the end of conversion and counter output is the ADC output.

4 bit DAC Using OPAMP summing amplifier



$$V_{out} = - \left(\frac{R_f}{R_D} \times V_D + \frac{R_f}{R_C} \times V_C + \frac{R_f}{R_B} \times V_B + \frac{R_f}{R_A} \times V_A \right)$$

A DAC has a current output of 10mA for an input 10101. Determine the output for the digital input 11101.

Sol:

$$(10101)_2 = 21$$

$$(11101)_2 = 29$$

$$\text{Analog output} = 10\text{mA}$$

We know,

$$k = \frac{\text{Analog Output}}{\text{Digital input}}$$

$$= \frac{10\text{m}}{21}$$

$$= 0.48\text{m}$$

$$\text{So, Analog output for } (11101)_2 = 0.48\text{m} \times 29$$

$$= 13.81\text{ mA.}$$

(Ans).

Fan-in:

It is a term that defines the maximum number of digital inputs that a single logic gate can accept. Most TTL have 1 or 2 fan-in.

Fan-out:

It is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.

A typical TTL gate has a fan out of 10.

Power Dissipation

The process in which an electric or electronic device produces heat as an unwanted by product of its primary action.

Speed Power Product

The product of the gate speed or propagation delay of an electric ckt and its power dissipation.