

Autumn-2022

Ans to the Question no:01 (a)

SR to T flip flop conversion:

Available Flip Flop = SR FF

Required FF = T FF

Characteristic table of T FF:

| Q_n | T | Q_{n+1} | S | R |
|-------|---|-----------|---|---|
| 0 | 0 | 0 | 0 | X |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | X | 0 |
| 1 | 1 | 0 | 0 | 1 |

Excitation table:

| Q_n | Q_{n+1} | S | R |
|-------|-----------|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | X | 0 |

S

T

| Q_n | 0 | 1 |
|-------|---|---|
| 0 | 0 | 1 |
| 1 | X | 0 |

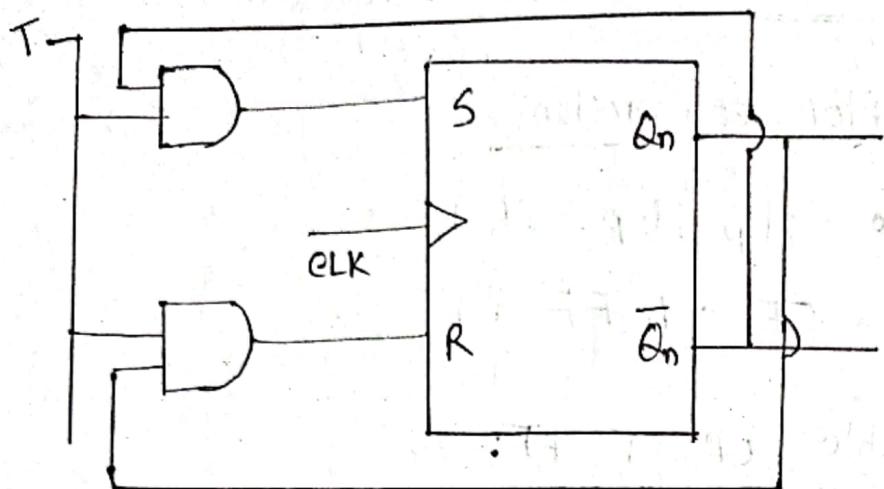
$$S = T \bar{Q}_n$$

R

T

| Q_n | 0 | 1 |
|-------|---|---|
| 0 | X | 0 |
| 1 | 0 | 1 |

$$R = T Q_n$$



JK to SR, T to SR and D to SR FF:

When $S=1$ and $R=1$ then $Q_{n+1} = \text{Invalid}$

But for $\neg J$, T , and D , $Q_{n+1} = \text{It}$ will never go in invalid state.

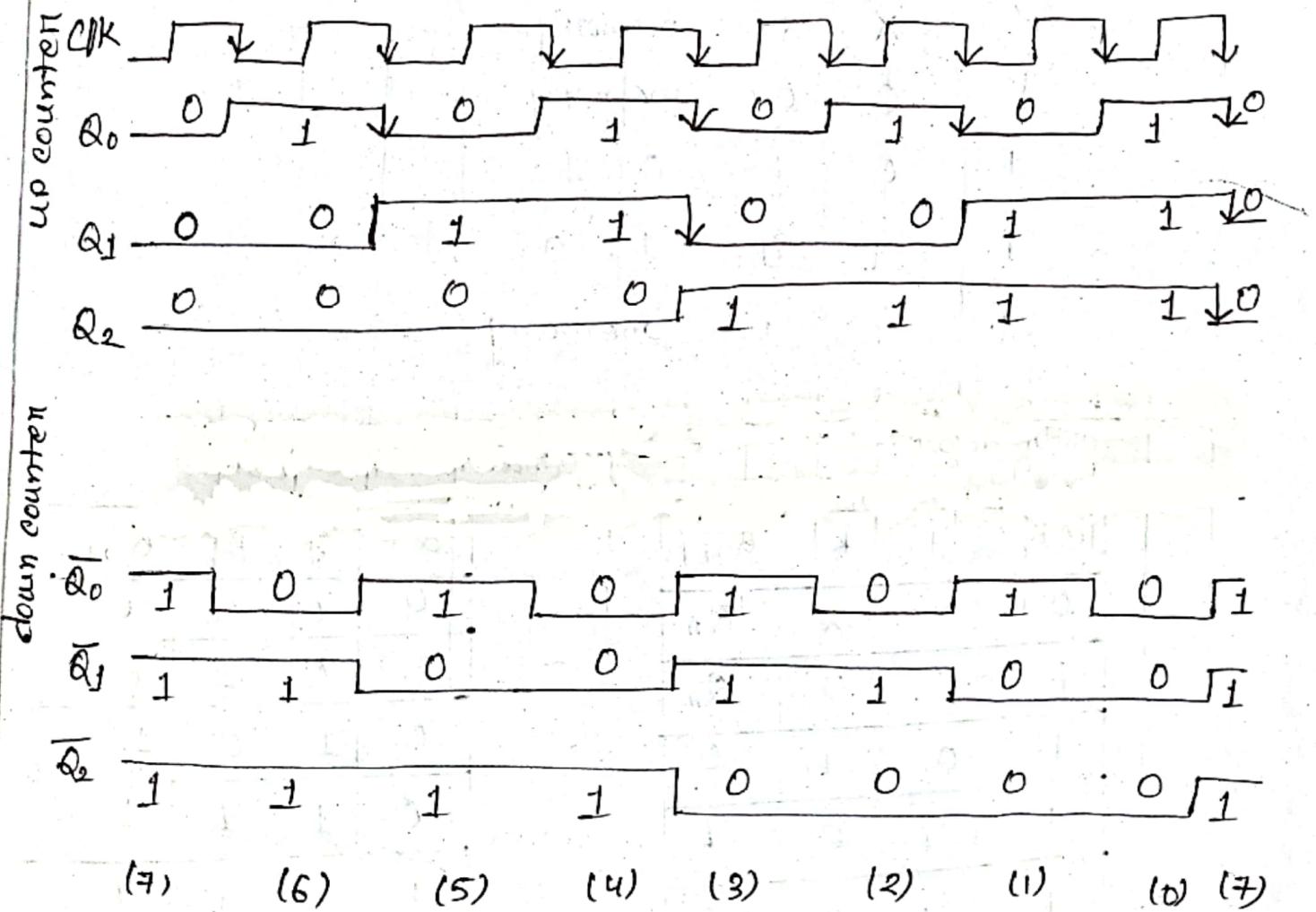
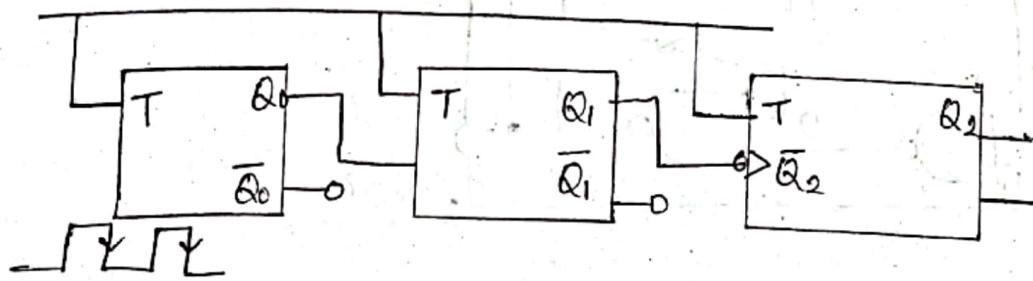
So we cannot form JK to SR, T to SR and D to SR Flip Flop.

Difference between latch and flip-flop:

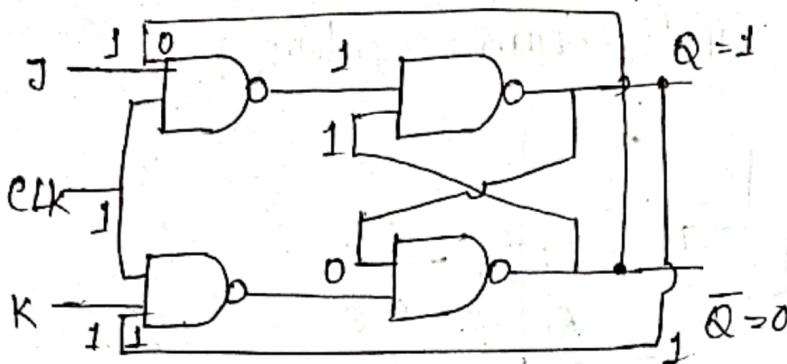
| Latch | Flip Flop |
|----------------------------------|----------------------------------|
| ① Made by logic gates only. | ① Made by logic gates and latch. |
| ② It is level trigger. | ② It is edge trigger. |
| ③ It cannot be used as register. | ③ It can be used as register. |
| ④ It is faster. | ④ It is slower. |
| ⑤ It requires less power. | ⑤ It requires more power. |

Ans to the Question no: Q1 (a)-OR

Asynchronous Ripple-down counter:



Ans to the Question no: 1(b)



| CLK | J | K | Q | \bar{Q} |
|-----|---|---|---|-----------|
| 0 | x | x | | memory |
| 1 | 0 | 0 | | memory |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | | memory |

Truth table -

Characteristic table

| CLK | J | K | Q_{n+1} |
|-----|---|---|-----------|
| 0 | x | x | Q_n |
| 1 | 0 | 0 | Q_n |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | Q_n |

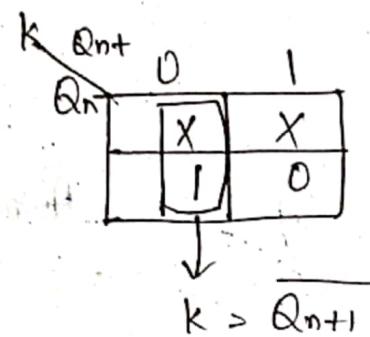
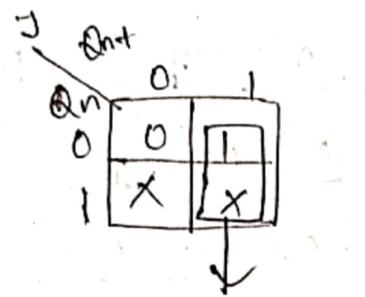
| Q_n | JK | 00 | 01 | 11 | 10 |
|-------|----|----|----|----|----|
| 0 | | 0 | 0 | 1 | 1 |
| 1 | | 1 | 0 | 0 | 1 |

$$Q_{n+1} = \bar{Q}_n J + Q_n K$$

| Q_n | J | K | Q_{n+1} |
|-------|---|---|-----------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Excitation table -

| Q_n | Q_{n+1} | J | K |
|-------|-----------|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |



Ans to the Question no: 02 (a)

Module counter by Asynchronous counter:

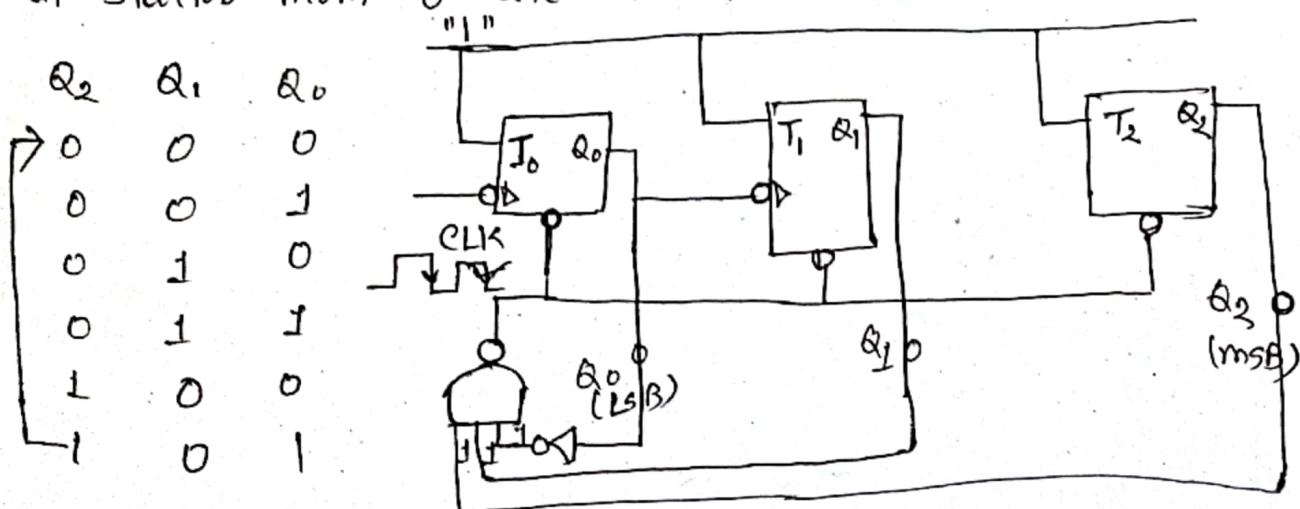
By 2 bits counter, At max we can have mod 4 counter.

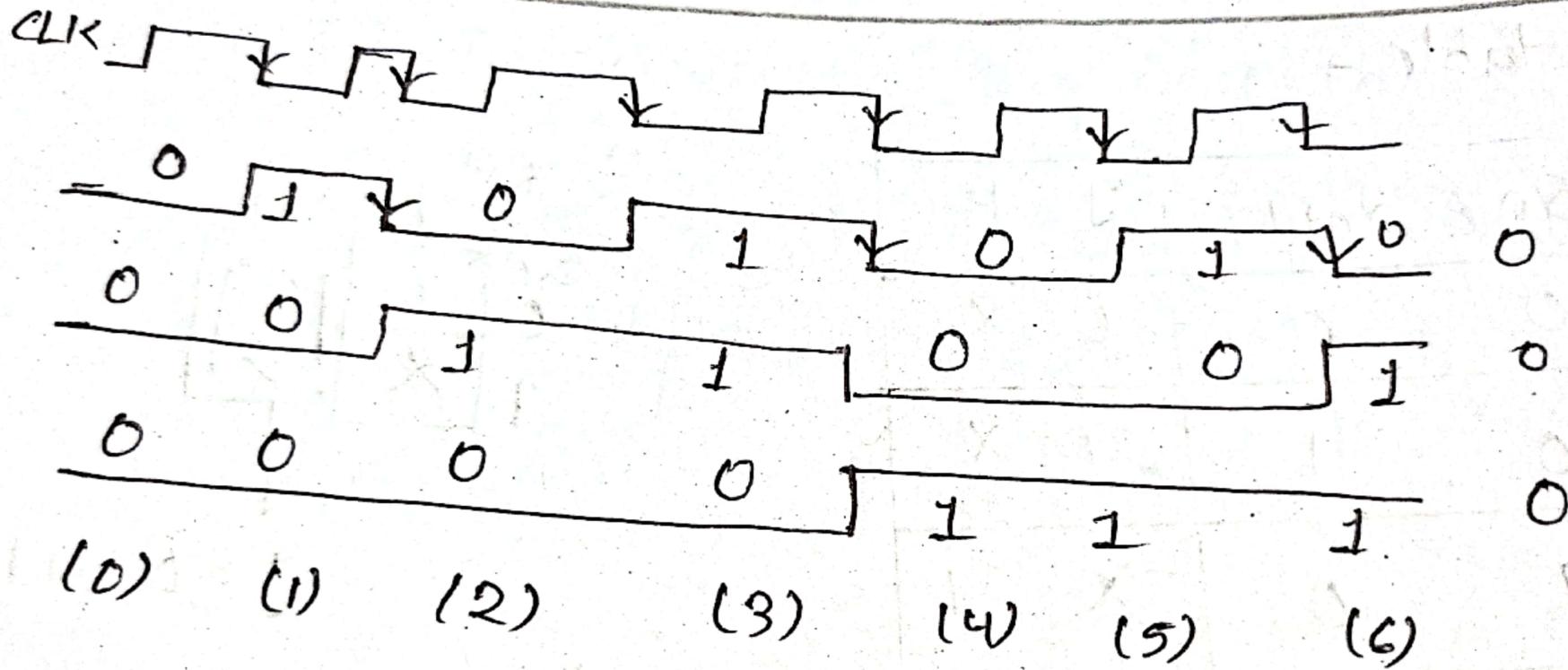
By 3 bit counter , At max we can have mod 8 counter.

By 4 bit counter, At max we can have mod 16 counter.

Eg modulo 6 counter

It starts from 0. and it will count up to 5

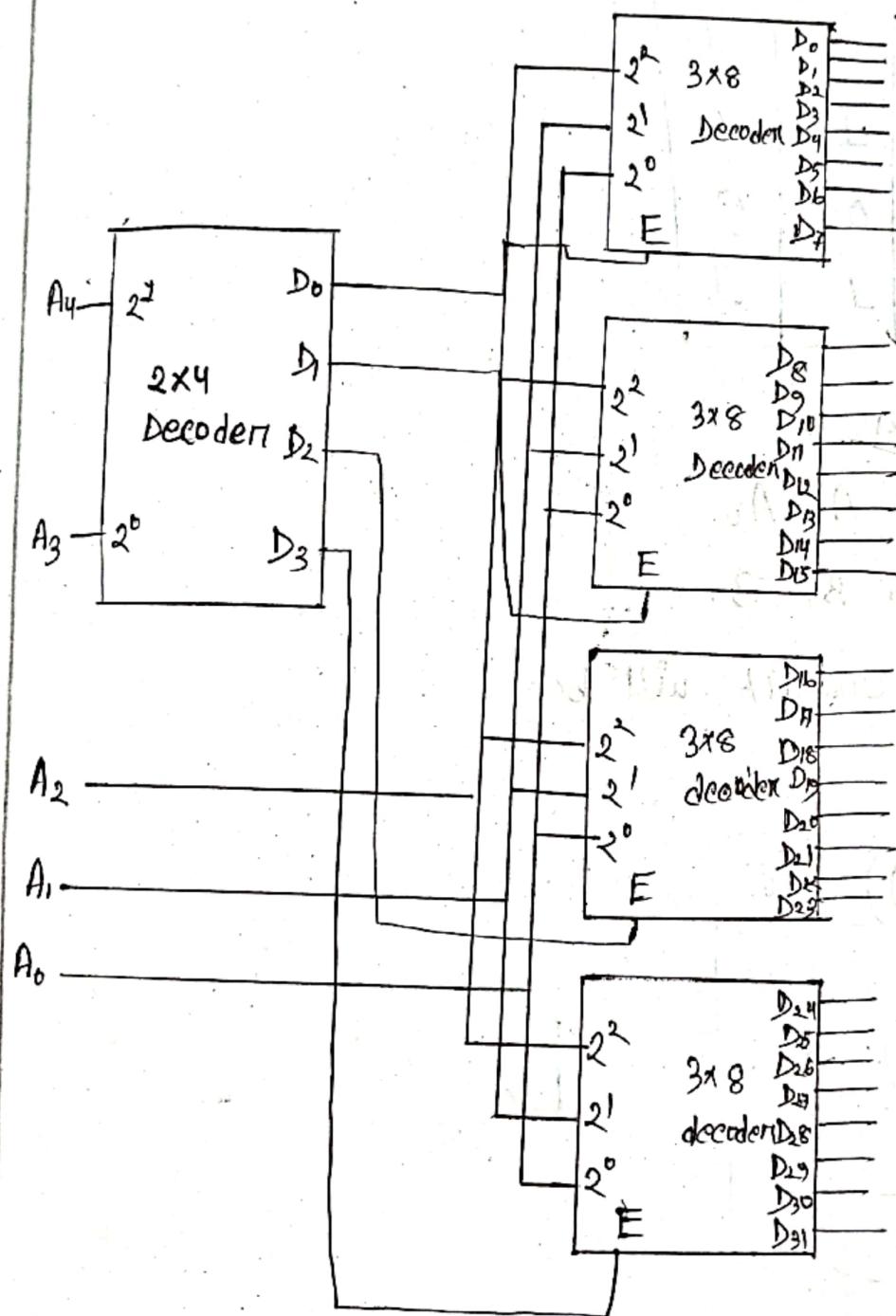




Ans to the Question no: 02(b)

5x32 decoder with four 3x8 decoders and a 2x4 decoder.

Input: A₄ A₃ A₂ A₁ A₀



Ans to the Question no: 02(b) OR

Suppose the two numbers are A and B;
X is the output of our circuit.

Truth table

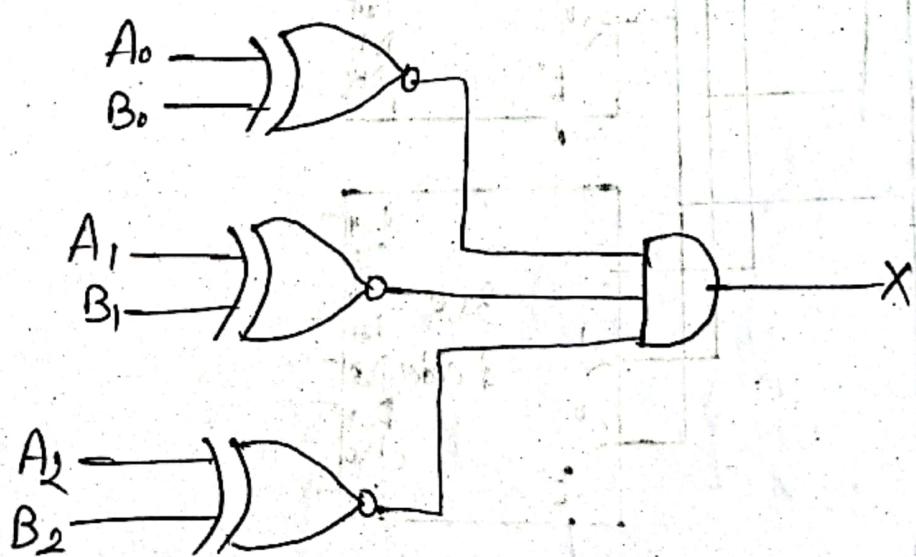
| A | B | X |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

$$\therefore X = A \oplus B$$

$$A = A_2 \ A_1 \ A_0$$

$$B = B_2 \ B_1 \ B_0$$

Desired circuit will be:



Ans to the Question no: 03(a)

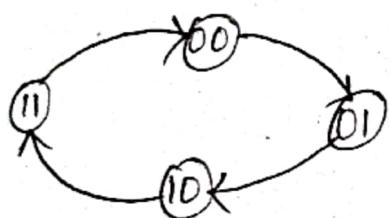
2 bit synchronous counter by JK flip-flop:

Hence, $n = 2$ bits, Flip Flop = JK Flip Flop

Now, the excitation table of JK Flip Flop is given by,

| Q_n | Q_{n+1} | J | K |
|-------|-----------|-----|-----|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

Now, we will create the state diagram and state table:



| Q_1 | Q_0 | Q_1^+ | Q_0^+ | J, K_1 | J_0, K_0 |
|-------|-------|---------|---------|----------|------------|
| 0 | 0 | 0 | 1 | 0 X | 1 X |
| 0 | 1 | 1 | 0 | 1 X | X 1 |
| 1 | 0 | 1 | 1 | X 0 | 1 X |
| 1 | 1 | 0 | 0 | X 1 | X 1 |

And we will find the boolean expression for it.

| J_1 | Q_0 | Q_1 |
|-------|-------|-------|
| 0 | 0 | 1 |
| 1 | X | X |

| K_1 | Q_0 | Q_1 |
|-------|-------|-------|
| 0 | 0 | 1 |
| 1 | X | X |

$$J_1 = Q_0$$

$$K_1 = Q_0$$

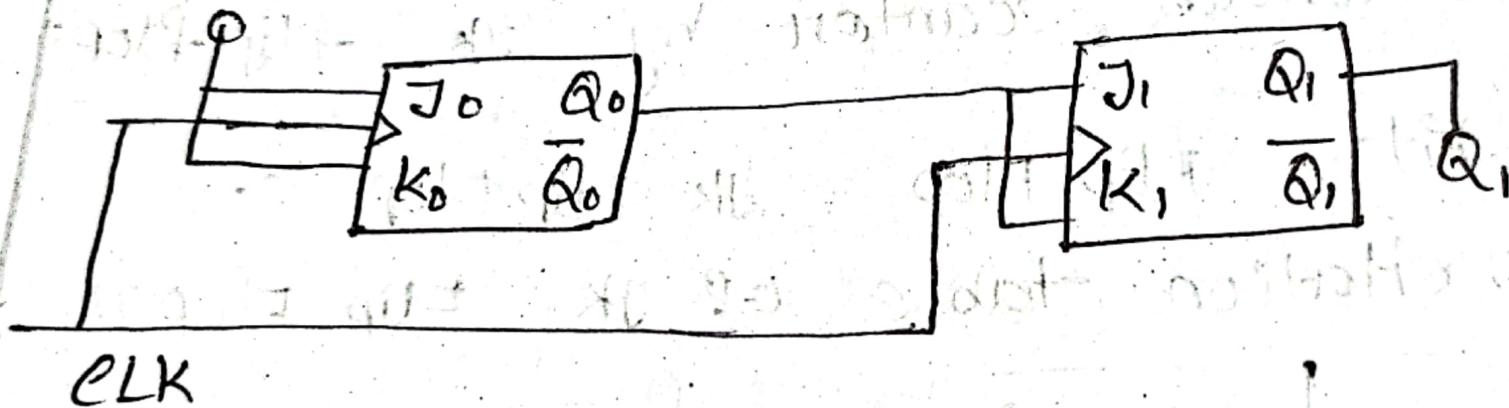
| J_0 | Q_0 | Q_1 |
|-------|-------|-------|
| 0 | 0 | 1 |
| 1 | X | X |

$$J_0 = 1$$

| K_0 | Q_0 | Q_1 |
|-------|-------|-------|
| 0 | X | 1 |
| 1 | X | 1 |

$$K_0 = 1$$

finally, we will make the circuit.



and that is how we design a 2 bit
Synchronous counter by JK Flip Flop.

Ans to the Question no: 04 (a)

Step 1 - counting num of ff. highest num = 7,

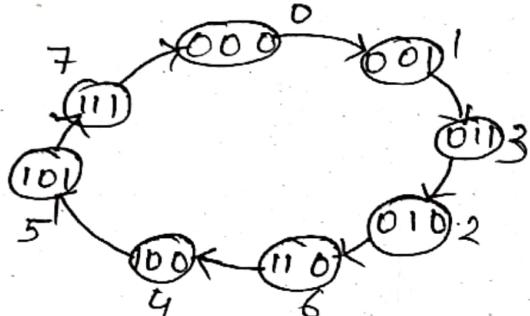
$$\therefore 7 + 1 = 8,$$

mod = 8 counter

$$2^n \geq N \Rightarrow \cancel{2^8}$$

$$\therefore 2^8 \geq 8, n = 3$$

Step 2 : state diagram



| | |
|---|-------------------|
| 0 | $\rightarrow 000$ |
| 1 | $\rightarrow 001$ |
| 3 | $\rightarrow 011$ |
| 2 | $\rightarrow 010$ |
| 6 | $\rightarrow 110$ |
| 7 | $\rightarrow 100$ |
| 5 | $\rightarrow 101$ |
| 4 | $\rightarrow 111$ |

Step 3: Excitation table of SR FF

| Q_n | Q_{n+1} | S | R |
|-------|-----------|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | X | 0 |

Step 4:

| P | Present State | | | | Next state | | | | FF | | | |
|---|----------------|----------------|----------------|------------------|------------------|------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | Q _A | Q _B | Q _C | Q _{A+1} | Q _{B+1} | Q _{C+1} | S _A | P _A | S _B | P _B | S _C | P _C |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | X | 0 | X | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | X | 1 | 0 | X | 0 |
| 2 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | X | 0 | 0 | X |
| 3 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | X | X | 0 | 0 | 1 |
| 4 | 1 | 0 | 0 | 1 | 0 | 1 | X | 0 | 0 | X | 1 | 0 |
| 5 | 1 | 0 | 1 | 1 | 1 | X | 0 | 1 | 0 | X | 0 | . |
| 6 | 1 | 1 | 0 | 1 | 0 | 0 | X | 0 | 0 | 1 | 0 | X |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

Step 5 Drawing k map

| | | S _A Q _B Q _C | | | |
|-----|---|--|----|----|----|
| | | 00 | 01 | 11 | 10 |
| (I) | 0 | 0 | 0 | 1 | 0 |
| | 1 | X | X | X | 0 |

$$S_A \rightarrow Q_B Q_C$$

| | | R _A Q _B Q _C | | | |
|------|---|--|----|----|----|
| | | 00 | 01 | 11 | 10 |
| (II) | 0 | X | X | 0 | X |
| | 1 | 0 | 0 | 0 | 1 |

$$R_A = Q_B \bar{Q}_C$$

| | | S _B Q _A Q _C | | | |
|-------|---|--|----|----|----|
| | | 00 | 01 | 11 | 10 |
| (III) | 0 | 0 | 1 | X | X |
| | 1 | 0 | 1 | 0 | 0 |

$$S_B = \bar{Q}_B \bar{Q}_C$$

| | | R _B Q _C | | | |
|------|---|-------------------------------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| (IV) | 0 | X | 0 | 0 | 0 |
| | 1 | X | 0 | 1 | 1 |

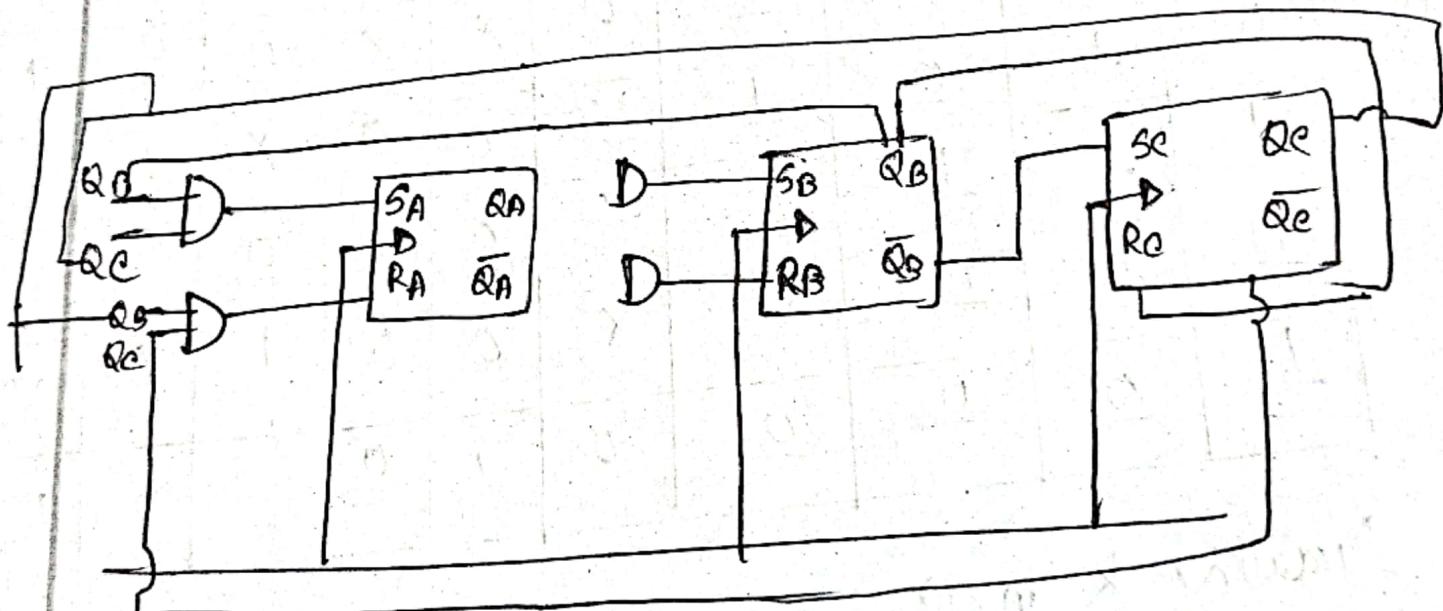
$$R_B = Q_A Q_3$$

(5) Sc:

| | QBQC | 00 | 01 | 11 | 10 |
|----|------|----|----|----|----|
| QA | 0 | 1 | X | 0 | 0 |
| | 1 | 1 | X | 0 | 0 |

| | QBQC | 00 | 01 | 11 | 10 |
|---|------|----|----|----|----|
| n | 0 | 0 | X | 1 | |
| | 0 | 0 | X | 1 | |

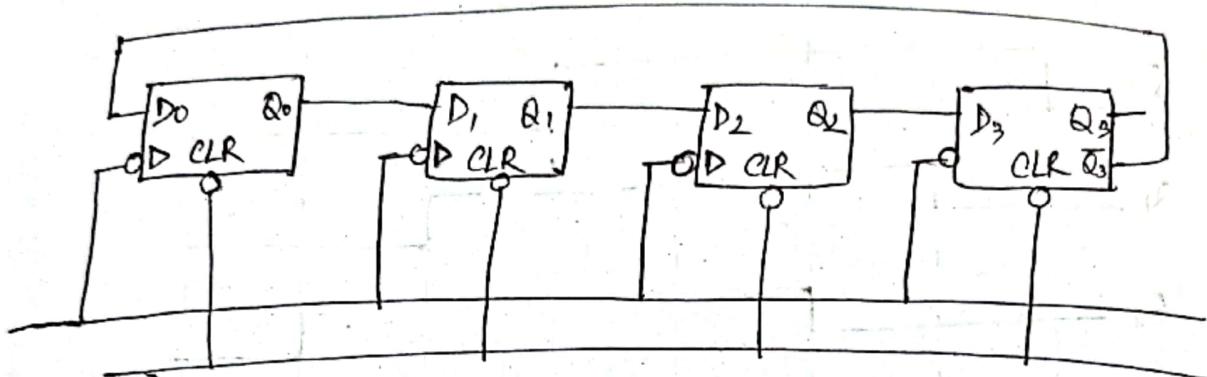
$S_C \rightarrow Q_B$



Ans to the Question no; 4(b)

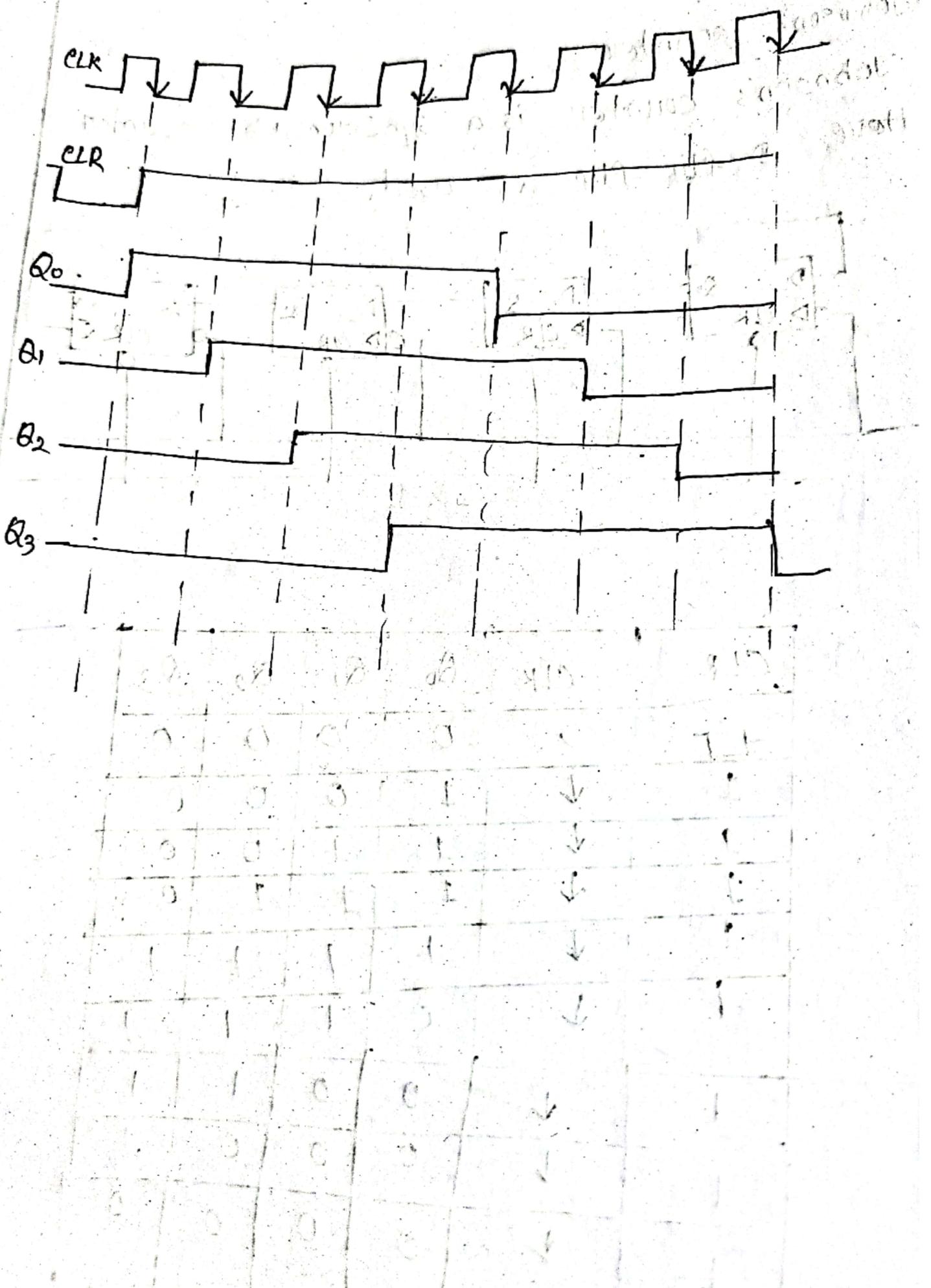
Johnson's counter:

Johnson's counter is a synchronous counter, hence D flip-flop are used.



| CLR | CLK | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
|-----|-----|----------------|----------------|----------------|----------------|
| 1 | X | 0 | 0 | 0 | 0 |
| 1 | ↓ | 1 | 0 | 0 | 0 |
| 1 | ↓ | 1 | 1 | 0 | 0 |
| 1 | ↓ | 1 | 1 | 1 | 0 |
| 1 | ↓ | 1 | 1 | 1 | 1 |
| 1 | ↓ | 0 | 1 | 1 | 1 |
| 1 | ↓ | 0 | 0 | 1 | 1 |
| 1 | ↓ | 0 | 0 | 0 | 1 |
| 1 | ↓ | 0 | 0 | 0 | 0 |

$\therefore \text{No of states} = 2 \times \text{No of bits}$



Ans to the Question no: 05 (a)

Rom: Rom stands for Read only memory.

It is a type of computer memory that stores data and ~~information~~ instructions permanently and cannot be easily modified. It retains its content even when the power is turned off and is commonly used for storing firmware and essential system data.

5(a) OR

Registers: Register is a component used to store and hold binary data temporarily. It consists of a group of flip flops or memory cells that can store multiple bits of information. Registers are commonly used in various digital systems such as microprocessors to store data during processing or to hold control signals.

Function of universal shift register:

1. Shift left
2. Shift right
3. PIP
4. Hold data

Ans to the Question no: 5(b)

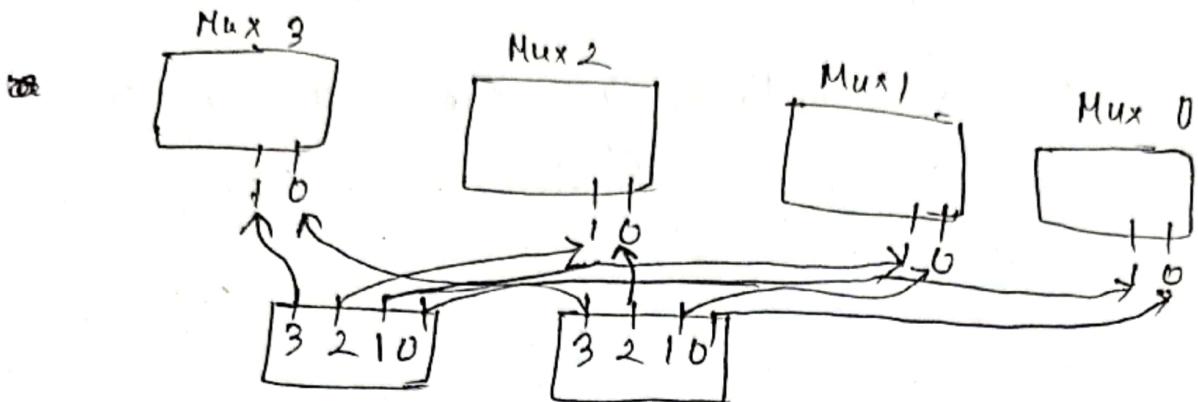
Moore's state machine with example:

Moore machine is a finite state machine in which the next state is decided by the current state and current input symbols. The output symbol at a given time depends only on the present state of the machine. Moore machine can be described by 6 types $(Q, q_0, \Sigma, O, \delta, \pi)$ where Q is the set of states.

Example: An elevator is a good example. Each floor is a different state in the machine. Now, when we press a button to get to a certain level we change the actual state of the machine to the new level without giving any additional input.

5(b) OR

A digital computer has a common



Hence, 2 registers having size 4 bits connect
4 multiplexers with 2 inputs.

2 registers with size $4 = 2 \times 1$ size of multiplexers
so, the number of 4 multiplexers are required.

Similarly, 16 registers with size 32 bits $= 16 \times 1$
size of multiplexers.

The number of 32 multiplexers are required
 ~~$2^3 = 16$~~

If size of multiplexer is 16×1 then
Selection require $2^n = 16$

$$2^n = 2^4$$

$$\therefore n = 4$$

That means four selection can be done.

So this four S_0, S_1, S_2, S_3 selection lines to select

one of 16 registers.

(b) The 16×1 size of multiplexers are needed.

(c) 32 multiplexers are required for this construction.

