CSE 331/503-COMPUTER ORGANIZATION

#HW3

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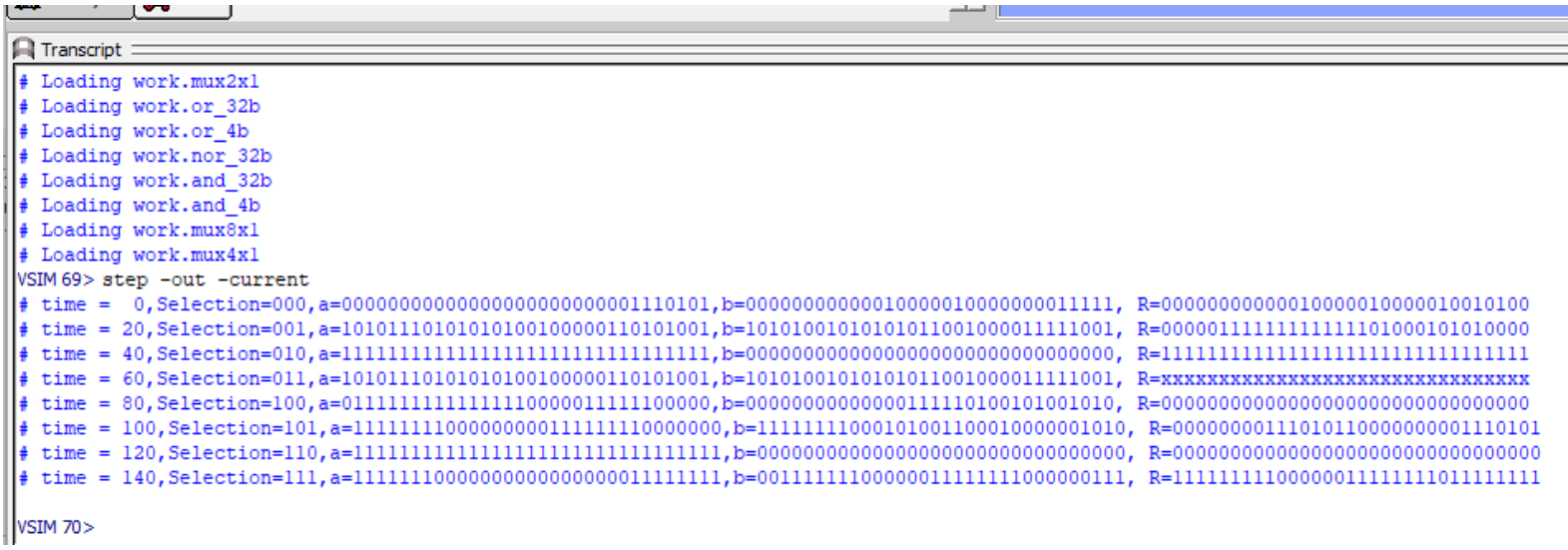
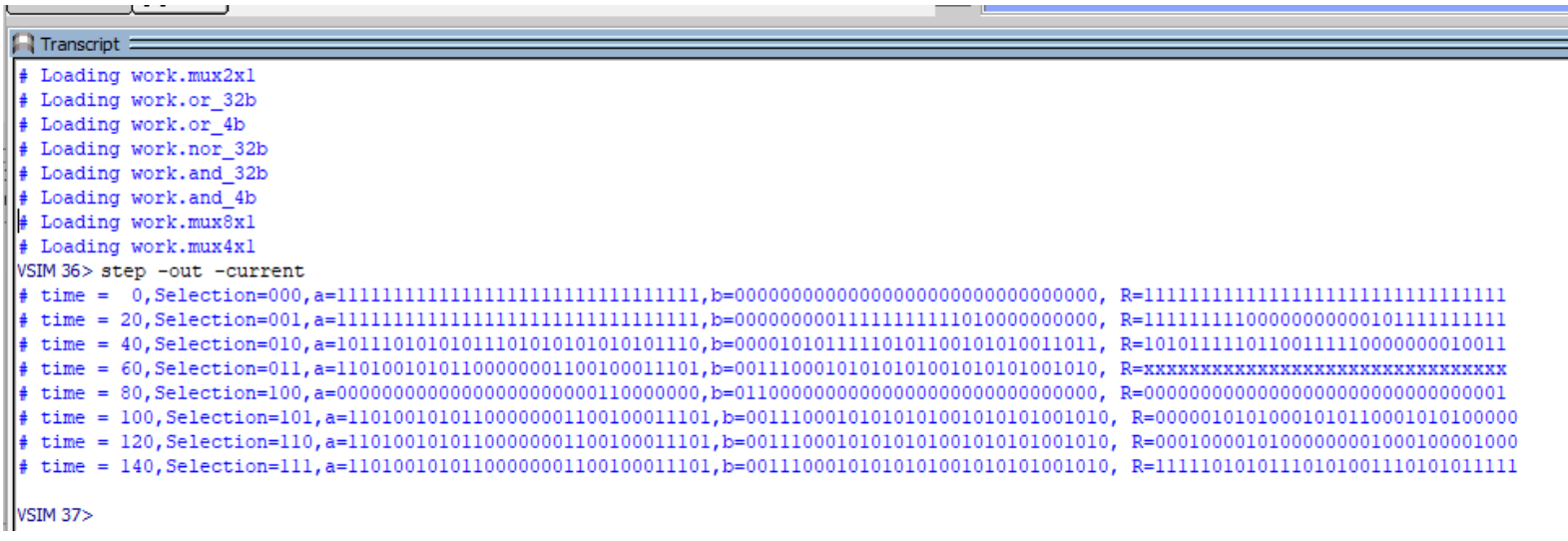
- In this homework i created 4 bit and,or,xor modules to create 32 bit and,or and xor gates. I created 32 bit nor gate by using 1 bit nor operator 32 times, 32 bit adder by calling 4 bit adder 8 times, substractor module by using 32 bit adder and 2x1 mux, slt module by using substractor and 2x1 mux. I also had to create 8x1 mux to select all these operations. For this, i created 4x1 mux by using 2x1 mux 3 times first. Then i used 4x1 2 times and 2x1 mux 1 times to create 8x1 mux. After all these implementations, i am able to run 32 bit ALU without multiplication. I couldn't implement multiplication so in the test images multiplication results are shown with xxxxx. You can run the program by compiling all .v files and run test.v file.





TESTBENCH RESULTS

and_4b Testbench:

```
1  `define DELAY 20
2  module and_4b_testbench();
3  reg [3:0] a,b;
4  wire [3:0] R;
5
6  and_4b a0(a,b,R);
7  initial begin
8  a = 4'b1010;
9  b = 4'b1111;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%4b,b=%4b,Result=%4b", $time,a,b,R);
14 end
15
16 endmodule
```

```
Transcript
# Loading work.and_4b_testbench
# Loading work.and_4b
add wave -position insertpoint  \
sim:/and_4b_testbench/a \
sim:/and_4b_testbench/b \
sim:/and_4b_testbench/R
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#
#           File in use by: atkna  Hostname: ATAKAN  ProcessID: 19568
#
#           Attempting to use alternate WLF file "./wlft374veb".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#
#           Using alternate file: ./wlft374veb
#
VSIM 45> step -out -current
# time =  0 ,a=1010,b=1111,Result=1010

VSIM 46>
```

or_4b Testbench:

```
1  `define DELAY 20
2  module or_4b_testbench();
3  reg [3:0] a,b;
4  wire [3:0] R;
5
6  or_4b o0(a,b,R);
7  initial begin
8  a = 4'b1010;
9  b = 4'b1111;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%4b,b=%4b,Result=%4b", $time,a,b,R);
14 end
15
16 endmodule
```

Transcript

```
# Loading work.or_4b_testbench
# Loading work.or_4b
add wave -position insertpoint  \
sim:/or_4b_testbench/a \
sim:/or_4b_testbench/b \
sim:/or_4b_testbench/R
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#
#           File in use by: atkna  Hostname: ATAKAN  ProcessID: 19568
#
#           Attempting to use alternate WLF file "./wlftvdacne".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#
#           Using alternate file: ./wlftvdacne
#
VSIM 25> step -out -current
# time =  0 ,a=1010,b=1111,Result=1111

VSIM 26>
```

Xor_4b Testbench:

```
1  `define DELAY 20
2  module xor_4b_testbench();
3  reg [3:0] a,b;
4  wire [3:0] R;
5
6  xor_4b x0(a,b,R);
7  initial begin
8  a = 4'b1010;
9  b = 4'b1111;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%4b,b=%4b,Result=%4b", $time,a,b,R);
14 end
15
16 endmodule
```

Transcript

```
# Loading work.xor_4b_testbench
# Loading work.xor_4b
add wave -position insertpoint  \
sim:/xor_4b_testbench/a \
sim:/xor_4b_testbench/b \
sim:/xor_4b_testbench/R
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#
#           File in use by: atkna  Hostname: ATAKAN  ProcessID: 19568
#
#           Attempting to use alternate WLF file "./wlftjkixet".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#
#           Using alternate file: ./wlftjkixet
#
VSIM 26> step -out -current
# time =  0 ,a=1010,b=1111,Result=0101

VSIM 27>
```

and_32b Testbench:

```
1  `define DELAY 20
2  module and_32b_testbench();
3  reg [31:0] a,b;
4  wire [31:0] R;
5
6  and_32b a0(a,b,R);
7  initial begin
8  a = 32'b01010101110101110101001010010001;
9  b = 32'b11100101010111101000011100111011;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%32b,b=%32b,Result=%32b", $time,a,b,R);
14 end
15
16 endmodule
```

```
Transcript
# -- Compiling module xor_4b_testbench
#
# Top level modules:
#       xor_4b_testbench
vlog -reportprogress 300 -work work E:/quartus/cse331/alu32/xor_32b.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b
#
# Top level modules:
#       xor_32b
ModelSim> vsim work.and_32b_testbench
# vsim work.and_32b_testbench
# Loading work.and_32b_testbench
# Loading work.and_32b
# Loading work.and_4b
VSIM 26> step -out -current
# time =  0 ,a=01010101110101110101001010010001,b=11100101010111101000011100111011,Result=01000101010101100000001000010001

VSIM 27>
```

or_32b Testbench:

```
1  `define DELAY 20
2  module or_32b_testbench();
3  reg [31:0] a,b;
4  wire [31:0] R;
5
6  or_32b o0(a,b,R);
7  initial begin
8  a = 32'b01010101110101110101001010010001;
9  b = 32'b11100101010111101000011100111011;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%32b,b=%32b,Result=%32b", $time,a,b,R);
14 end
15
16 endmodule
```

```
Transcript
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b
#
# Top level modules:
#       xor_32b
ModelSim> vsim work.or_32b_testbench
# vsim work.or_32b_testbench
# Loading work.or_32b_testbench
# Loading work.or_32b
# Loading work.or_4b
vsim work.or_32b_testbench
# vsim work.or_32b_testbench
# Loading work.or_32b_testbench
# Loading work.or_32b
# Loading work.or_4b
VSIM 27> step -out -current
# time =  0 ,a=01010101110101110101001010010001,b=11100101010111101000011100111011,Result=11110101110111111110101111010111011

VSIM 28>
```

xor_32b Testbench:

```
1  `define DELAY 20
2  module xor_32b_testbench();
3  reg [31:0] a,b;
4  wire [31:0] R;
5
6  xor_32b xor0(a,b,R);
7  initial begin
8  a = 32'b01010101111010111010100101001000 1;
9  b = 32'b11100101010111101000011100111011;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%32b,b=%32b,Result=%32b", $time,a,b,R);
14 end
15
16 endmodule
```

```
Transcript
# -- Compiling module xor_32b
#
# Top level modules:
#       xor_32b
vlog -reportprogress 300 -work work E:/quartus/cse331/alu32/xor_32b_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b_testbench
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.xor_32b_testbench
# vsim work.xor_32b_testbench
# Loading work.xor_32b_testbench
# Loading work.xor_32b
# Loading work.xor_4b
VSIM 28> step -out -current
# time =  0 ,a=01010101111010111010100101001000 1,b=11100101010111101000011100111011,Result=10110000100010011101010110101010

VSIM 29>
```

mux2x1 Testbench:

```
1  `define DELAY 20
2  module mux2x1_testbench();
3  reg [31:0]  a,b;
4  reg m;
5  wire [31:0] R;
6
7  mux2x1 m0(a,b,m,R);
8  initial begin
9  m=1'b0;
10 a = 32'b01010101010101010101110101011001;
11 b = 32'b10101110101010111111001010111010;
12 #`DELAY;
13 m=1'b1;
14 a = 32'b01010101010101010101110101011001;
15 b = 32'b10101110101010111111001010111010;
16 #`DELAY;
17 end
18
19 initial begin
20 $monitor("time = %2d ,a=%32b,b=%32b, Selection=%1b ,Result=%32b", $time,a,b,m,R);
21 end
22
23 endmodule
```

Transcript

```
# Top level modules:
#       xor_32b
vlog -reportprogress 300 -work work E:/quartus/cse331/alu32/xor_32b_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b_testbench
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.mux2x1_testbench
# vsim work.mux2x1_testbench
# Loading work.mux2x1_testbench
# Loading work.mux2x1
# Loading work.or_32b
# Loading work.or_4b
VSIM 29> step -out -current
# time =  0 ,a=01010101010101010101110101011001,b=10101110101010111111001010111010, Selection=0 ,Result=01010101010101010101110101011001
# time = 20 ,a=01010101010101010101110101011001,b=10101110101010111111001010111010, Selection=1 ,Result=10101110101010111111001010111010

VSIM 30>
```

mux4x1 Testbench:

```
1  `define DELAY 20
2  module mux4x1_testbench();
3  reg [31:0]  a,b,c,d;
4  reg  [1:0]m;
5  wire [31:0] R;
6
7
8  mux4x1 m0(a,b,c,d,m,R);
9  initial begin
10 m=2'b00;
11 a = 32'b10100101010111100111110000011101;
12 b = 32'b11001010101010111001111011101011;
13 c = 32'b01010101010100101001010010101010;
14 d = 32'b10101010010001110101010110110101;
15 #`DELAY;
16 m=2'b01;
17 a = 32'b10100101010111100111110000011101;
18 b = 32'b11001010101010111001111011101011;
19 c = 32'b01010101010100101001010010101010;
20 d = 32'b10101010010001110101010110110101;
21 #`DELAY;
22
23 m=2'b10;
24 a = 32'b10100101010111100111110000011101;
```

```
Transcript
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b_testbench
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.mux4x1_testbench
# vsim work.mux4x1_testbench
# Loading work.mux4x1_testbench
# Loading work.mux4x1
# Loading work.mux2x1
# Loading work.or_32b
# Loading work.or_4b
VSIM 29> step -out -current
# time =  0 , Selection=00 ,Out=10100101010111100111110000011101
# time = 20 , Selection=01 ,Out=11001010101010111001111011101011
# time = 40 , Selection=10 ,Out=01010101010100101001010010101010
# time = 60 , Selection=11 ,Out=10101010010001110101010110110101

VSIM 30>
```

-mux8x1 already tested in main code so it is not included here.

fullAdder Testbench:

```
 1  `define DELAY 20
 2  module full_adder_testbench();
 3  reg a, b, carry_in;
 4  wire sum, carry_out;
 5
 6  full_adder fatb (sum, carry_out, a, b, carry_in);
 7
 8  initial begin
 9  a = 1'b0; b = 1'b0; carry_in = 1'b0;
10  #`DELAY;
11  a = 1'b0; b = 1'b0; carry_in = 1'b1;
12  #`DELAY;
13  a = 1'b0; b = 1'b1; carry_in = 1'b0;
14  #`DELAY;
15  a = 1'b0; b = 1'b1; carry_in = 1'b1;
16  #`DELAY;
17  a = 1'b1; b = 1'b0; carry_in = 1'b0;
18  #`DELAY;
19  a = 1'b1; b = 1'b0; carry_in = 1'b1;
20  #`DELAY;
21  a = 1'b1; b = 1'b1; carry_in = 1'b0;
22  #`DELAY;
23  a = 1'b1; b = 1'b1; carry_in = 1'b1;
```

Transcript

```
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.full_adder_testbench
# vsim work.full_adder_testbench
# Loading work.full_adder_testbench
# Loading work.full_adder
# Loading work.half_adder
VSIM 31> step -out -current
# time =  0, a =0, b=0, carry_in=0, sum=0, carry_out=0
# time = 20, a =0, b=0, carry_in=1, sum=1, carry_out=0
# time = 40, a =0, b=1, carry_in=0, sum=1, carry_out=0
# time = 60, a =0, b=1, carry_in=1, sum=0, carry_out=1
# time = 80, a =1, b=0, carry_in=0, sum=1, carry_out=0
# time = 100, a =1, b=0, carry_in=1, sum=0, carry_out=1
# time = 120, a =1, b=1, carry_in=0, sum=0, carry_out=1
# time = 140, a =1, b=1, carry_in=1, sum=1, carry_out=1

VSIM 32>
```

half_adder Testbench:

```
1  `define DELAY 20
2  module half_adder_testbench();
3  reg a, b;
4  wire sum, carry_out;
5
6  half_adder hatb (sum, carry_out, a, b);
7
8  initial begin
9  a = 1'b0; b = 1'b0;
10 #`DELAY;
11 a = 1'b1; b = 1'b0;
12 #`DELAY;
13 a = 1'b0; b = 1'b1;
14 #`DELAY;
15 a = 1'b1; b = 1'b1;
16 end
17
18 initial
19 begin
20 $monitor("time = %2d, a =%1b, b=%1b, sum=%1b, carry_out=%1b", $time, a, b, sum, carry_out);
21 end
22
23 endmodule
```

Transcript

```
# Top level modules:
#       xor_32b
vlog -reportprogress 300 -work work E:/quartus/cse331/alu32/xor_32b_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b_testbench
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.half_adder_testbench
# vsim work.half_adder_testbench
# Loading work.half_adder_testbench
# Loading work.half_adder
VSIM 31> step -out -current
# time =  0, a =0, b=0, sum=0, carry_out=0
# time = 20, a =1, b=0, sum=1, carry_out=0
# time = 40, a =0, b=1, sum=1, carry_out=0
# time = 60, a =1, b=1, sum=0, carry_out=1

VSIM 32>
```

adder_4b Testbench:

```
1  `define DELAY 20
2  module adder_4b_testbench();
3  reg [3:0] a,b;
4  wire [3:0] R;
5  wire Cout;
6  reg Cin;
7  adder_4b a0(R,Cout,a,b,Cin);
8  initial begin
9  Cin = 1'b1;
10 a = 4'b1010;
11 b = 4'b1111;
12 #`DELAY;
13 Cin = 1'b0;
14 a = 4'b1010;
15 b = 4'b1111;
16 end
17
18 initial begin
19 $monitor("time = %2d ,a=%4b,b=%4b,Carry in=%1b,Carry out=%1b,Result=%4b", $time,a,b,Cout,Cin,R);
20 end
21
22 endmodule
```

Transcript

```
sim:/adder_4b_testbench/a \
sim:/adder_4b_testbench/b \
sim:/adder_4b_testbench/R \
sim:/adder_4b_testbench/Cout \
sim:/adder_4b_testbench/Cin
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#
#           File in use by: atkna  Hostname: ATAKAN  ProcessID: 19568
#
#           Attempting to use alternate WLF file "./wlftrbvz47".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#
#           Using alternate file: ./wlftrbvz47
#
VSIM 33> step -out -current
# time =  0 ,a=1010,b=1111,Carry in=1,Carry out=1,Result=1010
# time = 20 ,a=1010,b=1111,Carry in=1,Carry out=0,Result=1001

VSIM 34>
```

adder_32b Testbench:

```
1  `define DELAY 20
2  module adder_32b_testbench();
3  reg [31:0] a,b;
4  wire [31:0] R;
5  wire Cout;
6  reg Cin;
7  adder_32b a0(a,b,Cin,Cout,R);
8  initial begin
9  Cin = 1'b1;
10 a = 32'b10110101010000101010110101011011011;
11 b = 32'b01111010001010010100000111111100010;
12 #`DELAY;
13 Cin = 1'b0;
14 a = 32'b10110101010000101010110101011011011;
15 b = 32'b01111010001010010100000111111100010;
16 end
17
18 initial begin
19 $monitor("time = %2d ,a=%32b,b=%32b,Carry in=%1b,Carry out=%1b,Result=%32b", $time,a,b,Cout,Cin,R);
20 end
21
22 endmodule
```

```
Transcript
#       xor_32b
vlog -reportprogress 300 -work work E:/quartus/cse331/alu32/xor_32b_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b_testbench
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.adder_32b_testbench
# vsim work.adder_32b_testbench
# Loading work.adder_32b_testbench
# Loading work.adder_32b
# Loading work.adder_4b
# Loading work.full_adder
# Loading work.half_adder
VSIM 33> step -out -current
# time =  0 ,a=10110101010000101010110101011011,b=01111010001010010100000111111100010,Carry in=1,Carry out=1,Result=00101111100101111111000101011110
# time = 20 ,a=10110101010000101010110101011011,b=01111010001010010100000111111100010,Carry in=1,Carry out=0,Result=00101111100101111111000101011101

VSIM 34>
```

sub_32b Testbench:

```
1  `define DELAY 20
2  module sub_32b_testbench();
3  reg [31:0] a,b;
4  wire [31:0] R;
5  wire Cout;
6  reg Cin;
7  sub_32b a0(a,b,Cin,Cout,R);
8  initial begin
9  Cin = 1'b0;
10 a = 32'b10110101010001010101101011011011;
11 b = 32'b01111010010100101000011111100010;
12 end
13
14 initial begin
15 $monitor("time = %2d ,a=%32b,b=%32b,Result=%32b", $time,a,b,R);
16 end
17
18 endmodule
```

```
Transcript
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b_testbench
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.sub_32b_testbench
# vsim work.sub_32b_testbench
# Loading work.sub_32b_testbench
# Loading work.sub_32b
# Loading work.xor_32b
# Loading work.xor_4b
# Loading work.adder_32b
# Loading work.adder_4b
# Loading work.full_adder
# Loading work.half_adder
VSIM 34> step -out -current
# time =  0 ,a=10110101010001010101101011011011,b=01111010010100101000011111100010,Result=00111010111100101101001011111001

VSIM 35>
```

nor_32b Testbench:

```
1  `define DELAY 20
2  module nor_32b_testbench();
3  reg [31:0] a,b;
4  wire [31:0] R;
5
6  nor_32b a0(a,b,R);
7  initial begin
8  a = 32'b01010101110101110101001010010001;
9  b = 32'b11100101010111101000011100111011;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%32b,b=%32b,Result=%32b", $time,a,b,R);
14 end
15
16 endmodule
```

Transcript

```
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b
#
# Top level modules:
#       xor_32b
vlog -reportprogress 300 -work work E:/quartus/cse331/alu32/xor_32b_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module xor_32b_testbench
#
# Top level modules:
#       xor_32b_testbench
ModelSim> vsim work.nor_32b_testbench
# vsim work.nor_32b_testbench
# Loading work.nor_32b_testbench
# Loading work.nor_32b
VSIM 35> step -out -current
# time =  0 ,a=01010101110101110101001010010001,b=11100101010111101000011100111011,Result=00001010001000000010100001000100

VSIM 36>
```

slt_32b Testbench:

```
1  `define DELAY 20
2  module slt_32b_testbench();
3  reg [31:0] a,b;
4  wire [31:0] R;
5
6  slt_32b a0(a,b,R);
7  initial begin
8  a = 32'b01010101110101110101001010010001;
9  b = 32'b01100101010111101000011100111011;
10 end
11
12 initial begin
13 $monitor("time = %2d ,a=%32b,b=%32b,Result=%32b", $time,a,b,R);
14 end
15
16 endmodule
```

```
Transcript
#       xor_32b_testbench
ModelSim> vsim work.slt_32b_testbench
# vsim work.slt_32b_testbench
# Loading work.slt_32b_testbench
# Loading work.slt_32b
# Loading work.sub_32b
# Loading work.xor_32b
# Loading work.xor_4b
# Loading work.adder_32b
# Loading work.adder_4b
# Loading work.full_adder
# Loading work.half_adder
# Loading work.mux2x1
# Loading work.or_32b
# Loading work.or_4b
VSIM 36> step -out -current
# time =  0 ,a=01010101110101110101001010010001,b=01100101010111101000011100111011,Result=00000000000000000000000000000001

VSIM 37>
```