Design of Low Power 7T SRAM cell using Charge Pumps for IoT Applications.

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***Abstract*—This paper introduces a low-voltage 7T SRAM cell designed using a charge pump for IoT applications. A 3-stage charge pump circuit is introduced to improve the voltage supply VDD' to SRAM. In this design cross-connected NMOS charge pump is designed and placed in between the voltage supply and the SRAM cell.**

***Index Terms*—IoT, charge pump, low power, 7T SRAM.**

I. Introduction

Nowadays, there is a gradual rise in the usage of IoT devices. Power is very limited in IoT applications, but enhancing the circuits' performance requires higher voltages. To increase the voltage supply to SRAM a cross-connected NMOS charge pump is placed in between the voltage supply and the SRAM cell. For an SRAM to operate at high speeds it requires higher voltages. Instead of using the power supplies with higher voltages a charge pump can be introduced to overcome the problem of higher voltage requirements with limited power supply. In this design, a charge pump is introduced to increase the voltage across the SRAM so that faster read/write operations can be performed.

II. Principle of Generation

A 3-stage charge pump is introduced to increase the voltage across the inverters in the SRAM as shown in Fig. 1. The charge pump circuit is enabled only when there is read/write operation taking place in the hold situation actual input voltage is provided to the SRAM inverters. This allows to limit the power when there is no operation taking place in the SRAM.

III. Implementation

In Fig. 2, a 3-stage charge pump circuit is shown which consists of a voltage-controlled oscillator, driver, and the charge pump circuit. All the power supply is taken from the VDD and the input voltage VDD is amplified to a certain voltage at which the SRAM transistors can operate with improved drive strength. In this design, the transistor width in the oscillator and charge pump will be maintained low and the driver circuit comparatively requires a slightly higher width to drive more current so that there will be no voltage drop when supplied to the charge pump. The oscillator will be having a NAND gate followed by 4 inverters. This is to enable the oscillator when the operation is taking place.

IV. Issues and Improvement

Using this charge Pump the voltage amplification can be done to word line voltage so that read and write access speed is improved.

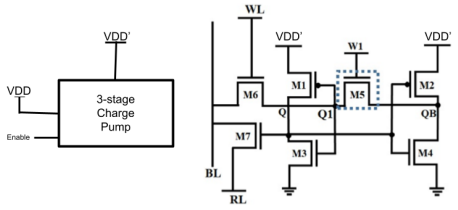

Fig. 1. Charge Pump based 7T SRAM

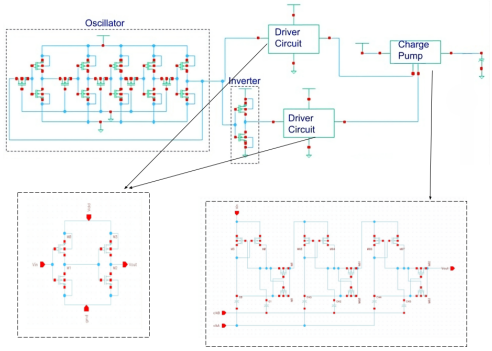

Fig. 2. 3-stage Charge Pump Circuit[3]

V. Conclusion

This paper discusses the design of a low-power 7T SRAM cell using a charge pump circuit to improve the speed of the SRAM at low-power applications. 7T SRAM cell is selected in design because the bandwidth of 7T SRAM is higher compared to 6T and 8T SRAM cells[1]. This allows the IoT devices to operate at relatively higher speeds with approximately similar power consumption.

References

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