

DESIGN OF ULTRA-LOW POWER FINFET CHARGE PUMPS FOR ENERGY HARVESTING SYSTEMS

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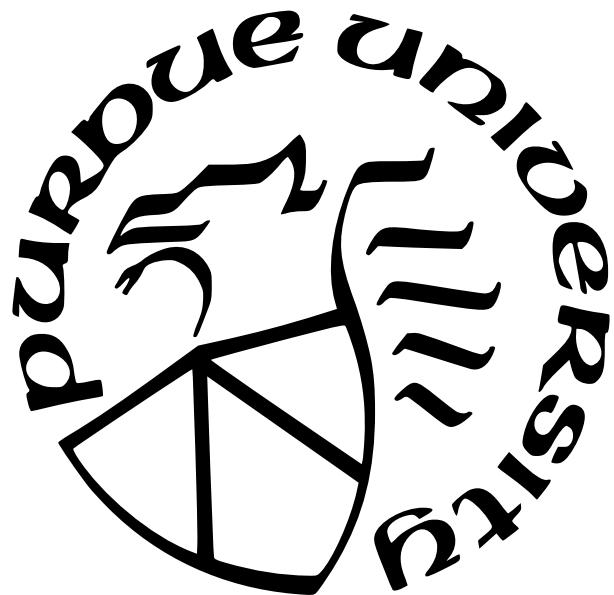
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ABSTRACT

Due to the increasing popularity and use of medical equipment such as body implants, biosensors, and health monitoring systems, there is an unending need for smaller, quicker, cheaper, safer, and lower power-consuming gadgets. Because of this, energy harvesting is an essential area of attention for many contemporary research projects. Energy harvesting is also helpful in several other applications, such as Internet of Things devices, cars, etc. Depending on the application, a charge pump circuit transforms a power source to a high or low voltage. In memory design, charge pumps are often considered a range of power supplies needed for more advanced memory systems. Additionally, charge pumps may be made to run at low voltage. They can change the small output voltage level of the energy harvesting device to the one required for the medical device to function. This study suggests using an integrated FinFET (Field Effect Transistor) based charge pump design for ultra-low-power energy harvesting applications.

The modeling and review of this system were carried out utilizing Cadence Virtuoso Schematic L-Editing, Analog Design Environment, employing 7nm FinFETs from the ASAP7 7nm PDK file. This research leverages inherent characteristics of FinFET technology, such as reduced body effects, switching speeds, lower threshold voltages, and decreased power consumption. The decreased threshold voltage of FinFETs is crucial for achieving high performance at lower supply voltages.

This work introduces an ultra-low-voltage charge pump for energy harvesters in biosensors. The unique aspect of the charge pump designed in this work is its two-level design, where the first stage elevates the voltage to a specific level, and the output voltage of the first stage becomes the input voltage of the second stage. Using two levels reduces the number of stages of the charge pump and improves efficiency to get a higher voltage gain. In our measurements, this charge pump design could convert a low 85 mV input voltage to a substantial 608.2 mV output voltage, approximately 7.15 times the input voltage, while maintaining a load resistance of $7\text{ M}\Omega$ and a 29.5% conversion efficiency.

1. INTRODUCTION

1.1 Motivation

Nowadays, there is a gradual rise in the usage of biosensors and wearable health monitoring devices. Using batteries for these devices can make the devices bulkier. Replacing and recharging the batteries might be difficult because some biosensors and devices cannot often be replaced. Energy harvesting technologies like thermoelectric generators and biochemical cells can produce voltage from human skin and body liquids. However, the voltages generated by these energy harvesters are very low, near a few milli volts. A low-input DC-DC converter circuit needs to boost the harvested voltage to a usable output voltage. The power management system in these applications uses switched capacitors, switched inductors, or both. These switch capacitors are used in low-power devices like sensors where energy harvesters produce voltage from their environment. A charge pump is one such switched capacitor containing diodes or CMOS transistors as switches to multiply the voltage. The charge pump is mainly used in energy-harvesting applications and memory management circuits [1]. However, using inductors and large capacitors results in bulking the device, which might not be suitable for biosensors. Many projects have implemented different charge pump circuit design techniques for energy harvesting applications, but most have off-chip components and contain inductors. A system-on-chip IC(integrated circuits) has been designed to overcome this issue. More studies are needed on the use of FinFET technology in designing charge pumps. The use of FinFET technology in charge pump design offers several significant advantages, including its unique ability to vary the width of the transistor while keeping the length constant and the potential to increase the width of the transistor by increasing the number of fins. These features make FinFET technology a promising tool for enhancing the efficiency and performance of charge. Pump designs. Efforts to strengthen charge pump performance significantly benefit many of today's leading industries. A single figure of merit does not encapsulate overall Charge Pump performance due to the varying design constraints such as output voltage requirements, area, and power efficiency. Recent research has predominantly focused on Charge Pump design for volatile and flash memory, where power consumption is considerably higher than in energy harvesting domains. Nonetheless,

these findings often apply across different domains and designs. A key area of advancement in adiabatic design methods is recycling, which would otherwise be wasted flowing to the ground terminal. Another effective adiabatic strategy involves efficient gate-controlling mechanisms, with recent work presenting a Linear Charge Pump utilizing isentropic gate control to enhance performance [2].

1.2 Methodology

This thesis work introduces an integrated Circuit design of a 7nm FinFET (Field Effect Transistor) charge pump with adiabatic pumping strategies. The standout feature of this work is its capability to convert an 85 mV voltage produced by an energy harvester to a controlled 608.2 mV pumped output voltage while maintaining a load resistance of $7\text{ M}\Omega$ without any external components. This system is designed and analyzed using Cadence Virtuoso Schematic L-Editing, Analog Design Environment with the 7nm FinFETs from the ASAP 7nm PDK [3]. The experiment is limited to schematic design and simulations because of the unavailability of software tools like layout vs. schematic (LVS) verification or parasitic extraction from the design netlist. To present a general roadmap, this thesis is arranged as follows: Chapter 2 delves into various energy sources of the human body, focusing on the thermoelectric generator. Chapter 3 explores related research addressing Charge Pump designs in energy harvesting applications. Chapter 4 introduces FinFETs, discussing their operation compared to traditional CMOS devices. Chapter 5 examines essential Charge Pump operations with an in-depth analysis of the Dickson Charge Pump. Chapter 6 covers the circuits necessary for the Charge Pump's functionality, including oscillators, pump drivers, and pumps, and presents the results, offering an objective comparison with other state-of-the-art Charge Pumps. Finally, Chapter 7 provides recommendations for future research, and Chapter 8 summarizes the work presented in this thesis.

2. ENERGY HARVESTING

2.1 Sources of Energy in Human Body

Energy, the capacity to do work, and power, the rate of doing work over time, are commonly measured in watts ($W = \text{kg} \cdot \text{m}^2/\text{s}^3$) or joules per second. The human body, a significant reservoir of energy, consumes energy at a stunning rate of almost 70,000 to 1,400,000 calories per hour, depending on our activity. Trained athletes can burn up to 9.5 million calories per hour for a short period. The energy rate, or power, utilized while sleeping is approximately 81 W [4]. Even harnessing a small fraction of this power could eliminate the need for batteries. However, challenges arise in acquiring, regulating, and distributing this power. The innovative aspect of this research lies in the fact that modern electronic devices are now small enough to be integrated into clothes or be worn on the body [5]. We will discuss various power generation methods from human activities, including breath, thermal energy, blood flow, and human body motion. Although some concepts may seem imaginative, each has unique benefits and practical applications in medical electronic systems, consumer electronics, and sensors. For example, an average person weighing 68 kg can intake air at about 30 liters per minute. However, the pressure from breathing is only 2% more than the atmospheric pressure. Increased effort for breathing intake can have adverse physiological effects, so only exhaling is considered for energy harvesting. Therefore, the available power can be calculated, although it decreases during sleep and increases with physical activity. Using an aircraft-style pressure mask can elevate breath pressure by a factor of 2.5 but stresses the user significantly. Breath masks, already used by professionals such as pilots and astronauts, could harness this energy. Despite the efficiency of turbines and generators being around 40 percent, trapping this energy source would cause additional stress on the user. An alternative method is fastening a tight, flexible band around the chest, taking advantage of the change in chest circumference during breathing. Empirical measurements show a 2.5-centimeter change with normal breathing and up to a 5-cm change is observed with deep breathing. The total power generated can be estimated with a breathing rate of 10 breaths per minute and a force of 100 N applied over 0.05 meters. A sprocket and flywheel system are attached to an elastic band around the chest could harvest some of the energy.

However, the resulting power of about 0.42 W is minimal and may not justify the inconvenience. The human body creates heat through metabolic processes required for maintaining life. The basal metabolic rate (BMR) produces the energy even at rest to maintain vital physiological functions, which translates to a continuous power output of approximately 100 watts. Thermoelectric generators (TEGs) transform heat energy into electrical energy using the Seebeck effect, where the heat difference across a thermoelectric material produces a voltage. Generating power from blood pressure, although seemingly impractical, offers intriguing possibilities. The power generated can be calculated by considering an average blood pressure of 100 mm Hg with a resting heart rate of 60 beats per minute and a heart stroke volume of 70 mL per beat [6]. This energy rate is doubled during physical activity; capturing it is complex. Introducing a turbine would cause stress on the heart, potentially to dangerous levels. However, even harnessing 2 percent of this power could support low-power microprocessors and sensors, enabling self-powered medical sensors. Comparing activities such as guitar playing and walking, which use up to 30 kcal/hr more power compared to standing, reveals significant potential for energy recovery from upper limb movements. Empirical studies indicate that for a 60 kg man, the lower arm mass is 1.4 kg, the upper arm is 1.8 kg, and the whole arm is 3.2 kg. The center of mass of the lower arm moves 0.335 meters on a good bicep curl, and raising the hand over the head moves the center of mass 0.725 meters. If bicep curls can be performed at a maximum speed of 2 curls per second and arm lifts at 1.3 per second, generating up to 24W and 60W, respectively. These calculations suggest that even less strenuous activities could yield recoverable energy. Assuming a user makes an arm gesture for two seconds, generating 3 W of power is feasible. With a pulley system on the belt, multiplying the load on the user's arms could recover 1.5 W, but this setup would be highly inconvenient. Walking also offers a promising method for generating power. The repetitive walking motion can be harnessed using piezoelectric materials that generate electricity under mechanical stress. Piezoelectric shoe inserts can convert the pressure and motion from walking into electrical energy. Studies suggest that a person walking at a brisk pace can generate around 5 watts of power per shoe. However, the conversion efficiency of this energy into usable power is currently around 20-30 percent. Nevertheless, even at this efficiency, walking could provide a continuous power source for low-energy devices.

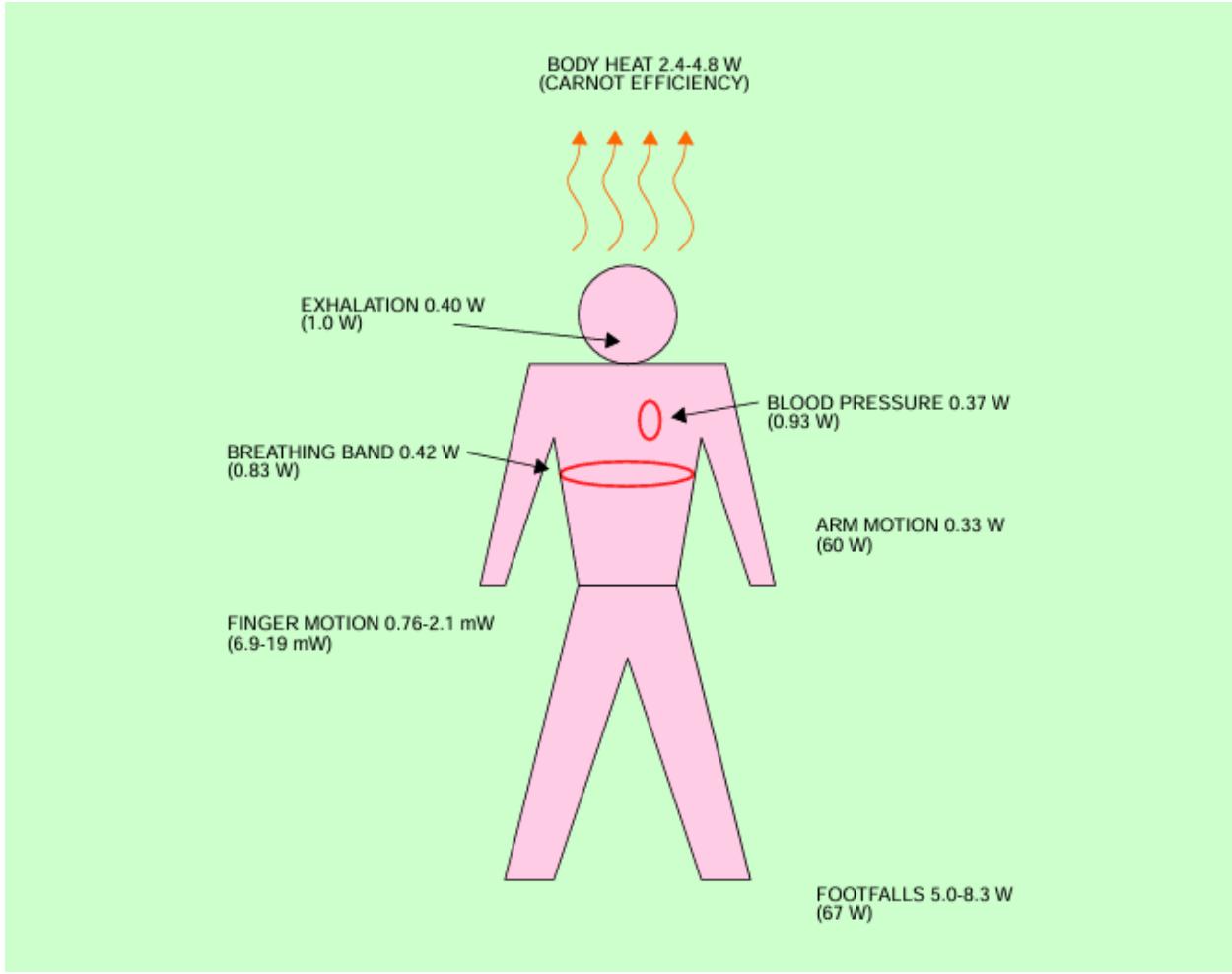


Figure 2.1. : Power from body-driven sources [4]

Typing and other repetitive finger motions can also be used for energy harvesting. Typing, for instance, involves rapid finger movements that can be captured using small piezoelectric generators embedded in keyboards or wearable devices. Although the power generated per keystroke is minimal, the high typing frequency can cumulatively produce significant power. For example, a typist averaging 40 words per minute could generate approximately 0.006 W, sufficient to power tiny sensors or contribute to the overall energy budget of a wearable device. In Figure 2.1, we observe various energy sources produced by the human body.

In these methods, body heat offers viable energy source. The average human body emits around 100 watts of heat, which can be captured using thermoelectric generators. These

devices exploit the temperature difference between the body and the surrounding environment to generate electricity. Although the efficiency of thermoelectric generators is relatively low, advancements in materials science and device design are steadily improving their performance. Even with modest efficiency, body heat provides a continuous and unobtrusive power source for wearable electronics and sensors. The potential for generating power from everyday human activities is vast and varied. While current technologies and methods have limitations, ongoing research and development hold promise for more efficient and practical energy harvesting solutions. Integrating these technologies into clothing, accessories, and everyday objects may reduce or even eliminate the need for traditional batteries in many applications. This inspiring prospect paves the way for more sustainable and self-sufficient electronic devices, revolutionizing the field of energy harvesting.

2.2 Thermal Energy

The human body is a continuous heat source primarily generated by metabolic processes. Figure 2.2 demonstrates the food energy taken by humans is utilized for work, stored as fat, and also releases thermal energy. While the body naturally dissipates this heat, exploring methods to capture and use it for technological applications offers intriguing possibilities. The human body emits heat energy, which can be harnessed. However, the efficiency of converting this waste heat into usable energy is constrained by the principles of thermodynamics, precisely Carnot efficiency. The Carnot efficiency provides a maximum limit on the conversion of heat to work based on the heat difference between the human body and the surrounding environment. For instance, with an average body temperature and an ambient temperature of 20°C, the Carnot efficiency can be calculated using the formula:

$$1 - \frac{T_{\text{ambient}}}{T_{\text{body}}} = \frac{(310 \text{ K} - 293 \text{ K})}{310 \text{ K}} = 5.5\% \quad (2.1)$$

Where T_{ambient} is the ambient temperature in Kelvin and T_{body} is the body temperature in Kelvin. In warmer environments (27°C), the Carnot efficiency drops to around 3.2%. Considering a typical power output of 116 W from the body while sitting, a Carnot engine could recover between 3.7 W and 6.4 W. However, higher efficiencies require more extreme tem-

perature differences, which are impractical in everyday settings due to the need to maintain thermal comfort. Moreover, evaporative heat loss, which accounts for approximately 25 % of total heat dissipation, further limits the recoverable energy. This heat loss occurs through insensible perspiration, including water diffusion through the skin and moisture-laden air from the lungs. Without reclaiming the latent heat of vaporization, the maximum power that can be effectively harnessed drops to about 2.8 W to 4.8 W. Any system designed to capture body heat would need to encapsulate the user, similar to a wetsuit, to transfer heat efficiently [4]. However, this approach presents challenges:

- **Thermoregulation:** The body's natural response to cold, which includes constricting blood flow to the skin, would reduce the heat available for recovery.
- **Practicality and Comfort:** Encapsulating devices might be impractical or uncomfortable for everyday use. However, localized solutions, such as a neck brace or a head cover, could provide some potential for harnessing heat energy.

The human body dissipates heat through several mechanisms:

- Radiation: Emitting infrared radiation.
- Convection: Heat transfer to surrounding air.
- Conduction: Direct heat transfer through contact with more excellent surfaces.
- Evaporation: Heat removal through the evaporation of sweat.

Physical activity significantly increases the body's heat production. Light activities like walking can increase heat production to 300-400 W, while strenuous activities like running can boost it to over 1,000 W. Thermogenesis refers to the production of heat within the body, occurring through:

- **Non-shivering Thermogenesis:** Primarily mediated by brown adipose tissue, which burns fatty acids to produce heat.
- **Diet-induced Thermogenesis:** The heat produced following food consumption due to the energy required for digestion and assimilation.

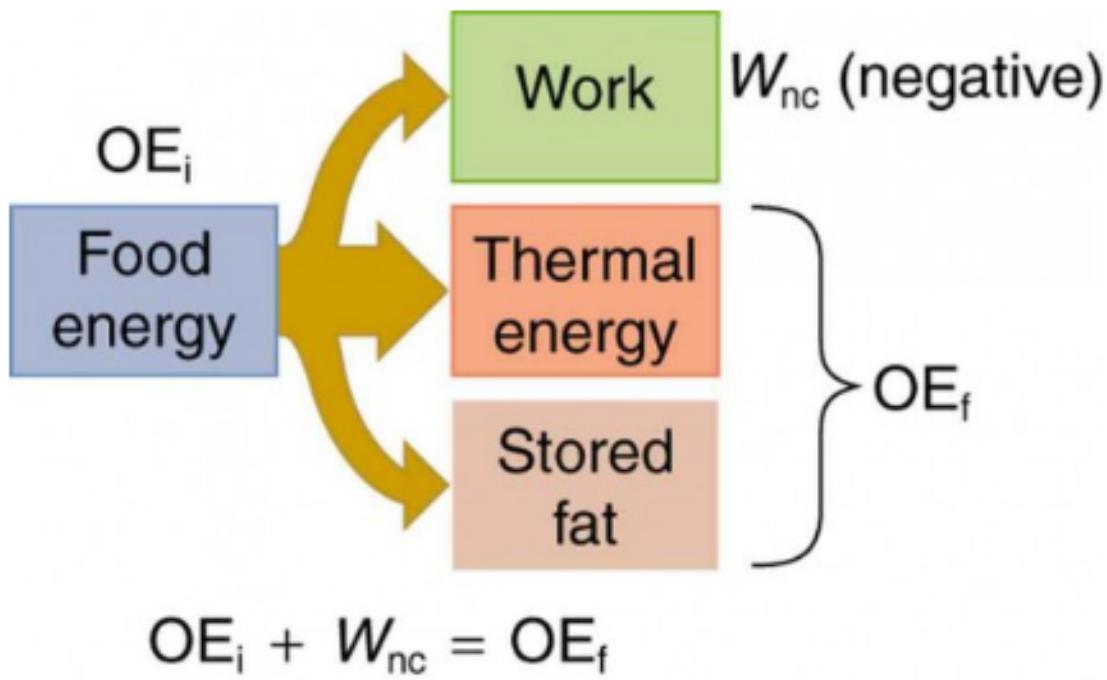


Figure 2.2. : Conversion of food energy into various forms, where thermal energy is released more than other forms [7].

Maintaining an optimal body temperature, around 37°C (98.6°F), is crucial for health. Deviations can lead to hyperthermia (overheating) or hypothermia (excessive cooling), which can have severe health implications. The human body is a dynamic system that produces heat energy essential for maintaining internal stability. Harnessing this energy presents technological challenges, particularly in terms of efficiency and practicality, but it also offers intriguing possibilities for innovations in wearable technologies and self-powered devices. Understanding the mechanisms of heat production and dissipation can guide the development of practical solutions to capture and utilize this energy.

2.3 Thermoelectric Generator

Thermoelectric generators (TEGs) convert temperature differences directly into electrical energy via the thermoelectric effect. A schematic of the thermoelectric generator is shown

in Figure 2.3. This phenomenon relies on three fundamental effects: the Seebeck effect, the Peltier effect, and the Thomson effect. The Seebeck effect, the primary mechanism in TEGs, generates an electric voltage when there is a temperature gradient across two different conductors or semiconductors. This voltage is produced as charge carriers in the material move from the hot side to the cold side. One of the significant advantages of TEGs is their lack of moving parts, contributing to their reliability and low maintenance requirements. They are instrumental in applications where converting waste heat into electricity is essential, such as in power plants and automotive systems. For instance, automotive thermoelectric generators (ATGs) enhance fuel efficiency by converting the heat from exhaust gases into additional electrical power. This process not only improves the vehicle's overall efficiency but also contributes to reducing fuel consumption and emissions. Although the efficiency of TEGs is generally lower than that of traditional heat engines, they offer several benefits, including compact size and the ability to function in harsh environments where mechanical systems might be impractical. This makes TEGs particularly valuable when other energy conversion methods are not feasible or practical. TEGs are also being explored for their potential in renewable energy systems. For instance, combining TEGs with solar concentrators can directly convert solar heat into electricity. Despite the current limitations in efficiency, this approach represents a promising avenue for renewable energy generation, particularly in off-grid and remote locations where conventional energy sources are unavailable. This potential offers hope for a future where sustainable energy solutions are more accessible and widespread [5][8]. Moreover, TEGs have practical applications in industrial settings with abundant waste heat. By installing TEGs in industrial processes, companies can recover waste heat and convert it into usable electricity, improving overall energy efficiency and reducing operational costs. This application is particularly relevant in steel manufacturing, glass production, and chemical processing, where high-temperature processes generate substantial amounts of waste heat. The potential for significant energy savings in these industries is inspiring. In summary, thermoelectric generators offer a unique and promising approach to energy conversion by directly transforming temperature differences into electrical energy. While their efficiency may be lower than that of conventional heat engines, the benefits of reliability, low maintenance, and the ability to operate in diverse environments make

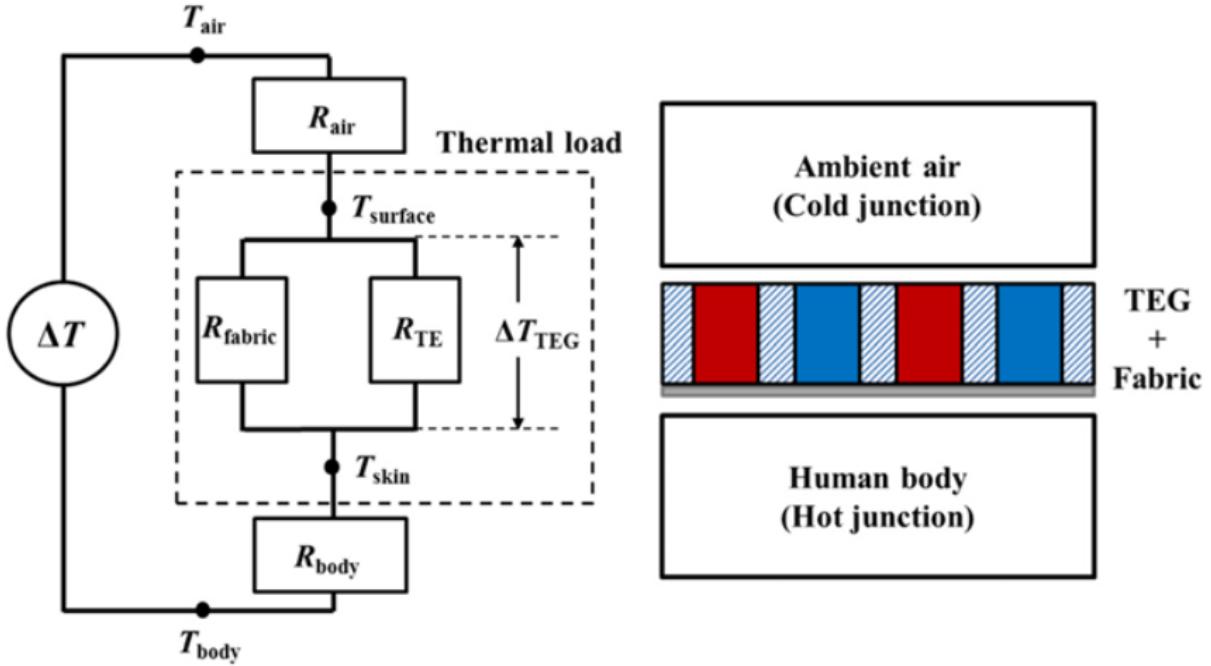


Figure 2.3. : Schematic of a Thermoelectric Generator [5]

them a valuable technology. Continued research and development in thermoelectric materials and device integration are essential for enhancing the performance and cost-effectiveness of TEGs, paving the way for broader adoption in various applications, including renewable energy systems, industrial waste heat recovery, and wearable technology.

In wearable technology, TEGs can harness energy from human body heat. These wearable TEGs are designed to be flexible and durable, allowing them to integrate seamlessly into clothing without impeding the wearers movement. A study by [5] showcased a wearable TEG (shown in Figure 2.4) that used dispenser-printed thermocouples embedded in a polymer-based fabric. This prototype was able to generate power from the temperature difference between the human body and the surrounding air, highlighting its potential for powering small electronic devices or sensors worn on the body. The design of wearable TEGs focuses on maximizing the temperature gradient between the skin (the hot junction) and the ambient environment (the cold junction). The study by [Kim et al.] demonstrated that the TEG's power output was influenced by the wearers movement, with higher voltages

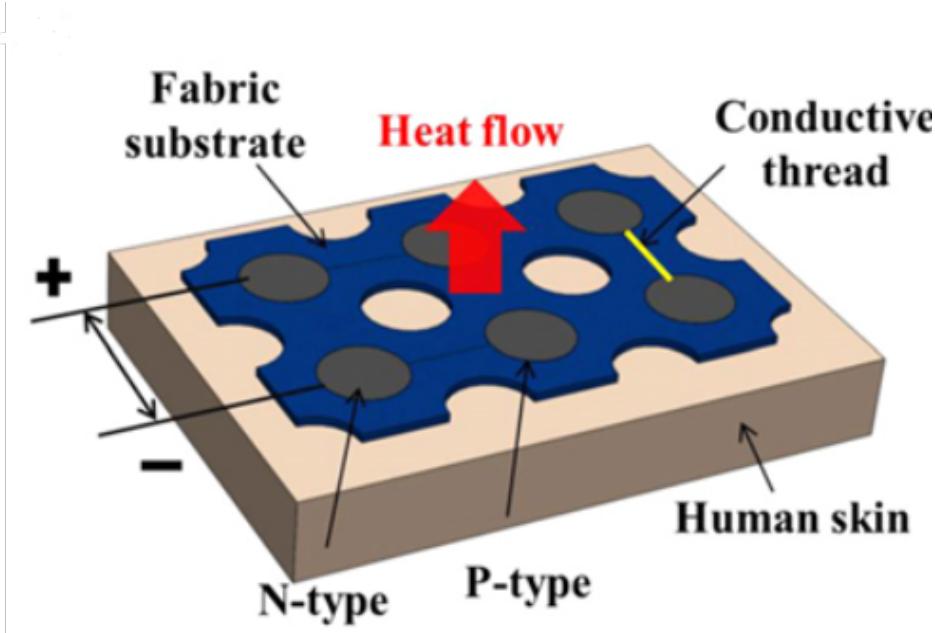


Figure 2.4. : Design of the wearable thermoelectric generator on the skin [5]

being maintained while walking compared to when stationary. This finding suggests that wearable TEGs could be particularly effective for active individuals, providing a continuous power source for wearable electronics. To enhance the efficiency and performance of TEGs, ongoing research is aimed at developing more effective thermoelectric materials. Innovations in material science, such as creating high-performance thermoelectric compounds and optimizing device architectures, are crucial for improving the conversion efficiency of TEGs. This ongoing research and development in TEGs instill optimism about the potential for future advancements and their impact on energy harvesting and sustainable power generation solutions.

3. RELATED WORK

3.1 Linear Charge Pumps Topologies

The voltage generated by other energy harvesting technologies is considerably lower, often about 100mV or less. Recent advancements in Charge Pump designs have led to the development of increasingly intricate topologies. These topologies aim to improve efficiency, reduce supply voltage requirements, minimize power consumption, and occupy a smaller physical space. Various varieties of charge pumps are available, but linear charge pumps are often utilized as topologies in low-voltage applications. Typically, current research combines one of these low-power structures with adiabatic design concepts. The linear charge pump is considered one of the most effective topologies for ultra-low voltage applications due to its ability to eliminate threshold voltage decreases, as seen in other topologies. An idea explored in this thesis is to leverage the intrinsic properties of FinFET technology. FinFETs provide several advantages, including reduced body effects, enhanced switching speeds, decreased threshold voltage, and improved power efficiency [9]. A lower threshold voltage is essential for achieving superior performance at lower supply voltages. The design of the Charge Pump system strategically utilizes these qualities, which will be discussed further in a subsequent presentation chapter 5 of the thesis. The Charge Pump employed in this design is categorized as a Linear Charge Pump with a two-stage structure. The linear charge pumps discussed in [2], utilize adiabatic gate control techniques provided by [10], which involve the addition of an external inverter level shifter to regulate the gate of the charge transfer switches. [11] was the pioneer in suggesting the virtual ground approach as a means to mitigate energy usage in Charge Pumps. Their efforts led to a 46% decrease in energy leakage in a 45nm process. A recent experiment conducted in [12] demonstrates that manipulating the Charge Transfer Switches' body potential can decrease the device's threshold voltage, enabling the Charge Pump to operate at lower voltages. [13] introduced an adiabatic Linear Charge Pump that can efficiently convert 390mV to 850mV with a remarkable efficiency of 59.2%. However, its maximum output current is limited to 250nA. A comprehensive search was conducted to locate FinFET charge pumps that resemble this design. However, a solitary instance was discovered and is showcased in [14]. The study in [14] demonstrated the

ability to convert an input voltage of 96mV to an output voltage of 475mV. However, this conversion was only achieved with a low load of 47.5nA. As a consequence, the efficiency of the conversion was 42.9%. Additionally, the implementation required several off-chip inductors, which are usually undesirable due to their high size. The study described in [15] developed a cross-coupled Charge Pump that achieves a remarkable conversion rate of 70mV to 1.25V, operating at a highly efficient rate of 58% and delivering a substantial output current of $12\ \mu\text{A}$. These results are pretty impressive. Nevertheless, a 10nF capacitance located outside the semiconductor was utilized to achieve these outcomes. This effort aims to achieve a shorter rise time for the designs being compared. The implemented design utilizes linear charge pump topologies that belong to the same category as [2], [10], [13], [14], and [16].

Figure 3.1 displays the primary block representation of the suggested design, which will be often referred to throughout this study. Before delving into each block's specific details, it is provided in advance to facilitate a more thorough understanding. The diagram illustrates that an energy harvester supplies the power source, V_{IN} , to the remaining circuits. The sequence in which this thesis offers the information on the particular blocks and circuits inside Figure 3.1 can be perceived as proceeding from left to right. In Chapter 6, the Oscillator is introduced initially, followed by the pump drivers and the charge pumps.

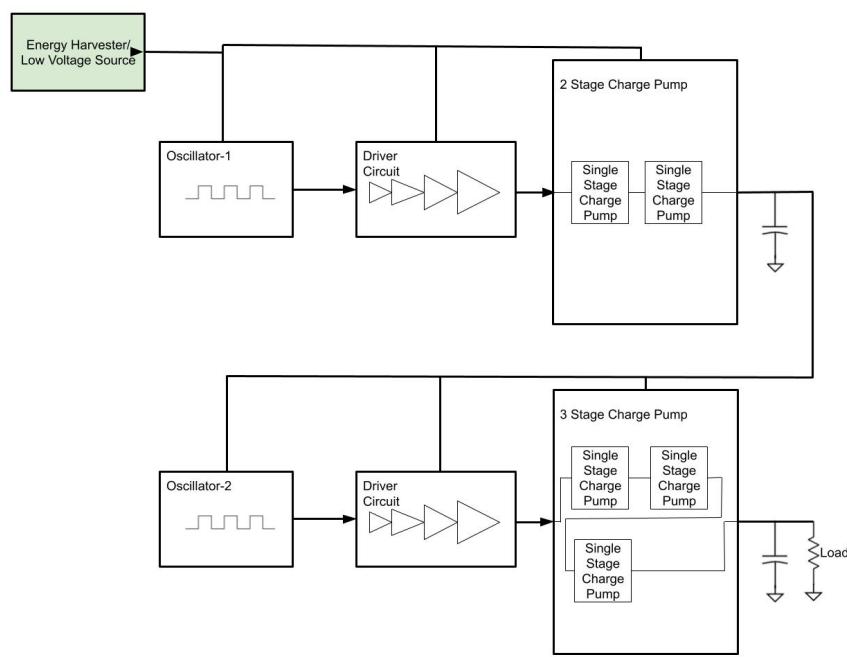


Figure 3.1. : High-level design of the Charge Pump proposed in this work

4. FINFET DEVICES, OPERATION AND MODELING

4.1 Metal-Oxide-Semiconductor Field-Effect Transistor

Metal-oxide-semiconductor field-effect Transistors (MOSFETs) are a cornerstone of modern electronics, widely utilized in analog and digital circuits. These devices are essential due to their high efficiency, scalability, and performance in various applications, from power management to complex integrated circuits. A MOSFET comprises three central regions: the source, the drain, and the gate, with an insulating layer of oxide between the gate and the semiconductor material, typically silicon. There are two types of MOSFETs: n-channel (NMOS) and p-channel (PMOS), differentiated by the type of charge carriers that flow through them. In NMOS, electrons are the charge carriers, whereas in PMOS, holes are the charge carriers. The conductivity of the channel between the source and drain is influenced by the electric field produced when a voltage is supplied to the gate. In an NMOS transistor, a positive voltage applied to the gate attracts electrons towards the gate, forming a conductive channel. Conversely, in a PMOS transistor, a negative voltage repels electrons, creating a channel through which holes can move. The ability to control this channel with gate voltage allows the MOSFET to function as a switch or amplifier.

4.2 Fin Field-Effect Transistor

Field-effect transistors with fin-like shapes are referred to as FinFETs. Because of its fin-shaped body, which is silicon, a transistor is distinguished as a drain/source node. "Field-effect" refers to how an electric field affects a material's conductivity, much like a MOSFET. In contrast to planner MOSFET, a FinFET is a non-planar device. Because it has a third dimension, the device is 3D. By expanding the width of the channel or the height of the Fin, the drive current of the FinFET can be raised. By creating parallel multiple fins joined together, we can also improve the device driving current. It suggests that variable channel width is not achievable since a FinFET's channel width is always a multiple of the fin height. A large leakage current results from reducing the gate length (L_g) below 45 nm and below 28 nm; the leakage is enormous, and the transistor is rendered worthless.

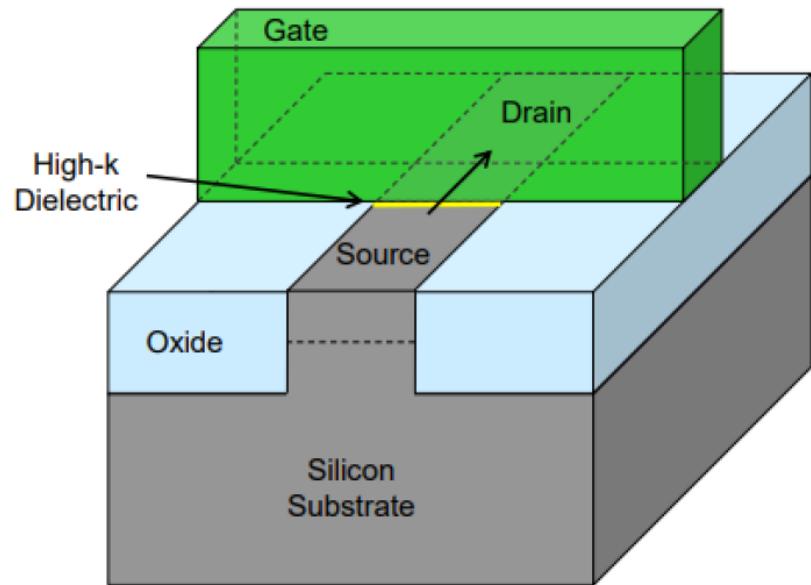


Figure 4.1. : Traditional Planar MOSFET Structure[17]

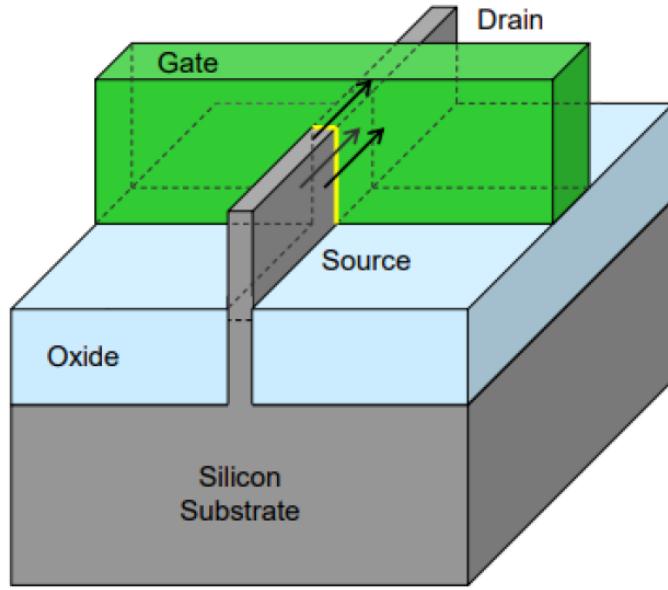


Figure 4.2. : Single Fin FinFET Device [17]

Therefore, FinFETs came into action. Because fin thickness affects the device's subthreshold swing and short-channel behavior, the fin thickness is a crucial parameter. The subthreshold swing gauges a transistor's effectiveness. Compared to traditional MOSFET technology, FinFET devices have superior short-channel performance, faster switching times, and a greater current density. The first 22nm FinFET to be used commercially was introduced in 2012. The FinFET architecture was later enhanced, leading to increased performance and decreased area. Increasing the fin height to get a higher driving current is one benefit of the 3D aspect of the FinFET. However, the leakage problem reappears as we move to a lower technological node, such as below the 5nm node. Threshold flattening, a rise in power density, and thermal dissipation are just a few of the complications that result from this. Heat can quickly collect on the fins of a FinFET structure, making it less effective in dissipating heat.

The FinFET devices used throughout this study are sourced by using the ASAP7 7nm Process Design Kit (PDK), which was collaboratively produced by Arizona State University

and ARM Ltd. specifically for academic applications. This PDK is a practical implementation that employs the assumptions made with respect to the 7nm technology node. It is not specifically associated with any particular foundry. [3]. It is important to note that these devices should not be mistaken for devices that are 7nm in length. The term "7nm" actually refers to the width of a fin on one of these devices. Figure 4.2 displays the complete arrangement of a FinFET including a solitary fin. The resemblance of the constituents between the FinFET seen in Figure 4.2 and the planar MOSFET illustrated in Figure 4.1 is rather evident. Nevertheless, the connection between the silicon gate and the substrate is fundamentally distinct. Currently, there is an interaction between three fins, as opposed to only one. This enhances channel regulation, allowing for the smooth passage of electric current. The conductive channel is now oriented vertically and could be densely arranged, which is one of the most notable advantages compared to a standard planar MOSFET. Figure 4.3 showcases a device using three fins, emphasizing an additional advantage of the FinFET design. Increasing the number of fins enhances the drive strength. Based on observations, this phenomenon causes an expansion of the device, allowing a greater amount of electric current to flow through. The ASAP7 PDK allows the designer to adjust the device width by modifying the number of fins in the parameter file. The density of transistors on silicon devices has experienced a large rise as a result of the quick driving strength enhancement provided by FinFETs. The semiconductor industry may partially fulfill Moore's Law, which forecasts that the quantity of transistors on a compact integrated circuit would almost double every two years, with the assistance of FinFETs. [9]. Increasing the vertical height of the fins is an alternative method to augment the driving strength of the FinFETs, as opposed to including more fins. The gate length is aggressively decreased to about 1214 nm when the size of the standard Planar MOSFET is reduced to a comparable 7 nm node [18]. Reduced gate length will result in more short channel effects, raising leakage current and, in turn, raising static power consumption. For this reason, FinFETs are a popular choice, as relative scaling is possible without significantly reducing the device's gate length. Due to the channel's more excellent controllability, FinFETs can also lower the amount of leakage current. The FinFET outperforms the planar MOSFET by 18% at a 1V power supply and by 37% with a 0.7V power supply [9]. This inherent reduction in power usage at lower power supply

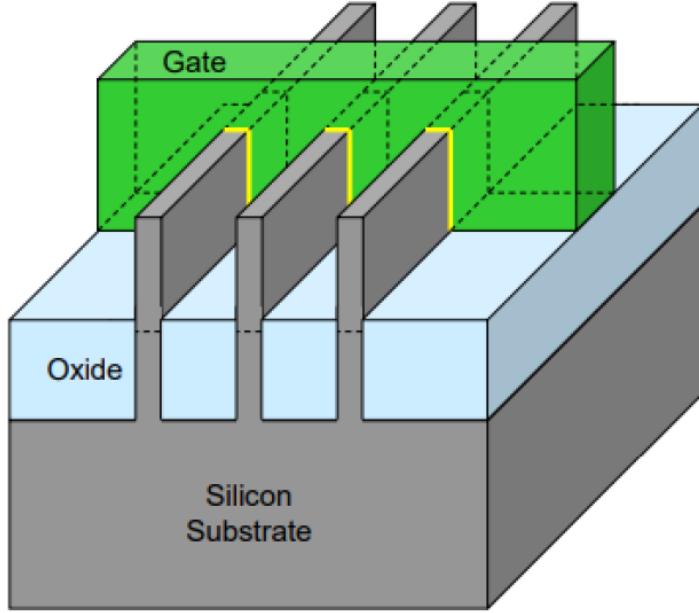


Figure 4.3. : Tri-Fin FinFET Device [17]

levels is a promising advantage. However, the altered design flow and the need for specialized, costly equipment in FinFET production pose significant challenges. Overcoming these challenges could lead to a broader adoption of FinFET technology, potentially revolutionizing the semiconductor industry. Figure 4.4 shows a genuine image of a planar MOSFET. Figure 4.5 displays a genuine image of the FinFET that was captured using extremely powerful scanning electron microscopes. FinFET devices are excellent choices for static random access memory (SRAM) architectures and low-voltage energy harvesting applications due to the benefits above. Research and design work on FinFET SRAM cells have been extensively undertaken [19], [20], [21], [22]. However, without a FinFET Charge Pump, an entire SRAM IC could not be constructed. A thorough search has been done to find specific FinFET CPs for any application. It was found that these gadgets' advantages exceed their proportional drawbacks. For all of the circuits provided subsequently in this work, this design will therefore use the ASAP7 FinFETs, as the presented design is better suited for energy harvesting applications; some minor adjustments could make this a feasible design for an SRAM IC.

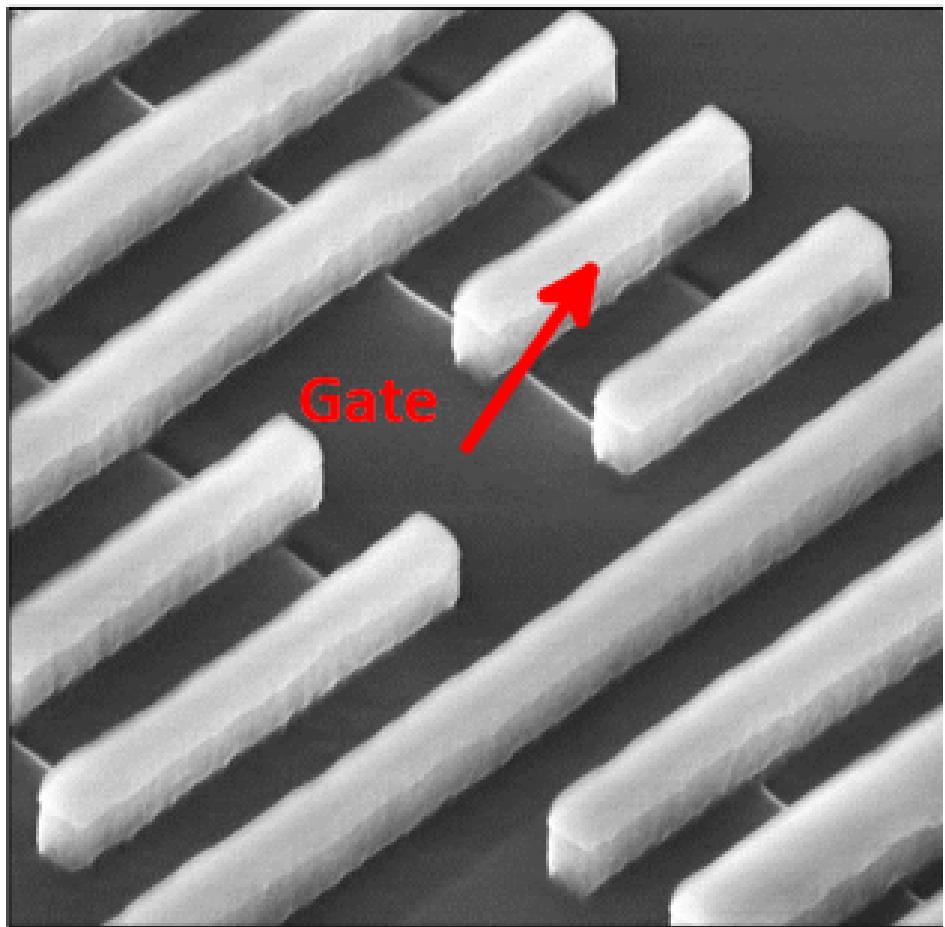


Figure 4.4. : Planar Transistor[[17](#)]

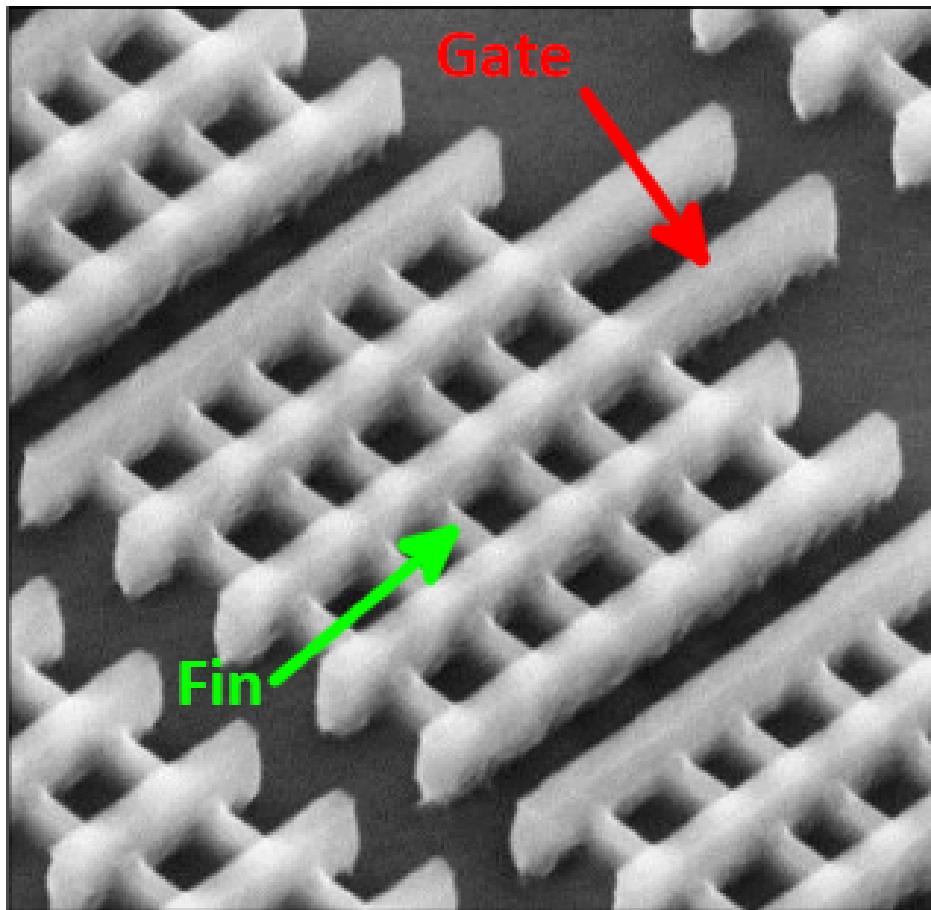


Figure 4.5. : Tri-Fin FinFET Transistor [17]

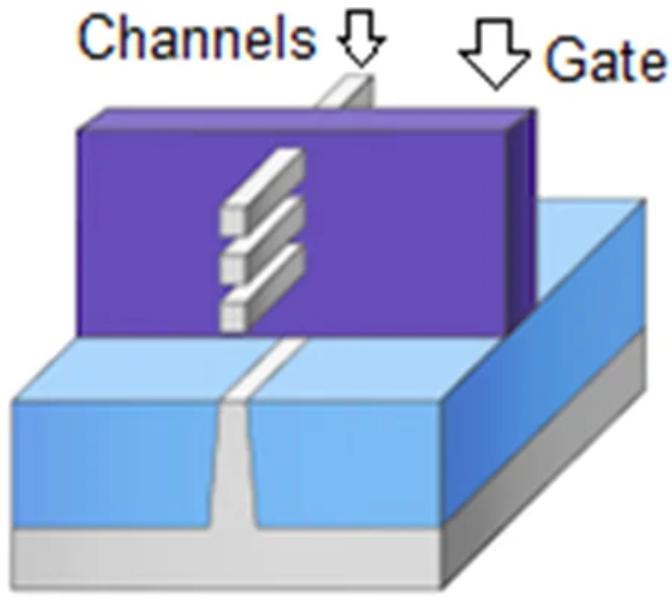


Figure 4.6. : GAAFET Structure

4.3 Gate-All-Around Field-Effect Transistor

The three-dimensional layout created a construction where the gate is entirely wrapped, as shown in Figure 4.6. The Gate-All-Around FET (GAAFET) in this structure has nanowires or nanosheets. The demand for low-power applications, high packing densities, maintenance of high gate sensitivity, individual or bulk (arrayed) fabrication capability, scalability, and, most recently, investigation of ballistic carrier transport behavior for potential high-performance electronic devices make nanowire FETs necessary. Even bandgap engineering of the FET channel is possible with nanowire FETs, enabling designers to optimize device performance. There are several things to consider when improving an FET device. Low drive voltage operation, high carrier mobility/speed, low leakage current, low power operation, high transconductance (gate sensitivity), and good subthreshold properties are a few of them. Other qualities include low threshold voltage and low series resistance. In GAAFET, additional areas are not required to improve the device speed. The footprints of the FinFETs can be used for the GAAFETs as well.

4.4 FinFET modeling in Cadence

Cadence Virtuoso is a comprehensive suite for custom IC design that provides robust modeling and simulating tools, enabling designers to leverage these benefits effectively. In Cadence Virtuoso, modeling of the FinFET devices begins by importing the appropriate technology files and process design kits (PDKs). These files contain the parameters and models specific to FinFET technology, ensuring accurate simulations. ASAP7 PDK files are used in this work. A new library is created in Virtuoso to organize the FinFET models and associated design files. Ensure that the library references the correct technology file. Define the FinFET device parameters such as fin height, width, gate length, and doping concentrations. These parameters are crucial for capturing the physical characteristics and behavior of the FinFET. In the ASAP7 PDK file, the number of fins can be varied, which changes the device's width. In Cadence Virtuoso Schematic Editor, schematics are designed, and components are added to the schematic editor from an instance where several electronic components will be available for creating the circuit. Conduct transient simulations to study the behavior of the designed schematic. This analysis helps understand the dynamic performance, including rise/fall times, switching speeds, and voltages concerning time. The schematic simulation is done by launching the ADE file. All kinds of simulations are done in this file.

5. CHARGE PUMPS, ARCHITECTURE AND MATHEMATICAL MODELING

5.1 Operation of a Charge Pump

An analysis of the Dickson Charge Pump [24] can provide a clear understanding of the fundamental concepts of the Charge Pump circuit. The Dickson Charge Pump, seen in Figure 5.1, consists of several diode-connected NMOS transistors arranged in N stages, together with a series of capacitors that are controlled by nonoverlapping oscillator phases ϕ_1 and ϕ_2 . The clock phases alternate between $0V$ and V_ϕ facilitating the transfer of charge from the power source to the output capacitor C_{out} . This is achieved by charging and discharging the chain of capacitors during each half-clock cycle. The disparity between the voltages of the nodes V_N and V_{N+1} can be expressed, as seen in Figure 5.1:

$$\Delta V = V_{N+1} - V_N = V'_\phi - V_{TH} \quad (5.1)$$

where V'_ϕ represents the voltage swing at each node caused by the capacitive coupling from the oscillator [25]. When the clock transitions from a low state to a high state, assuming a long clock cycle, the linked node is incremented by V'_ϕ . V'_ϕ is determined by the charge that

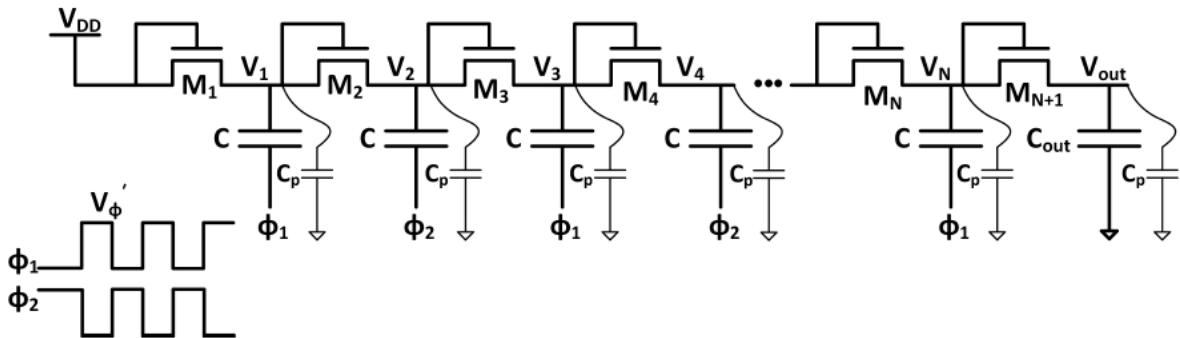


Figure 5.1. : Dickson Charge Pump [23]

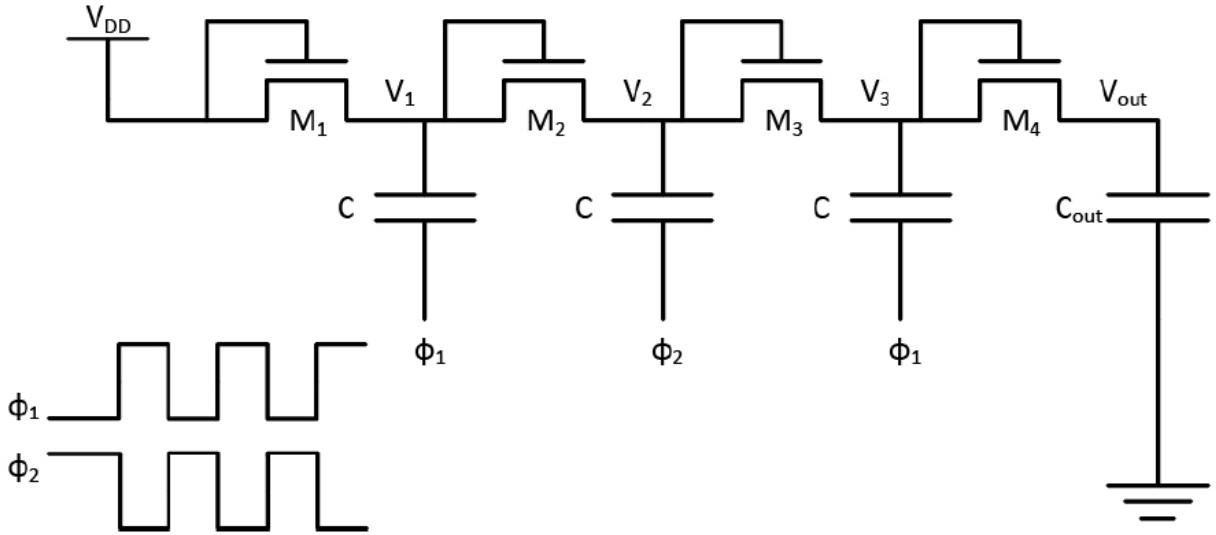


Figure 5.2. : 3 Stage Dickson Charge Pump [23]

is split between the coupling capacitance C and parasitic capacitance C_p . This rise is due to the fundamental fact that the voltage across a capacitor cannot change instantly.

$$V'_\phi = \frac{C}{C + C_p} V_\phi \quad (5.2)$$

To demonstrate the functioning of the Dickson Charge Pump, consider a basic scenario with 3 steps as seen in Figure 5.2. Let's consider a starting circumstance where ϕ_1 is low level and ϕ_2 is high level. Given a lengthy clock cycle, when the signal ϕ_1 is low state, the transistor M_1 will be activated, causing the voltage at node N_1 is changed to:

$$V_1 = V_{DD} - V_{TH} \quad (5.3)$$

where V_{TH} is the transistor's threshold voltage. Next, when ϕ_1 is in high state and ϕ_2 will be in low state, the voltage at N_1 is calculated to be:

$$V'_1 = V_{DD} - V_{TH} + V'_\phi \quad (5.4)$$

Due to the oscillator pulse switching, M_1 is deactivated, preventing reverse current flow into the power supply. M_2 will continue to operate until the voltage at N_2 is charged to:

$$V_2 = V_{DD} - 2V_{TH} + V'_\phi \quad (5.5)$$

Thus, when ϕ_2 goes from low state to high state, N_2 is boosted up to:

$$V'_2 = V_{DD} + 2(V'_\phi - V_{TH}) \quad (5.6)$$

This same procedure is repeated for the 3rd stage to give:

$$V'_3 = V_{DD} + 3(V'_\phi - V_{TH}) \quad (5.7)$$

Subsequently, M_4 functions as an isolating diode, separating the 3rd stage from the output. Therefore, in optimal circumstances, the highest achievable voltage produced by this third stage Charge Pump is:

$$V_{max} = V_{DD} - V_{TH} + 3(V'_\phi - V_{TH}) \quad (5.8)$$

The end result can be extended to provide the highest output voltage following N steps:

$$V_{max} = V_{DD} - V_{TH} + N(V'_\phi - V_{TH}) \quad (5.9)$$

Substituting equation (5.2) into (5.9) provides the maximum possible voltage that can be produced by the charge pump:

$$V_{max} = V_{DD} - V_{TH} + N \left[\left(\frac{C}{C + C_p} \right) V_\phi - V_{TH} \right] \quad (5.10)$$

It is notable that equation (5.10), which depicts the fundamental functioning of a charge pump, is derived from an ideal situation. Typically, a load is connected to the output stage, which functions as an ultra-low power device by drawing current from the Charge Pump. The charge transmitted by each diode during a clock period, Q_s . The clock frequency f time

the clock period, Q_s , is the total current that the Charge Pump can produce during a single clock period.

$$I_{\text{out}} = Q_s \cdot f = V_L(C + C_s)f \quad (5.11)$$

V_L represents the amount of voltage that is lost in each stage in order to provide the average load current. Hence, when a suitable load is connected to the pump output, a more accurate output voltage may be obtained by combining Equations (5.10) and (5.11) as follows:

$$V_{\text{out}} = V_{DD} + N \left[\left(\frac{C}{C + C_p} \right) V_\phi - V_{TH} - \frac{I_{\text{out}}}{(C + C_s)f} \right] - V_{TH} \quad (5.12)$$

5.2 Various Charge Pumps

Charge pumps are not just components of a circuit, but essential parts of energy harvesting, particularly in medical equipment. These devices are designed to efficiently convert energy from various sources, including movement and body heat, into electrical power. Charge pumps are especially beneficial because they raise low input voltages to higher levels needed by implants, medical sensors, and health monitoring devices. This unique feature ensures that specific medical devices continue to function without the need for frequent battery changes, thereby improving patient lifetime and convenience. Charge pumps are crucial in developing self-sustaining medical technology, as they optimize power management. In this section, we will explore a few important charge pump technologies.

5.2.1 Cross-coupled Charge Pump

A cross-coupled charge pump functions as a voltage multiplier, relying primarily on capacitors for energy storage and transfer. The fundamental idea is to move the charge between capacitors by raising the voltage level step-by-step. The term "cross-coupled" pertains to the specific arrangement of transistors within the circuit to facilitate effective charge transfer and voltage enhancement. This design generally features two branches of capacitors, as shown in Figure 5.3, and switches alternately activated by clock signals. This alternating activation ensures a continuous process of charge pumping and voltage amplification. One kind of cross-

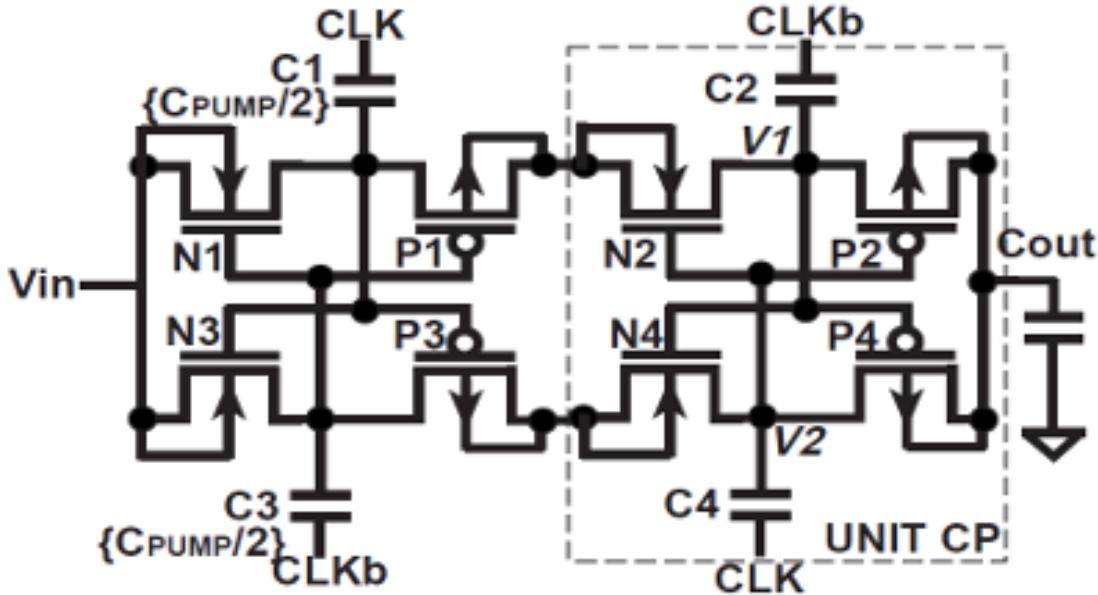


Figure 5.3. : Cross-coupled Charge Pump [26]

coupled Charge Pump is a cross-connected NMOS charge pump shown in Figure 5.4 that utilizes NMOS transistors and capacitors to transfer and boost charge sequentially. The fundamental principle involves using clock signals to alternately switch the transistors, enabling charge transfer between capacitors. This sequential switching results in a step-wise increase in voltage, effectively multiplying the input voltage to a higher level. A cross-connected NMOS charge pump is used in this design.

5.2.2 Fibonacci Charge Pump

The Fibonacci charge pump is a sophisticated type of charge pump that leverages the principles of the Fibonacci sequence to optimize voltage boosting. This innovative design in Figure 5.5 is particularly beneficial in applications requiring efficient voltage multiplication with minimal components. It is found in integrated circuits (ICs), power management systems, and other electronic devices. The Fibonacci charge pump operates based on each number in the Fibonacci sequence, which is equal to the sum of the two numbers that came before it (e.g., 0, 1, 1, 2, 3, 5, 8, etc.). Using this sequence, the charge pump can achieve

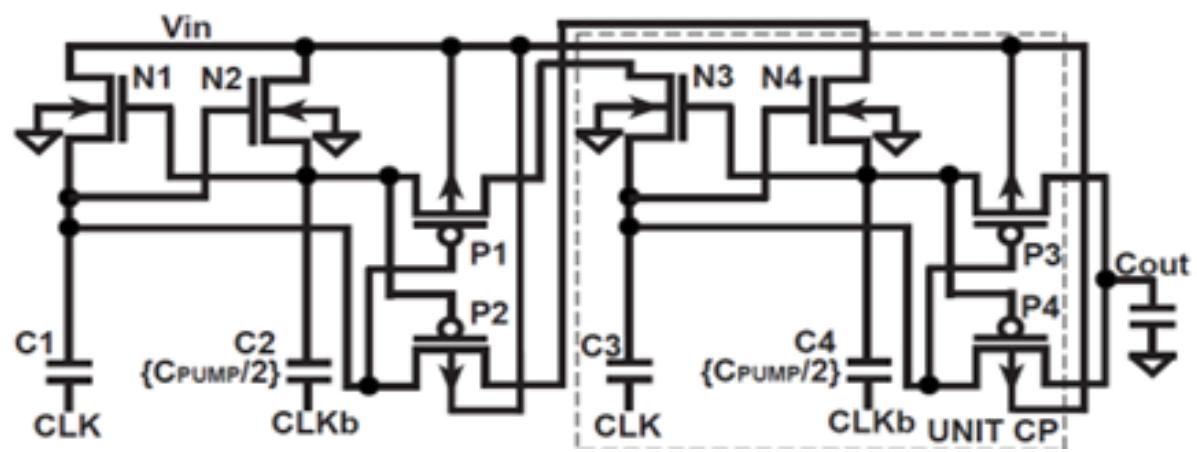


Figure 5.4. : Cross connect NMOS Charge Pump[26]

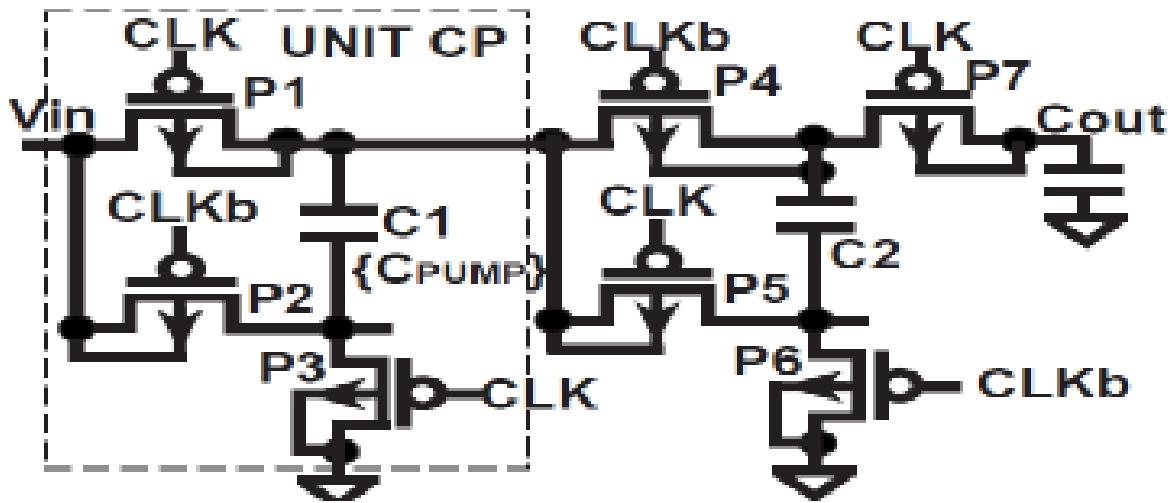


Figure 5.5. : Fibonacci charge pump [26]

efficient voltage boosting with fewer stages than traditional charge pumps. This design minimizes the number of components required while maintaining high efficiency. However, the Fibonacci Charge Pump is a nonlinear charge Pump that cannot be used in ultra-low voltage applications.

6. INTEGRATED CIRCUIT CHARGE PUMP

To validate this two-level Charge Pump's design shown in Figure 6.1, schematics, theory, and waveforms will be used to discuss the circuits' components. Both levels have the same components.

6.1 CMOS Inverter

The inverter is a vital and crucial circuit, since it serves as a basic component in the construction of any integrated circuit. Within this design, inverters are employed to generate and disseminate the oscillator, general purpose buffers, and the primary Charge Pump core

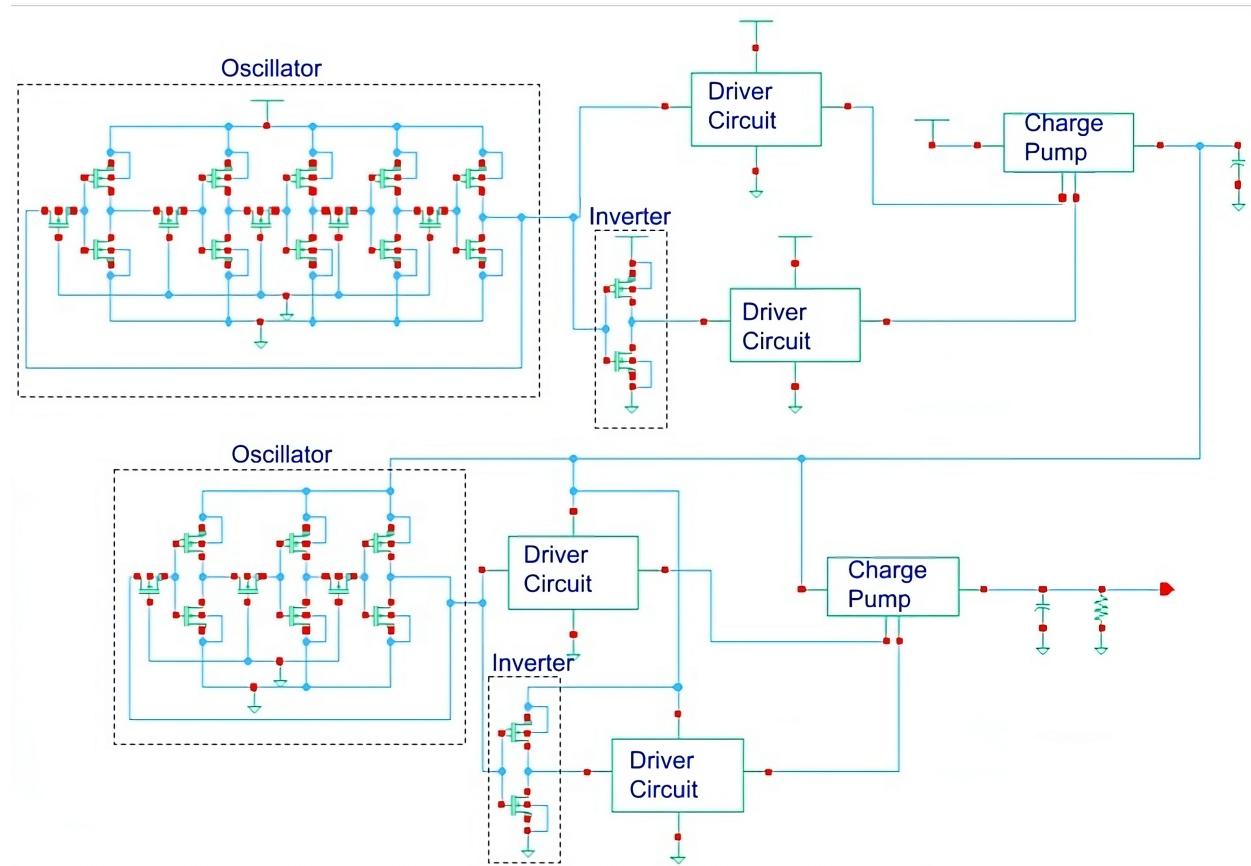


Figure 6.1. : Schematic of a 2-level Charge Pump

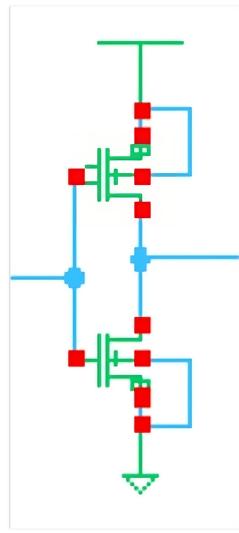


Figure 6.2. : Inverter Schematic [23]

drivers. Their purpose is to ensure the accurate logic output for both the comparator and the feedback loop. The fundamental operational concept of the inverter is that its output will be the opposite of its input. Despite utilizing transistors from the ASAP7 7nm PDK that employ FinFET technology, the functionality of these transistors is comparable to that of conventional CMOS devices. The inverter consists of a single P-type device serving as the pull-up circuit and a single N-type device serving as the pull-down network, as seen in Figure 6.1. A notable feature among these FinFET semiconductors is their deviation from the conventional practice of making the PMOS device twice as wide as the NMOS device. The ASAP7 7nm PDK transistors have a 10:9 ratio of NMOS to PMOS driving. This statement refers to the observed pattern in the transition of leading foundries from 32nm planar technology to 16 and 14 nm FinFETs. It suggests that the process of obtaining PMOS strain is relatively simpler in the latter. The quantity of fins directly defines the breadth of the device. The following schematics assume that all devices without labels are SLVT and have fins that vary based on level and component. An attractive characteristic of these FinFET devices is their ability to challenge conventional knowledge by designing the PMOS device to have twice the width of the NMOS device. The NMOS to PMOS driving ratio for the ASAP7 7nm PDK devices is 10:9. According to observations made for major foundries, it is easier to create PMOS strain in FinFETs at 16nm and 14 nm compared to 32 nm planar technology [3]. The number of fins determines the device's breadth. It is presumed that all unlabeled devices in the following schematics are SLVT and have fins based on the component and level.

6.2 Oscillator

This section will discuss the oscillator circuit design. The oscillators use inverters as their primary source of oscillations. Clocks, timers, signal generators, and many other electronic systems use inverter oscillators because of their simplicity, dependability, and ease of integration. Phase shift and feedback are two main working principles of an inverter oscillator. Essentially, a circuit that can produce a complete phase shift of 360 degrees (or 0 degrees) around the loop and a loop gain of one or more is needed to operate an oscillator. This

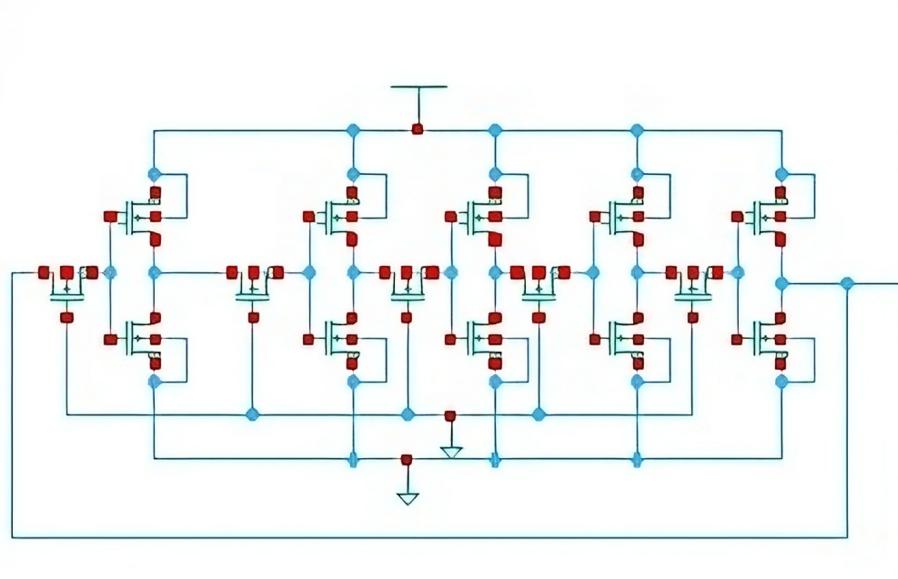


Figure 6.3. : 5-stage oscillator for level-1

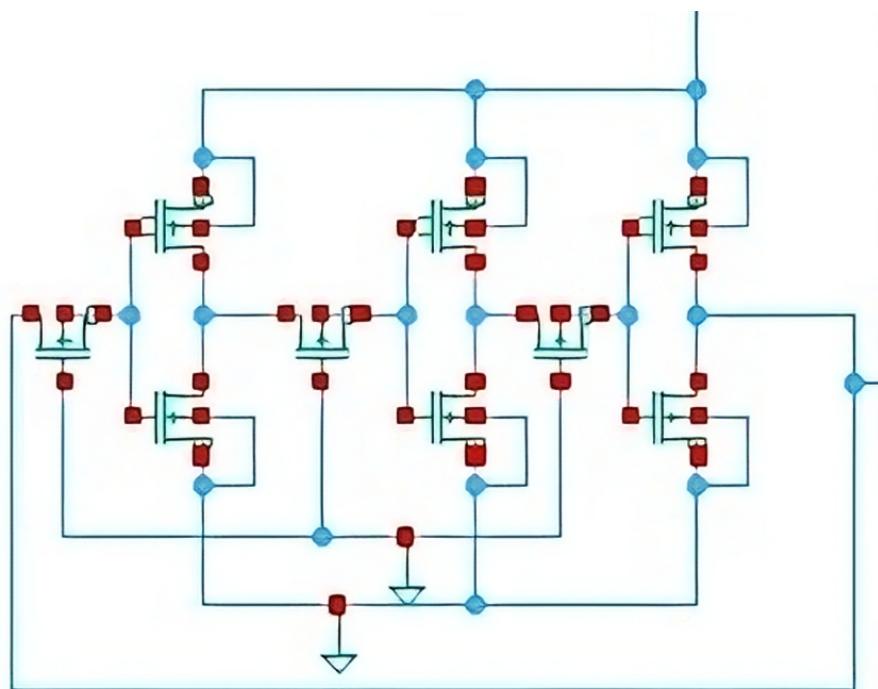


Figure 6.4. : 3-stage oscillator for level-2

is accomplished via inverter oscillators, which use an odd number of inverters coupled in a feedback loop, each of which shifts phase by 180 degrees. The oscillator, a pivotal circuit design component, is explicitly designed to achieve the required frequency. In this case, a two-phase, non-overlapping oscillator was intended. It features an inverter-based oscillator with NMOS LVT transistors between the inverters illustrated in Figure 6.3 and Figure 6.4 for level 1 and level 2 respectively. The NMOS LVT transistors determine the circuit's time constant, thus controlling the frequency of the oscillations. The output will be two non-overlapping clock pulses, CLKA and CLKB, where CLKB is generated by placing an inverter to produce a non-overlapping clock pulse. Varying the oscillator parameters allows the charge pump to achieve an optimum frequency, demonstrating the precision and control in the design. This design incorporates two oscillators, one for each level. Level 1 contains a 5-stage oscillator, while level 2 contains a 3-stage oscillator.

6.2.1 Optimum Pumping Frequency

The precision and control in the design of the oscillator are demonstrated by the ability to vary its parameters to achieve an optimum frequency. This showcases the engineering skill involved and keeps the reader engaged in the technical details of the design. Equation (6.1) gives the oscillator frequency, providing a comprehensive understanding of its operation.

$$f = \frac{I_s}{2 \cdot N \cdot V_{IN} \cdot C_f} \quad (6.1)$$

From equation (1) I_s , N , V_{IN} , and C_f are 5.9nA, 5, 85 mV, and 1.8fF, respectively, which generates 3.93 MHz of frequency for level 1. Similarly, for level 2 I_s , N , V_{IN} , and C_f are 5.9nA, 3, 164.6 mV and 0.1fF, respectively to get 1.55 MHz.

6.3 Driver Circuits

A voltage drop may occur when the clock pulses from the oscillator are directly connected to the charge pump circuit. Driver circuits are inserted between the oscillator and the charge pump to prevent this issue. These circuits serve as intermediaries, ensuring that low-power

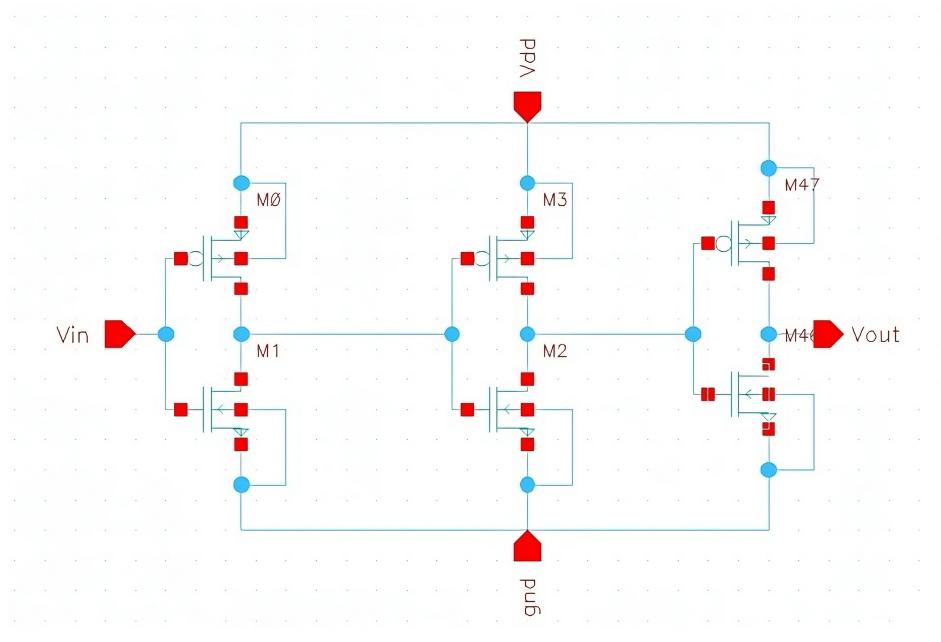


Figure 6.5. : Level-1 Driver circuit

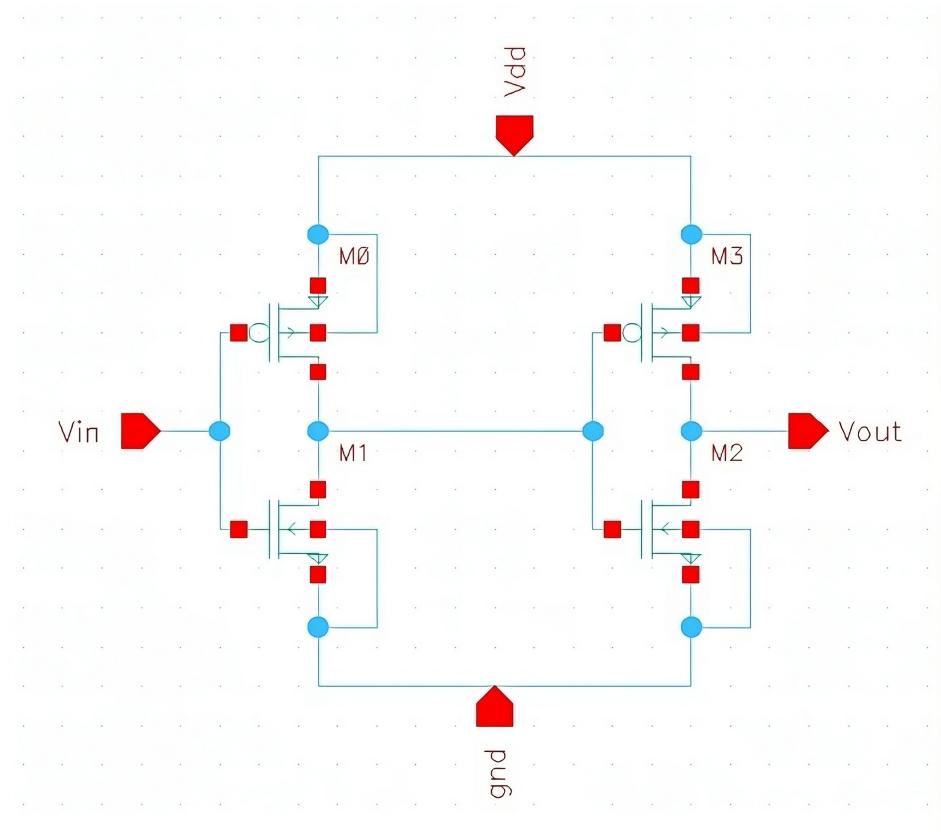


Figure 6.6. : Level-2 Driver circuit

control signals are effectively amplified to drive high-power devices. This article delves into driver circuits' principles, design, operation, and applications, underscoring their crucial role in modern electronics. Driver circuits receive low-power input signals and amplify them to levels suitable for driving high-power devices. Depending on the load's requirements, the amplification process can involve voltage, current, or both. Driver circuits amplify the input signal to a level that can effectively control the target device. Often, driver circuits provide electrical isolation between the control circuitry and the high-power device, protecting sensitive components from potential damage. Driver circuits match the impedance between the control signal source and the load to ensure maximum power transfer and efficient operation. Driver circuits employ buffers to manage the increase in the size of transistors. For FinFET devices, the size can vary by increasing the fins. In level 1, three buffers are used, as shown in Figure 6.5, while in level 2, only two buffers are used, as illustrated in Figure 6.6. The use of three buffers in level 1 is due to the larger size of the charge transistor compared to level 2 transistors. The size of the last buffer of the driver circuit must be comparatively larger than the size of the charge pump transistor to avoid voltage drop. Accurate sizing is crucial, as increasing the transistor sizes results in larger current leakage.

6.4 Charge Pump Circuit

This design uses a charge pump circuit with cross-connected NMOS cells, the same as in [15]. In level 1, the 2-stage charge pump is used, as shown in Figure 6.7, while a 3-stage charge pump is used, as shown in Figure 6.8 in level 2. A 2-stage charge pump is designed in the first level because the transistors are much larger than those of level 2 transistors. If the transistor sizes are large, this decreases the charge pump's efficiency. Factors affecting the efficiency include leakage current and the capacitance in the transistor. SLVT transistors are used in designing the charge pump because the threshold voltage is very low. With two-phase non-overlapping clock signals, the transistors are turned ON and OFF depending on the clock pulse provided to the capacitors. This helps to transfer the voltage from one capacitor to the other, which allows multiplying the input voltage supplied to the charge

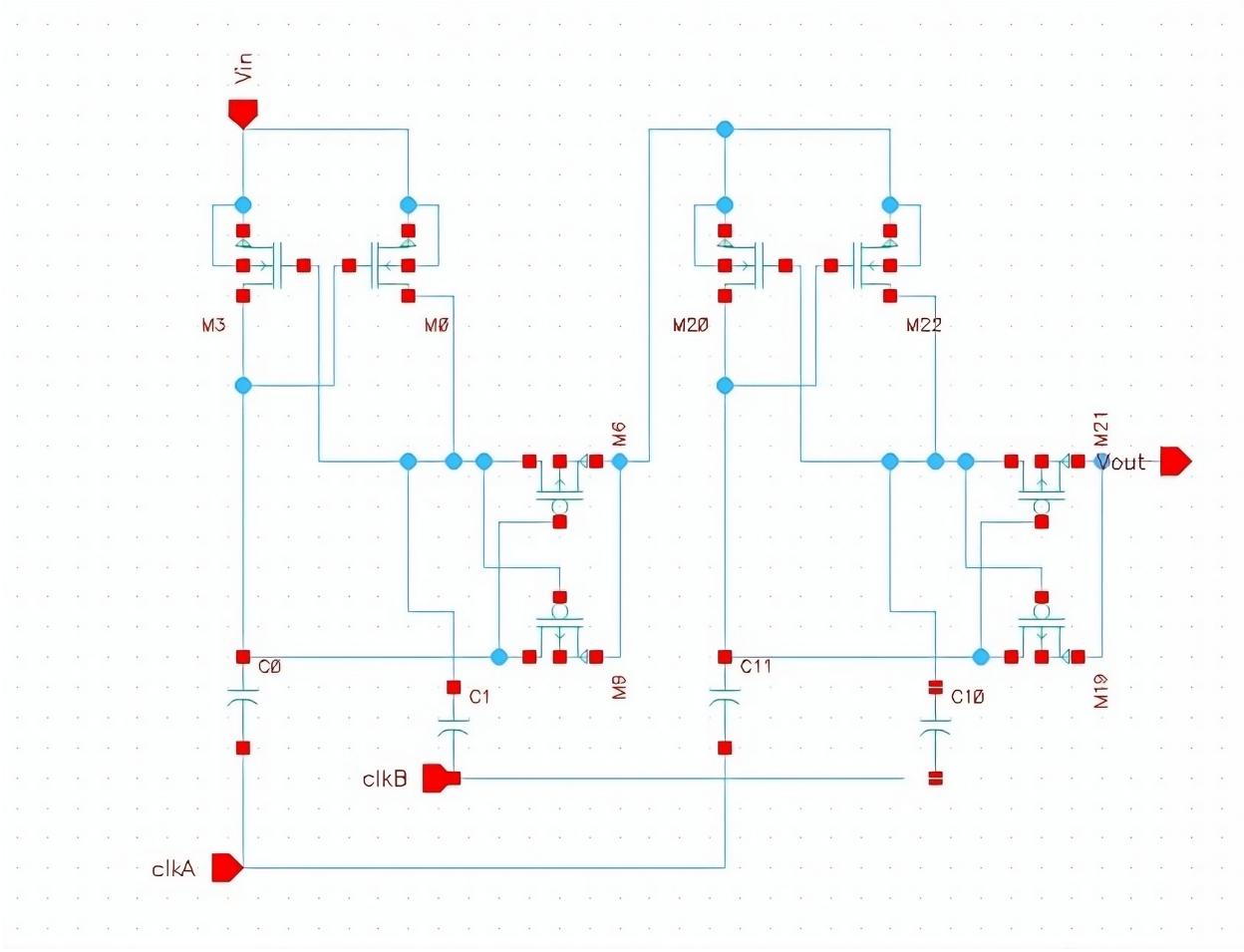


Figure 6.7. : Level-1 two-stage Charge Pump

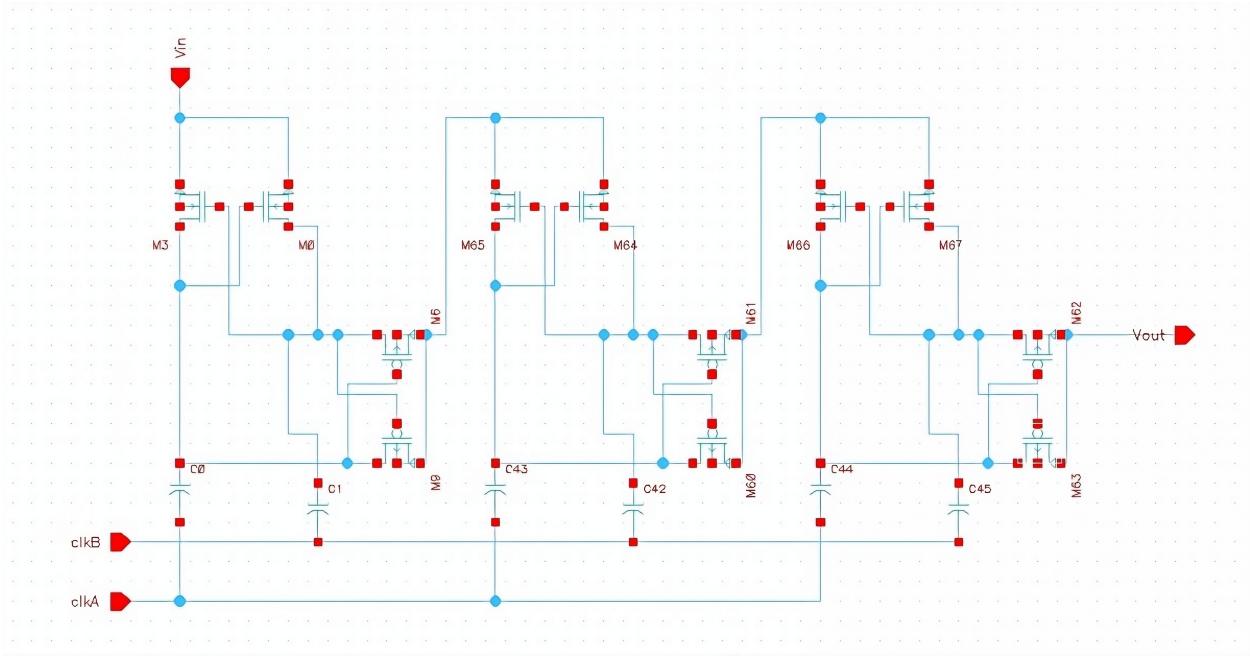


Figure 6.8. : Level-2 three-stage Charge Pump

pump. The size of the capacitor is another factor affecting the output voltage gain. In a cross-connect NMOS charge pump, input voltage gets multiplied by the number of stages in the charge pump, but the number of stages of the charge pump will be limited depending on the efficiency of the transistor switches. The estimated value of the output voltage at the N-th stage may be determined by

$$V_N = (N + 1)V_{DD} - \Delta V \quad (6.2)$$

Where ΔV denotes the losses caused by the parasitic leakage current and the voltage drop across the PMOS Charge Transfer Switch resulting from its finite resistance [2]. This Charge Pump architecture is frequently employed in ultra-low voltage applications due to utilizing a step charge sharing technique in each gate signal of the accompanying Charge Transfer Switch, which was introduced in [16]. The first voltage change of the transistor triggers the transfer of charge across the capacitors of both stages, enabling the Charge Transfer Switch to utilize the remaining charge on the capacitor from the stage prior to it. This method leads to a substantial 50% decrease in the energy supplied by the source. This decrease is a direct consequence of the practical step charge-sharing approach, which adds to the technology's allure. Charge sharing is responsible for the first half. When CLKA pumps the transistor, the second half is transmitted from the power supply. The total energy E transferred, is given by

$$E = \frac{1}{2}C_p \left(\frac{V_f}{2} - V_i \right)^2 + \frac{1}{2}C_p \left[V_f - \left(\frac{V_f}{2} + V_i \right) \right]^2 = C_p \left(\frac{V_f}{2} - V_i \right)^2 < \frac{1}{2} (V_f - V_i)^2 \quad (6.3)$$

where V_i and V_f are the initial and final voltage levels of the capacitor[27]. The load of the first-level Charge Pump is the Load of the second-level Charge Pump, which is $7M\Omega$.

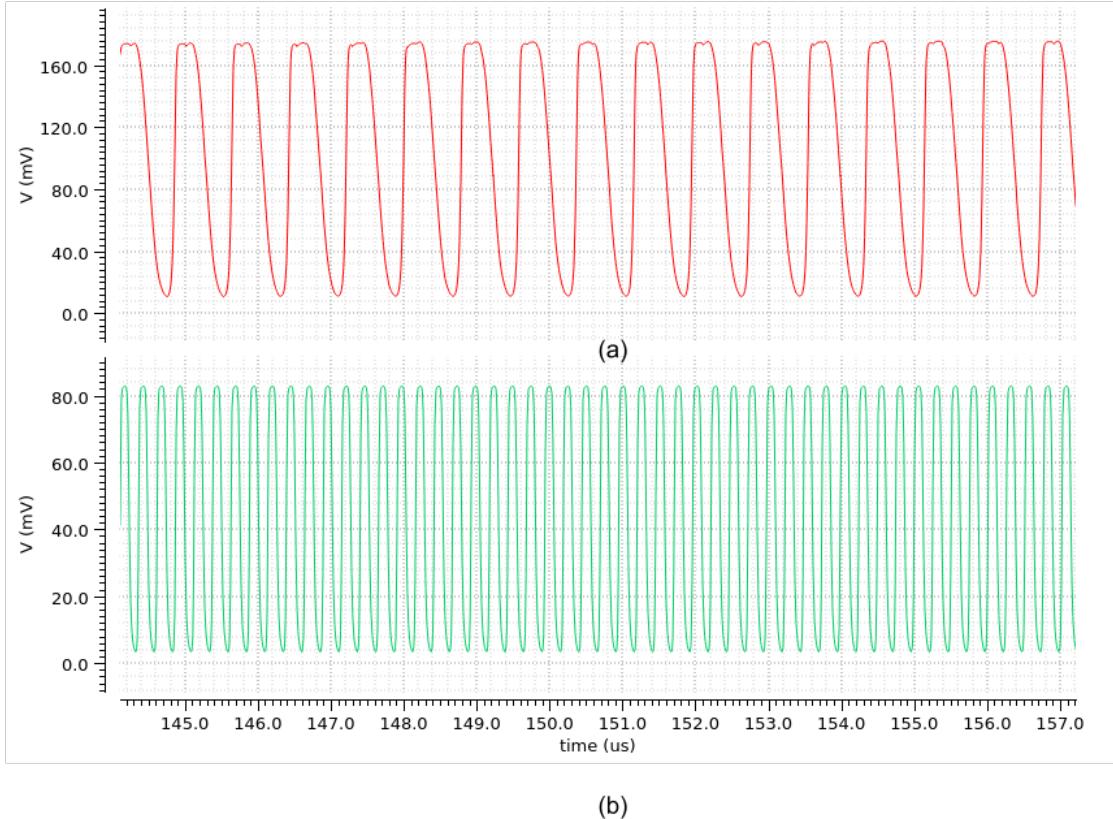


Figure 6.9. : (a) Level 2 clock pulse with an amplitude of 164.6mV and frequency of 1.55MHz and (b) Level 1 clock pulse with an amplitude of 83mV and frequency of 3.93MHz

6.5 Experimental Results

6.5.1 Clock Pulse

The clock pulses of level 2 and level 1 are shown in Figure 6.9. The frequency of the level 1 clock pulse is 3.93 MHz at an amplitude of 83 mV, and the frequency of the level 2 clock pulse is 1.55 MHz at an amplitude of 164.6 mV.

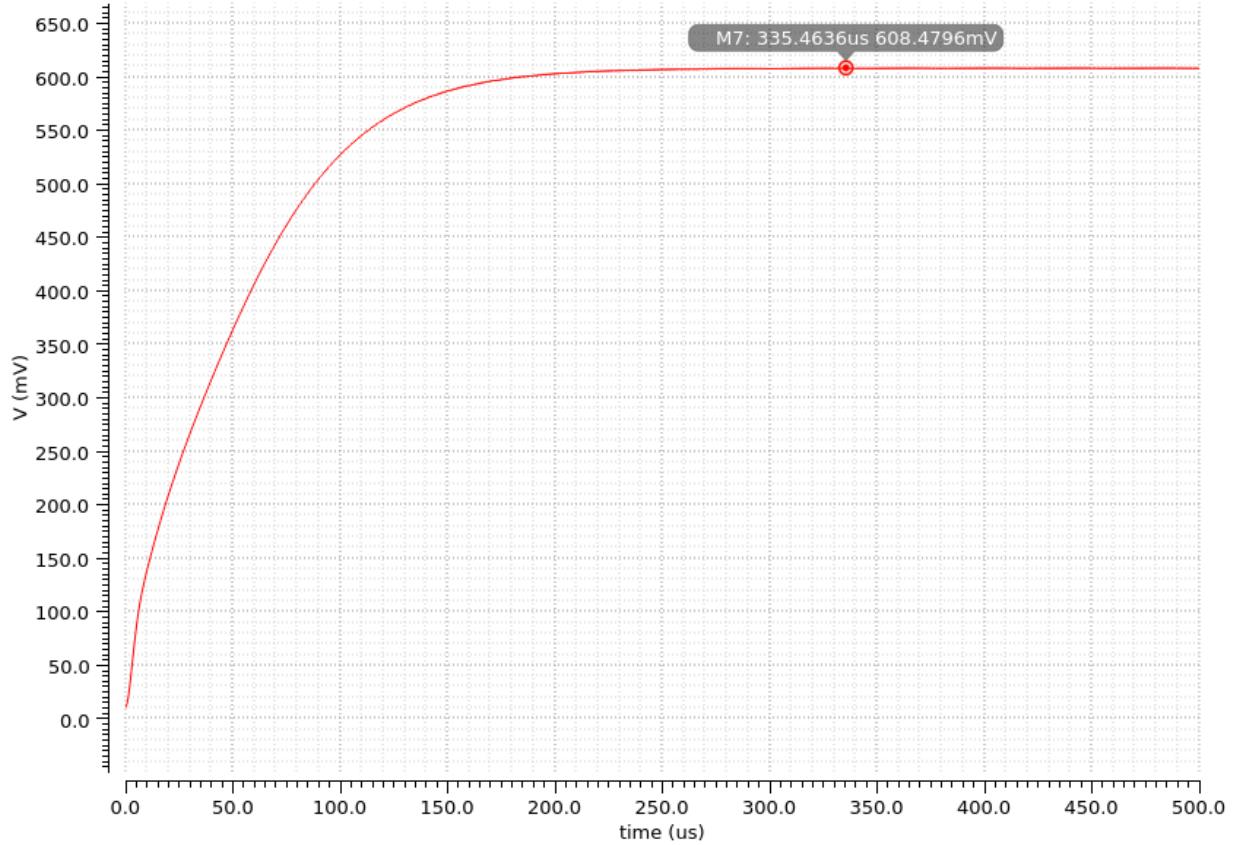


Figure 6.10. : Transient Response of V_{OUT} at $7 \text{ M}\Omega$

6.5.2 Output Voltage

The transient response of the charge pump output voltage at $V_{\text{OUT}} = 608.6 \text{ mV}$ and load resistance of $7 \text{ M}\Omega$ and a rise time of $335 \mu\text{s}$ with very low voltage ripple can be observed in Figure 6.10. Figure 6.11 shows an efficiency and output voltage graph concerning the output load resistance. The highest voltage was around 700 mV at $11 \text{ M}\Omega$, but the efficiency was slightly reduced at this load. At $7 \text{ M}\Omega$ output resistance, we can achieve an output voltage of 608 mV with an efficiency of 29.5% . Efficiency η can be calculated as follows:

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{V_{\text{OUT}} \cdot I_{\text{OUT}}}{V_{\text{IN}} \cdot I_{\text{IN}}} \quad (6.4)$$

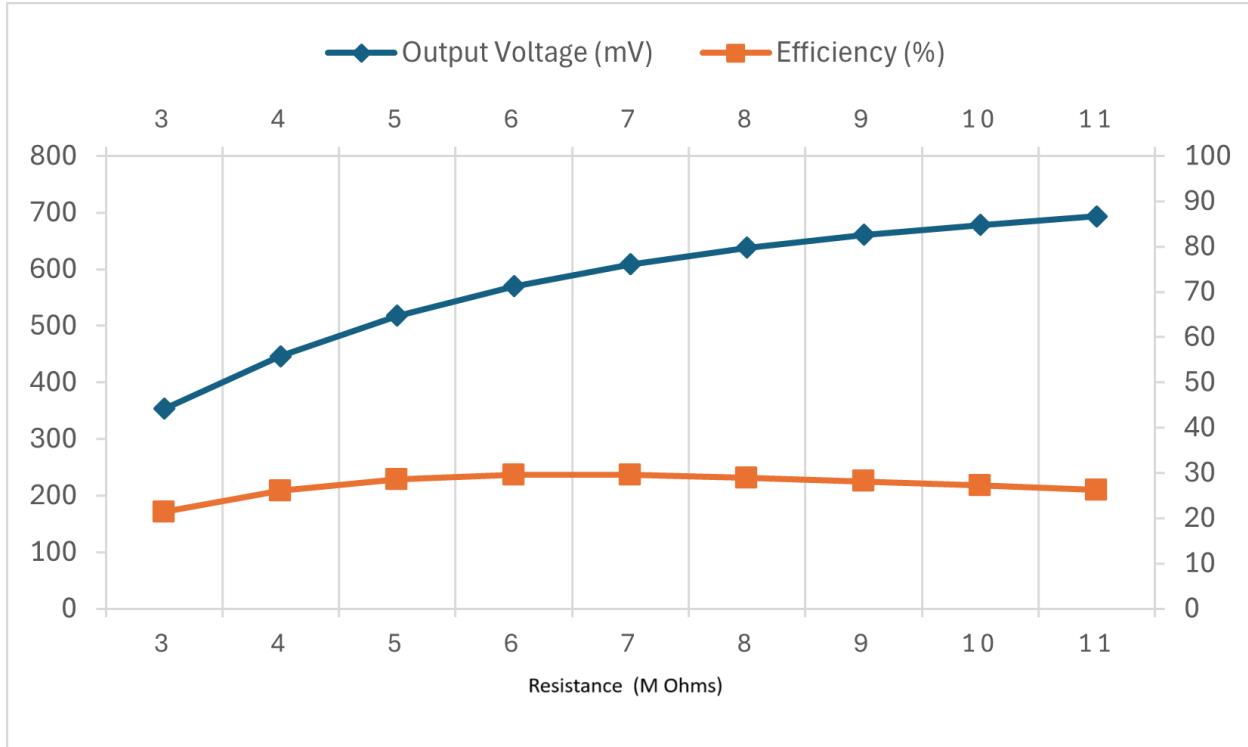


Figure 6.11. : Comparison of output voltage and efficiency at different Load resistance

where P_{OUT} is the output power, P_{IN} is the input power, V_{OUT} is the output voltage, V_{IN} is the input voltage, I_{OUT} is the output current, and I_{IN} is the input current.

6.5.3 Minimum Input Voltage

To know the minimum operating voltage this design can operate at, the voltage supply was taken from 50mV and increased by 5mV from 50mV to 85mV. The minimum input voltage that can be considered for this charge pump design is 75 mV because the graph's slope primarily increased from that point, as can be seen in Figure 6.12. The minimum input voltage is considered if the boosted voltage is comparatively larger than the input voltage supplied.

Table 6.1 presents a comparison between the outcomes of this study and other cutting-edge Charge Pumps that possess similar attributes. Several design measures are said to be highly equitable when evaluating this work with others. Upon investigation, it can be

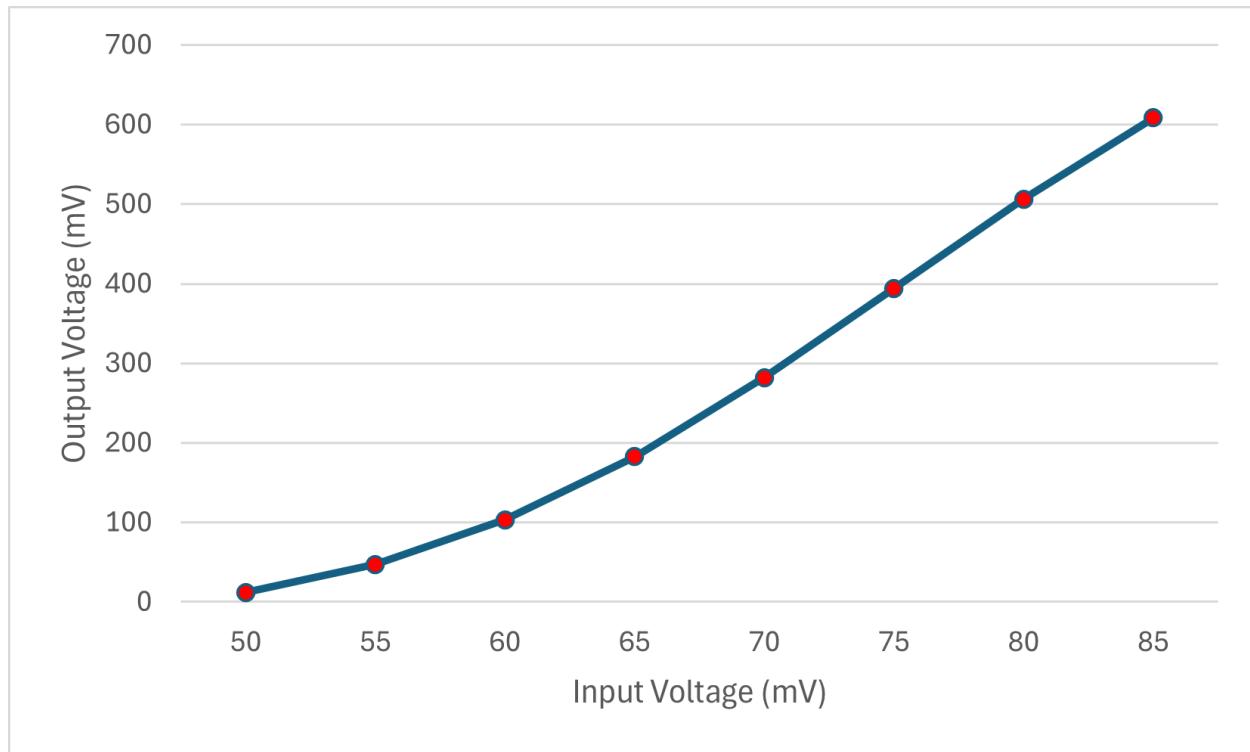


Figure 6.12. : Minimum V_{IN}

observed that each of the Charge Pumps in the following table are identical to one another. However, each option offers unique and desired features that may not be available in others. Although it has been said often in this study, it is important to emphasize that the results reported here are only based on simulations and may be subject to change depending on the completion of the design layout. Compared to the others presented in Table 6.1, some advantages of this work include a decent rise time, off-chip components are not used, and the ability to provide 608.2mV at $7M\Omega$ load resistance while functioning at the slightest input voltage of 75mV. Of all the designs presented with no off-chip components, this work multiplies the input voltage by 7.15 times at a load of $7M\Omega$. A disadvantage of this work is the second lowest efficiency of 29.5%, whereas the lowest is 24%.

Table 6.1. : Comparison of various Charge Pumps

Ref	[28]	[2]	[14]	[23]	This Work
Process (nm)	180	130	18	7	7
Technology	CMOS	CMOS	FinFET	FinFET	FinFET
Input Voltage (nm)	96	200	96	150	85
Output Voltage (nm)	420	610	474.91	633	608.2
Power Consumption (μ W)	0.23	-	0.03	2.14	0.126
Efficiency (%)	24	51	42.9	31.76	29.5

7. FUTURE WORK

One possible avenue for future research is to continue with the arrangement of this study and assess the outcomes by including parasite extraction into the design. Due to the lack of connection between this PDK and foundries, it is not possible to construct the design after the layout process. Additional research might be conducted to decrease the minimal operatable voltage to 50 mV. Although this charge pump utilizes efficient adiabatic clocking techniques, an alternative approach to investigate is amplifying the clock signal right before it reaches the Pump Cores. Additionally To minimize the ripple voltage at the output, it is necessary to optimize the clock frequencies and output capacitance. This work has the potential to be integrated with a FinFET SRAM array and the required peripheral circuits to enhance low-voltage memory solutions for FinFET technology. An additional advantage might be the opportunity to conduct a sociological research comparing the performance of two new technologies, CMOS and FinFET, in the medical area specifically in relation to low-power charge pumps. The prevalence of body-implanted medical devices, health monitoring devices, and wearable gadgets is expected to rise. In order to conduct a comprehensive research, it is necessary to use appropriate measures to guarantee a fair comparison of the technologies, considering the numerous variables that might impact the performance of a charge pump.

8. SUMMARY

This thesis introduces a design for an ultra-low power FinFET charge pump specifically for energy harvesting systems. The design is then compared to many existing state-of-the-art charge pumps. The charge pump implemented in this study utilizes a two-level design, employing the identical charge pump circuits but adjusting the number of fins in FinFETs. The simulation of this study was conducted using Cadence Virtuoso. It involved converting an 85mV supply voltage, supposed to be sourced from an energy harvester, into a pumped output voltage of 608.2mV. This pumped output voltage was capable of supplying a broad variety of loads, depending on the clock frequency. The minimum necessary supply voltage for operation is an impressive 75mV, making it highly competitive. Additionally, it has a quicker rise time of around $300\mu\text{s}$ compared to other designs. This system was specifically built for the purpose of low-voltage energy harvesting. Nevertheless, with slight modifications and enhancements, it has the potential to be utilized in nearly any low-voltage design that requires an additional on-chip power source. A power calculation was performed to determine the efficiency and offer a quantitative assessment of the overall system. This thesis includes a range of both digital and analog circuits, together with their corresponding waveforms, to demonstrate and confirm the functioning of each circuit and the overall system. The findings of this thesis demonstrate that FinFET charge pumps provide a feasible option for ultra-low-power systems that harvest energy and can serve as a substitute for a normal CMOS system, depending on the limitations set by the designer.

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