

Design of Ultra-Low Power FinFET Charge Pumps for Energy Harvesting Systems

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Abstract—This paper introduces an ultra-low-voltage charge pump for energy harvesters in biosensors. The unique aspect of the proposed charge pump is its two-level design, where the first stage elevates the voltage to a specific level, and the output voltage of this stage becomes the input voltage of the second stage. Using two levels reduces the number of stages in a charge pump and improves efficiency to get a higher voltage gain. In our measurements, this charge pump design could convert a low 85 mV input voltage to a substantial 608.2 mV output voltage, approximately 7.15 times the input voltage, while maintaining a load resistance of 7 MΩ and a 29.5% conversion efficiency.

Index Terms—FinFET, charge pump, ultra-low power, Energy Harvesting, bio-sensors

I. INTRODUCTION

Nowadays, there is a gradual rise in the usage of biosensors and wearable health monitoring devices. Using batteries for these devices can make the devices bulkier. Also, replacing and recharging the batteries might be difficult because some biosensors and devices cannot be easily accessed. Energy harvesting technologies like thermoelectric generators and biochemical cells can produce voltage from human skin and body liquids. However, the voltages generated by these energy harvesters are very low, near a few milli volts. Thus, a low-input DC-DC converter is required to boost the harvested energy to a usable output. The power management system in these applications uses switched capacitors, switched inductors, or both. These switched capacitors are used in low-power devices like sensors where energy harvesters produce voltage from their environment. A charge pump is one such switched capacitor containing diodes or CMOS transistors as switches to multiply the voltage. The charge pump is mainly used in energy-harvesting applications and memory management circuits. However, using inductors and large capacitors results in bulking the device, which might not be suitable for biosensors. Many projects have implemented different charge pump circuit design techniques for energy harvesting applications, but most have off-chip components and contain inductors. A

system-on-chip IC (integrated circuits) has been designed to overcome this issue. More studies are needed on the use of FinFET technology in designing charge pumps. In our work, we leverage FinFET transistors to implement a charge pump circuit as a system on a chip. This approach allows us to multiply an 85 mV input voltage to obtain an output voltage of 608.2 mV at a load resistance of 7 MΩ. The use of FinFET technology in charge pump design offers several significant advantages, including its unique ability to vary the width of the transistor while keeping the length constant and the potential to increase the width of the transistor by increasing the number of fins. These features make FinFET technology a promising tool for enhancing the efficiency and performance of charge pump designs.

II. FINFET TECHNOLOGY

The FinFET devices are 3D structured devices that use fin-shaped channels. FinFET transistors' enhanced gate control over the channel allows for more aggressive transistor size scaling, reducing short-channel effects. Enhancing speed and power efficiency, these transistors provide greater driving currents and reduced off-state leakage currents. They are perfect for high-performance computer and mobile applications since they can have faster clock rates and use less power. Since more transistors can be crammed into a smaller space thanks to the 7nm manufacturing technology, transistor density increases. Integrated circuit complexity and chip size reduction are a result of this. 7nm FinFETs are more power-efficient and perform better because of their better architecture. Because of this, they are especially well-suited for portable gadgets and situations where the energy economy is crucial. The ASAP 7nm Process Design Kit (PDK), created by Arizona State University and ARM Ltd. for academic use, contains the FinFET technology utilized in this work. This PDK is feasible and independent of a foundry based on the assumptions for the 7nm technology node [17]. Two of the four transistor

types available for the ASAP7 PDK are used in this work: the low threshold voltage (LVT) and super low threshold voltage (SLVT). Increasing the number of fins will increase the transistor's width with this FinFET technology, where the length stays fixed, and only the width may be changed.

III. SYSTEM ARCHITECTURE

When the input voltage is extremely low, converting it into a usable output with optimal efficiency at a single level poses a challenge. As the number of stages in a charge pump increases, the efficiency of the charge pump drops, resulting in lower voltage gain. However, in this design, the circuit is divided into two levels. In the first level, the circuits boost the voltage to a certain voltage to achieve an output voltage with decent efficiency. The output voltage of the first-level charge pump is then fed to the oscillator, charge pump, and driver circuits of the second level. This architectural innovation helps reduce the number of charge pump stages, instead adding an oscillator and driver circuits. The top-level block-level representation is shown in Figure 1 below, which shows biofuel cells supplying the voltage to the system. The voltage supply is provided to the charge generator and driver circuit to operate, and the same V_{IN} is provided to the charge pump circuit in level one as the input voltage. Doubled at the output of level 1, the V_{OUT} nearing 164.6 mV. The 164.6 mV is fed to the second level of the circuit; the second level also contains the same circuits as level one. The output voltage of level one is supplied to the second-level oscillator and driver circuit to operate, and the same voltage is provided to the 3-stage charge pump as input voltage. The output voltage is near 608 mV at a load resistance of $7\text{M}\Omega$.

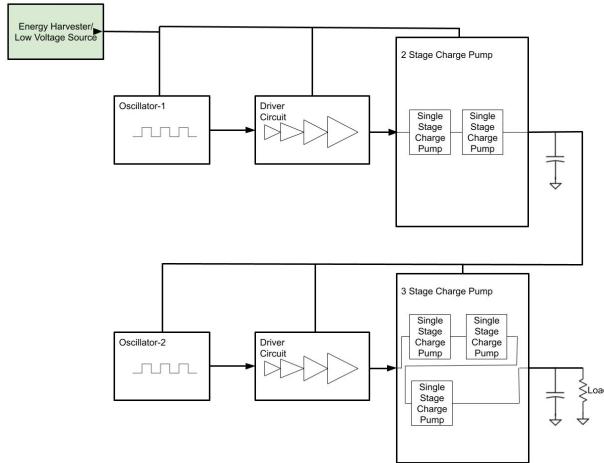


Fig. 1. Block diagram of the designed Charge Pump.

IV. OSCILLATOR

The oscillator is a pivotal component of the circuit design. In this case, a two-phase, non-overlapping oscillator was specifically designed. It features an inverter-based oscillator with NMOS LVT transistors placed between the inverters to

achieve the required frequency. Varying the oscillator parameters allows the charge pump to achieve an optimum frequency. This design incorporates two oscillators, one for each level. Level 1 contains a 5-stage oscillator, while level 2 contains a 3-stage oscillator. The oscillator frequency is given by equation (1), providing a comprehensive understanding of its operation.

$$f = \frac{I_s}{2 \cdot N \cdot V_{IN} \cdot C_f} \quad (1)$$

From equation (1) I_s , N , V_{IN} , and C_f are 5.9nA, 5, 85 mV, and 1.8fF, respectively, which generates 3.93 MHz of frequency for level 1. Similarly, for level 2 I_s , N , V_{IN} , and C_f are 5.9nA, 3, 164.6 mV and 0.1fF, respectively to get 1.55 MHz.

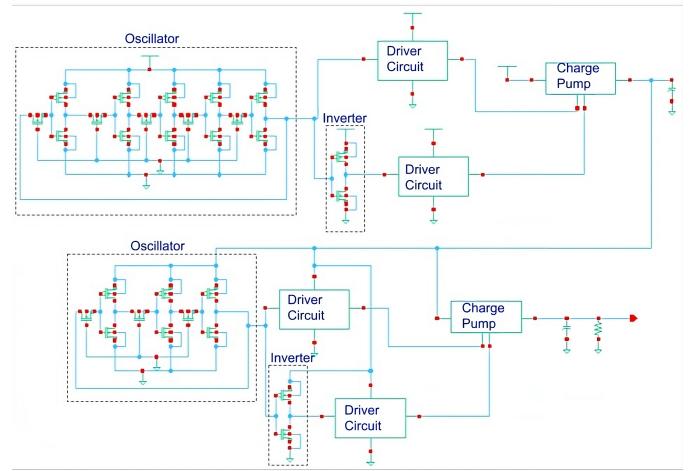


Fig. 2. 5-stage and 3-stage oscillator circuits for level-1 and level-2.

V. DRIVER CIRCUITS

A voltage drop may result when the clock pulses generated from the oscillator are directly connected to the charge pump circuit. To avoid this problem, driver circuits are placed between the oscillator and the charge pump. In driver circuits, buffers are placed in series with the increase in the size of transistors. For FinFET devices, the size can vary by increasing the fins. In level 1, three buffers are used, while in level 2, only two buffers are used. Three buffers are used in level 1 because the size of the transistor of the charge is more significant compared to level 2 transistors. The size of the last buffer of the driver circuit must be comparatively larger than the size of the charge pump transistor to avoid voltage drop. The sizing must be done accurately because increasing the transistor sizes results in larger current leakage.

VI. CHARGE PUMP CIRCUIT

This design uses a charge pump circuit with cross-connected NMOS cells same as in [15]. In level 1, the 2-stage charge pump is used, while a 3-stage charge pump is used in level 2. A 2-stage charge pump is designed in the first level because the transistors are much larger than those of level 2 transistors. If

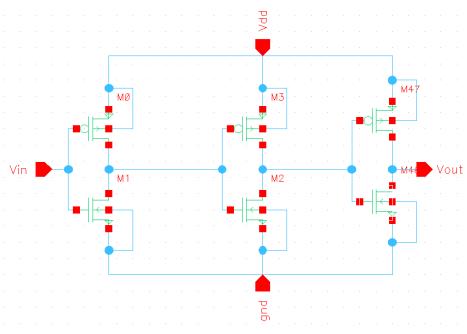


Fig. 3. Level-1 Driver circuit.

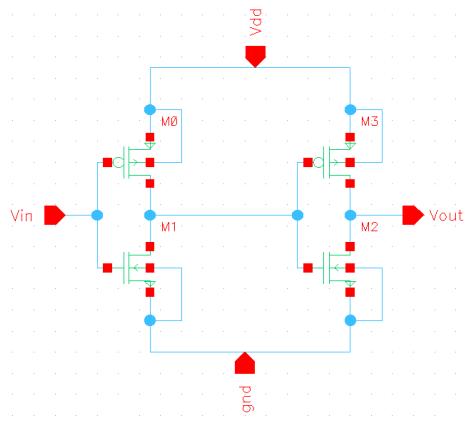


Fig. 4. Level-2 Driver Circuit.

the transistor sizes are large, this decreases the charge pump's efficiency. Factors affecting the efficiency include leakage current and the capacitance in the transistor. SLVT transistors are used in designing the charge pump because the threshold voltage is very low. With two-phase non-overlapping clock signals, the transistors are turned ON and OFF depending on the clock pulse provided to the capacitors. This helps to transfer the voltage from one capacitor to the other, which allows multiplying the input voltage supplied to the charge pump. The size of the capacitor is another factor affecting the output voltage gain. In a cross-connect NMOS charge pump, input voltage gets multiplied by the number of stages in the charge pump, but the number of stages of the charge pump will be limited depending on the efficiency of the transistor switches. .2ectionExperimental Results

The clock pulses of level 2 and level 1 are shown in Figure 7. The frequency of the level 1 clock pulse is 3.93 MHz at an amplitude of 83 mV, and the frequency of the level 2 clock pulse is 1.55 MHz at an amplitude of 164.6 mV.

The transient response of the charge pump output voltage at $V_{OUT} = 608.6$ mV and load resistance of $7\text{M}\Omega$ and a rise time of 335\mu s with very low voltage ripple can be observed in Figure 8.

Figure 9 shows an efficiency and output voltage graph concerning the output load resistance. At $7\text{M}\Omega$ output resistance,

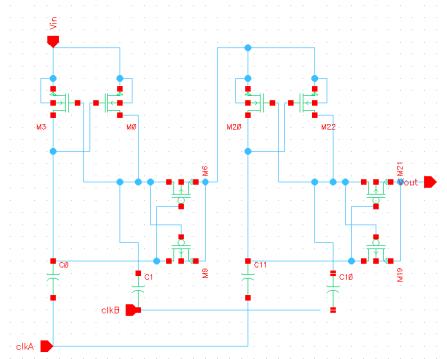


Fig. 5. Level-1 two-stage charge pump.

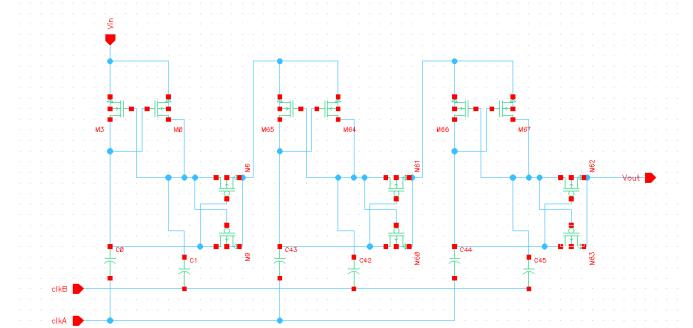


Fig. 6. Level-2 three-stage charge pump.

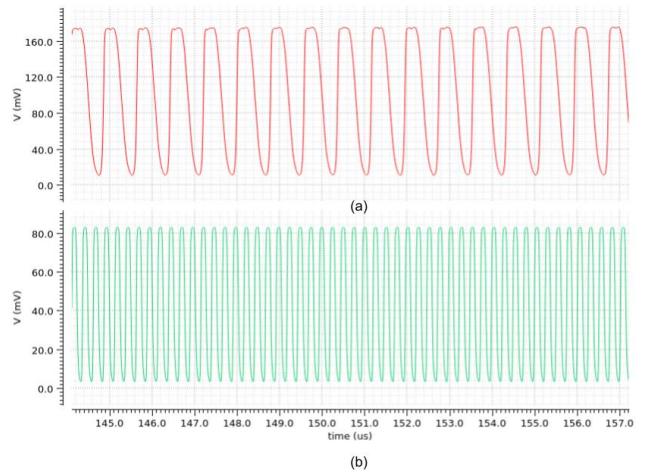


Fig. 7. (a) Level 2 clock pulse and (b) Level 1 clock pulse.

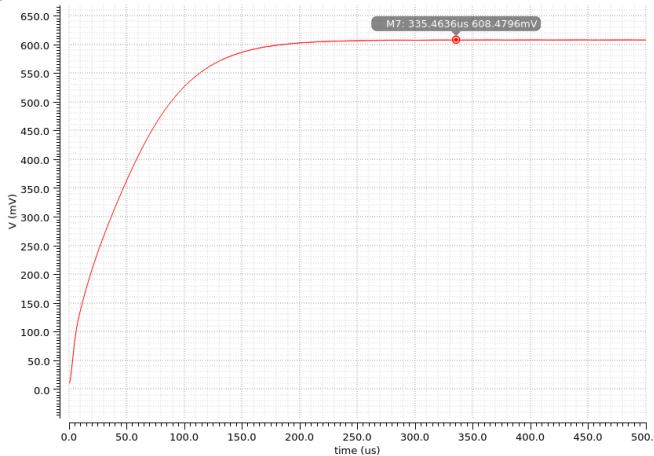


Fig. 8. Transient Response of V_{OUT} at $7 \text{ M}\Omega$.

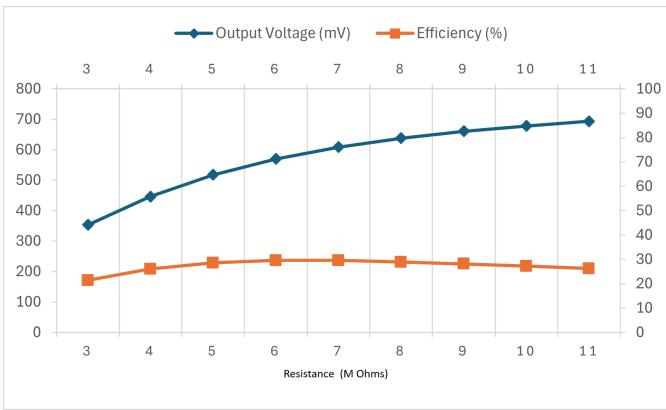


Fig. 9. Comparison of output voltage and efficiency at different Load resistance

we can achieve an output voltage of 608 mV with an efficiency of 29.5%. Efficiency η can be calculated as follows:

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{V_{\text{OUT}} \cdot I_{\text{OUT}}}{V_{\text{IN}} \cdot I_{\text{IN}}} \quad (2)$$

The minimum input voltage that can be considered for this charge pump design is 75 mV because the slope of the graph primarily increased from that point.

TABLE I
COMPARISON OF VARIOUS CHARGE PUMPS

Ref	[4]	[3]	[2]	[1]	This Work
Process (nm)	180	130	18	7	7
Technology	CMOS	CMOS	FinFET	FinFET	FinFET
Input Voltage (mV)	96	200	96	150	85
Output Voltage (mV)	420	610	474.91	633	608.2
Power Consumption (μW)	0.23	-	0.03	2.14	0.126
Efficiency (%)	24	51	42.9	31.76	29.5

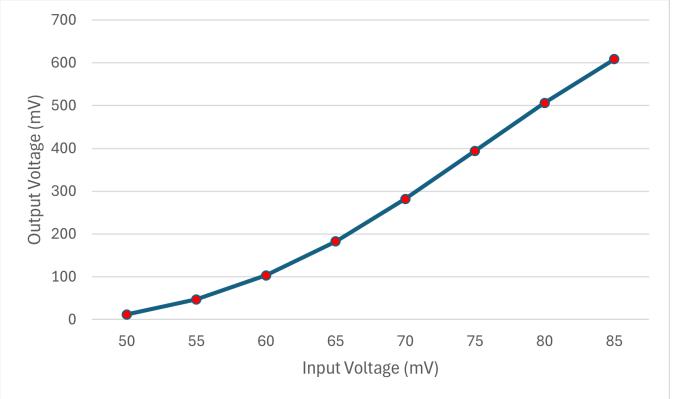


Fig. 10. Minimum V_{IN} .

VII. CONCLUSION

This paper discusses the design of an ultra-low-power FinFET charge pump for energy harvesting systems. The two-level architecture of the charge pump demonstrated a significant improvement in efficiency and voltage gain, converting an 85 mV input voltage to a 608.2 mV output voltage with a 29.5% conversion efficiency at a load resistance of $7 \text{ M}\Omega$. Results indicate that the two-level design minimizes the number of stages required in the charge pump, enhancing the overall efficiency and output voltage at low input voltage. The output power of the charge pump could be further boosted by increasing the transistor sizes—additionally, the impact of varying load resistances on the performance of the charge pump warrants further investigation. Future work will explore integrating the FinFET charge pump design into more complex systems, such as multi-functional wearable devices, and further miniaturize the components to enhance portability and usability with increased output power. Investigating the charge pump's long-term stability and reliability in real-world applications will also be an essential step towards commercial viability.

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