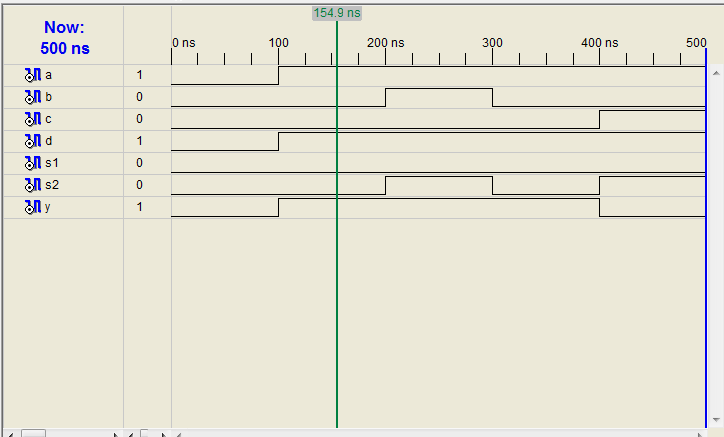
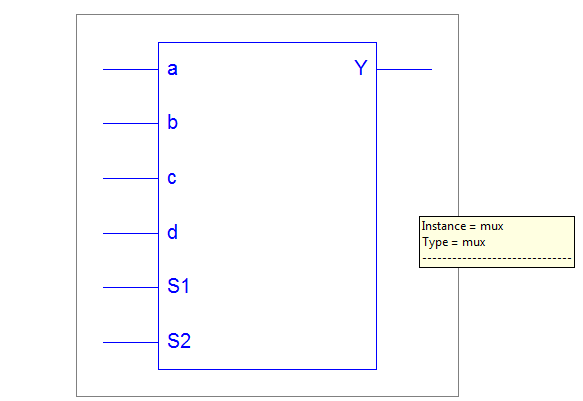


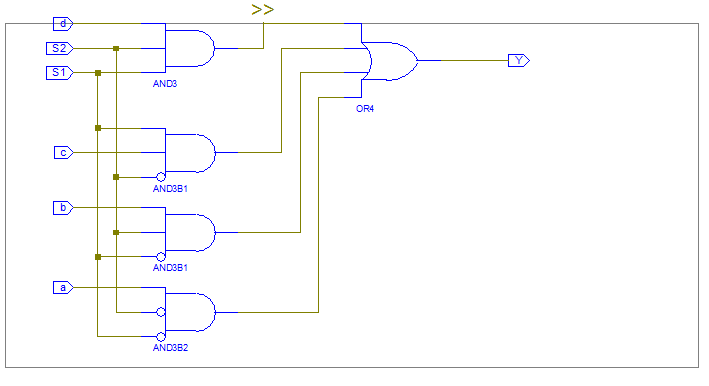
Waveform:



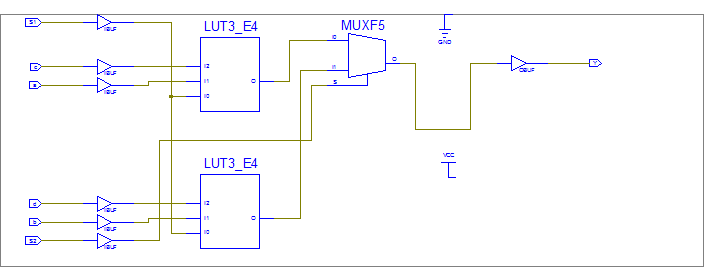
Behavioral:

Rtl:

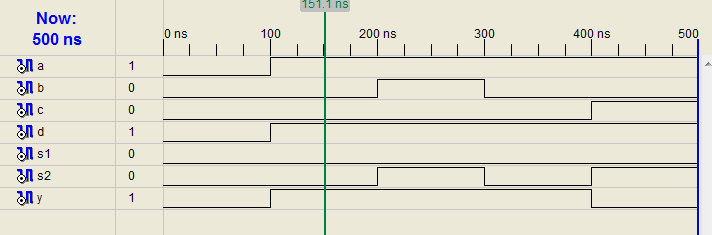




Technological:

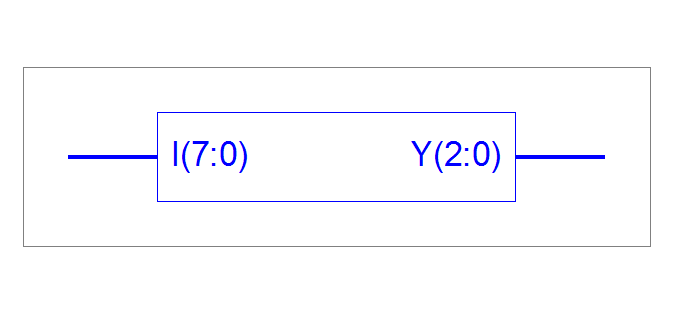


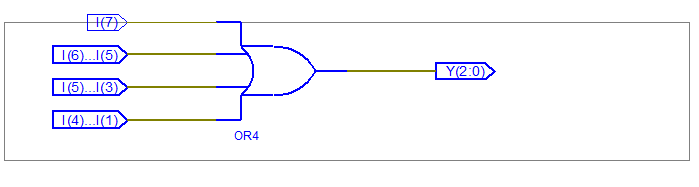
Waveform:



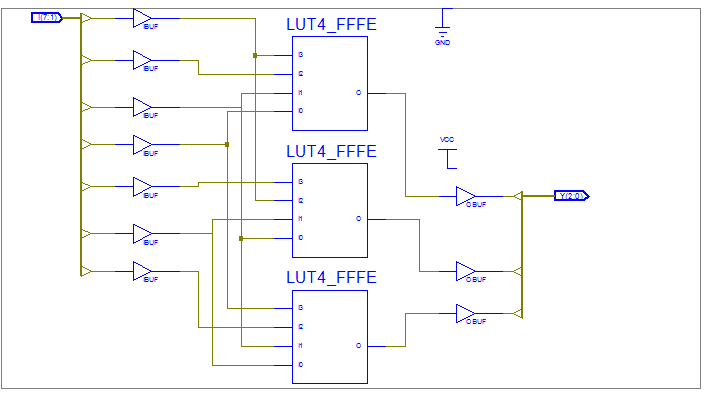
ENCODER 3:8-

RTL View:

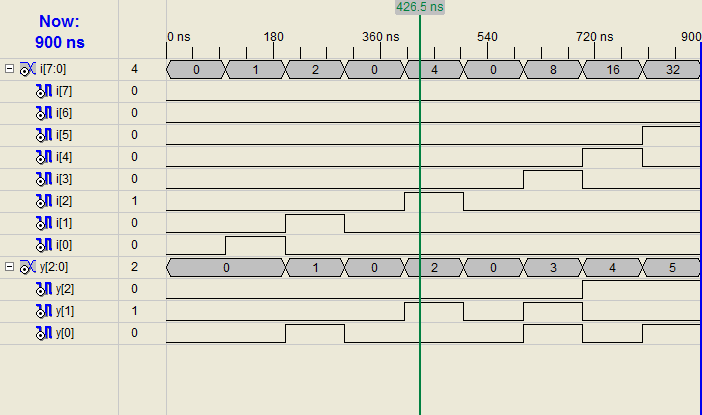




TECHNOLOGICAL:



OUTPUT WAVEFORM:



Proirity encoder

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity priority\_1 is

Port ( I : in STD\_LOGIC\_VECTOR (7 downto 0);

Y : out STD\_LOGIC\_VECTOR (2 downto 0));

end priority\_1;

architecture Behavioral of priority\_1 is

begin

begin process(I)

if (I(7)='1')then

Y <= "111";

elsif(I(6) ='1')then

Y <= "110";

elsif(I(5) = '1')then

Y <= "101";

elsif(I(4) = '1')then

Y <= "100";

elsif(I(3) = '1')then

Y <= "011";

elsif(I(2) = '1')then

Y <= "010";

elsif(I(1) = '1')then

Y <= "001";

elsif(I(0) ='1')then

Y <= "000";

else

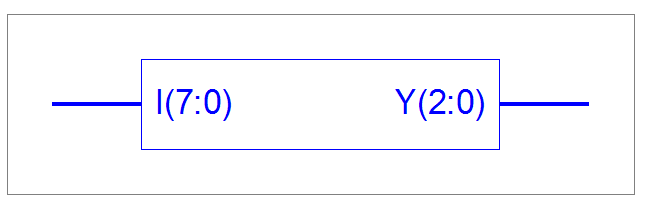
NULL;

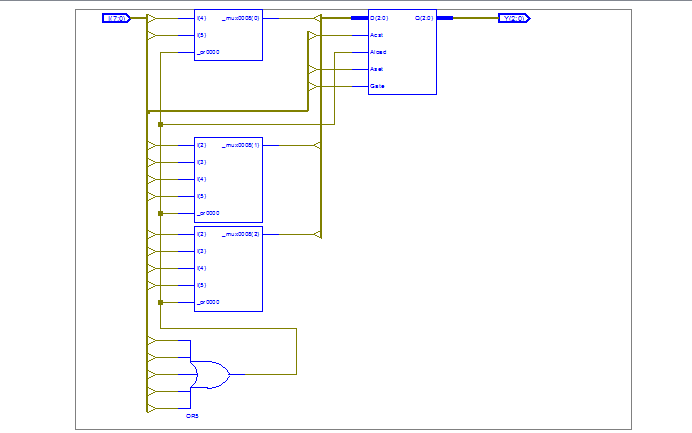
end if;

end process;

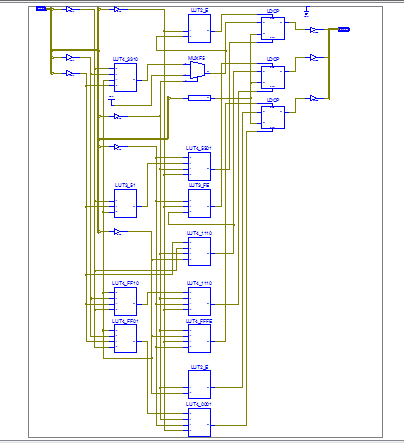
end Behavioral;

RTL view:

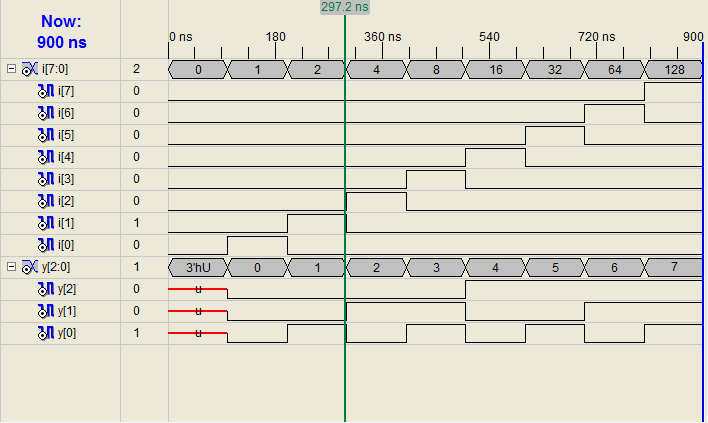




Technological view:



Output waveform:



Decoder

RTL view: