ABSTRACT

The thermomechanical stresses due to the variation in coefficients of thermal expansion (CTE) of the base material, material of the chips and the adhesives has a significant impact of the stresses in the product used in high temperature applications. The subject essentially consists of SiC die attached to an Alumina substrate using epoxies attach. Characterization of the heat distribution within the die attach, die and substrate along the thermal resistance of the die attach is essential to predicting the reliability of the packaging structure.

A parametric research has been performed to find the heat flux distribution and thermal shock resistance by simulating it at high temperature and comparing it with analytical calculation. The project also focuses on the processes involved in the packaging of the die and study of the devices and their functions.

The outcome of the project is to provide guidelines to optimize the design of the package and comparison and getting to hand on work knowledge on the whole process of the packaging.

The packaging is done in the VAPD lab of Semi-Conductor laboratory and the simulation of the thermomechanical designing is done on various software like CATIA, ANSYS AIM etc.

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Chapter 1 INTRODUCTION

1.1 INTRODUCTION TO WORK DONE:

Semiconductor packaging can be defined as the interconnection of the semiconductor chip and the establishment and regulation of its operational environment in order to meet specified performance, reliability and cost requirements. In the hierarchy of electronic packaging, the semiconductor package is often considered as level 1 with printed wiring board, subsystem and system packaging regarded as levels 2,3,4 respectively. Integrated circuit is defined as a miniature device that combines elements such as transistors, resistors, dielectrics, and capacitors into an electrical circuit having a specified function. System refers to all electronic devices.

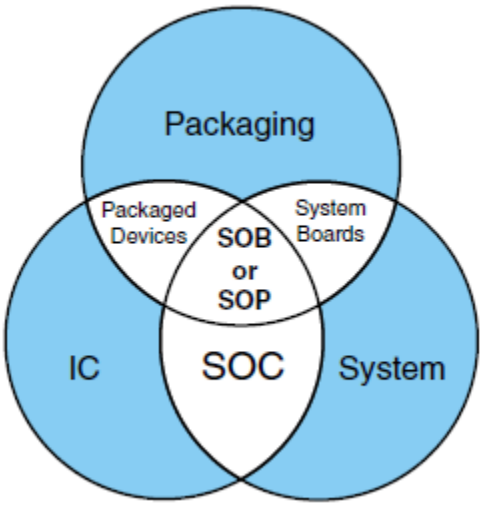

Fig. 1.1.a. Integration of IC, packaging and system.

IC packaging has always been a challenge because of its mini structure and exposure to harsh environments. alloy, silicon and kovar has not yet been found that will perfectly meet all the required challenges. Thermal stability is one of the most important challenge that needs to be overcome as the exposure of epoxies in high temperature for a longer period of time is very tough and delicate. Sharp changes in temperature also causes cracks and breakages in ceramic objects which is also an arising problem in this scenario. Large difference in ratios of coefficient of thermal expansion also lessen down the electrical transmission speed. Improving the quality and investing in higher accuracy devices and soft wares are also very expensive, hence cost effective researches are going on. IC's in SCL are mostly used in space related application hence there is a possibility of sudden elevation of temperature and pressure, so simulation of various dies and its material modelling using finite element analysis with the help of simulation soft wares are done. Using of newly invented alloys with conventional sealing gases and kovar is one of the mostly used process. Space Research Organization always deals with alias environmental situations where the guarantee of ambient conditions are not known. Integrated Circuits make up the whole communication and working of any satellite or space craft, so the most important

parameter is spacing and weight. Hence, material science is taken into consideration while it comes to the base of those devices. All the materials should be strong, sustainable and light weighted for space studies.

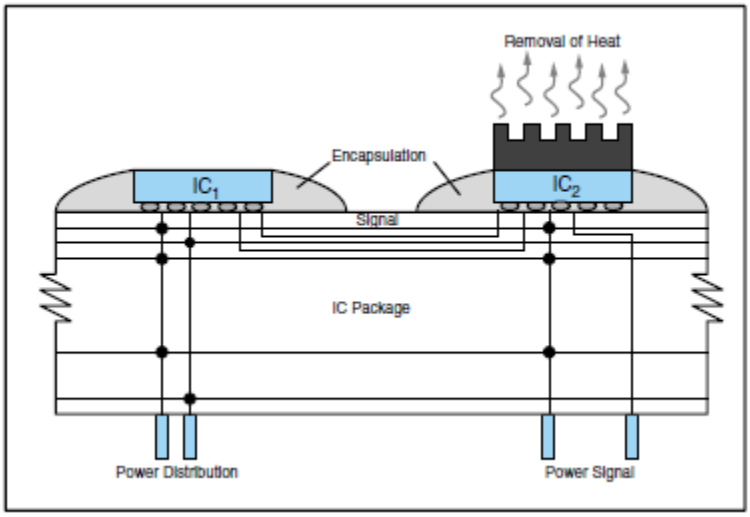

Fig. 1.1.b. IC Packaging

1.2 PROJECT OBJECTIVE:

The main objective of the project is to do the thermal analysis of the materials that are used for IC packaging. Ceramics are inorganic materials which are crystalline or partly crystalline in nature. It is formed by the action of heat and subsequent cooling. They are extremely hard and corrosion resistant material. Ceramics are generally selected for dies which need higher degree of reliability and of hermetic isolation of the die as they provide heat dissipation with lowest thermal resistance. So, this project focuses on finding out the right alloys and resins and finding their compatibility in their coefficient of thermal expansion. The project also focuses on getting the knowledge of the packaging process by hands on experience of the processes involved in the packaging and research on the future scope.

1.3 ORGANIZATION OF REPORT:

- Literature review of the researches that are ongoing globally. As this is one of the trending challenge so knowing about the ongoing project is must.
- Experimental knowledge in laboratories in SCL.
- Getting to know the processes involved in packaging.
- Studying finite element analysis and learning more about material modelling and material models.
- Final, simulation of the materials and dies in soft wares like ANSYS WORKBENCH, ANSYS APDL, CATIA etc.
- Research on further scopes.

Chapter 2 BACKGROUND MATERIAL

2.1 CONCEPTUAL OVERVIEW:

Integrated circuits are array of circuits and components that are implanted on the surface of a unit chip or crystal. Input/ output connections are generally connected to the IC product. Packaging can be defined as the interconnection of the semiconductor chip and the establishment and regulation of its operational environment in order to meet specified performance, reliability and cost requirements. It is a part of assembly department. Division of IC is done on the basis of following types:

- Structures
- Materials
- Size
- Thickness
- Bonding
- Number of connections
- Cost
- Performance
- Reliability

There are different types of IC packages:

- Through Hole - If the package has pins that can be inserted into the holes of PWB, they are called through hole packages.
- Surface Mount – If the package is not inserted into the PWB, but are mounted on the surface of PWB, they are called surface mount packages.

Types:

- Dual In Line Package
- Pin Grid Arrays
- Small Outline Package
- Quad Flat Package
- Ball Grid Array
- Chip Scale Package

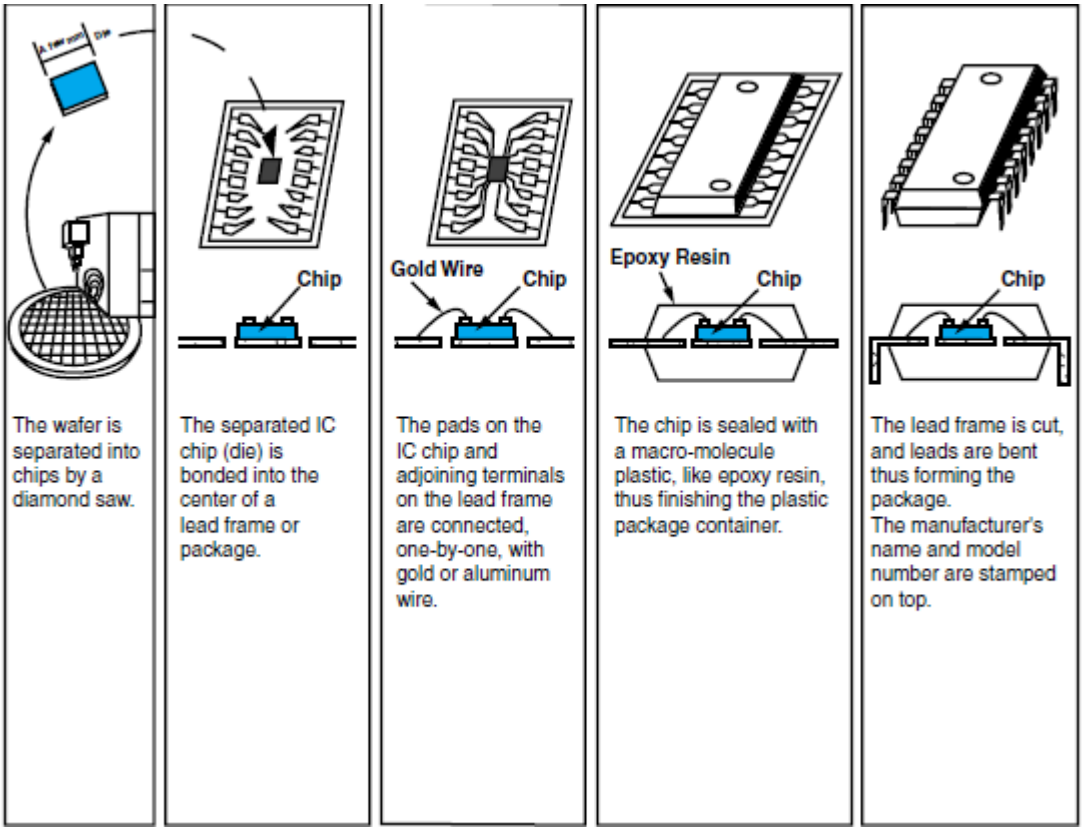

Fig. 2.1.a. Dual In Line IC packaging with wire-bonding

Until early 1980's, Semiconductor device manufacturers emphasized chip fabrication over packaging nearly to a point without much change and therefore not worthy of great attention. Unfortunately to the manufacturers, the package has now been found to have a serious impact on the size, performance, reliability and cost of the packaged chip. In fact, it is anticipated that continuing evaluation of high performance systems will soon be severely limited by characteristic of packages rather than by those semiconductor chips. Therefore, semiconductor packaging must be treated as a broad field incorporating the following characteristics:

- Packaging families and their associated fabrication technologies.
- Assembly operations involved in placing the semiconductor chip into the package.
- The performance and reliability characteristics of the package.

Historically, packaging has evolved as physical hierarchies of the interconnect structures that are delineated according to specific levels. There are 4 levels. Level 1 occurs when the individual chip is extracted from the wafer and then mounted and interconnected on a printed wire board, representing level 2. An array of board interconnected by means of a motherboard and configured into a subsystem, represent level 3 and the computer system, level 4.

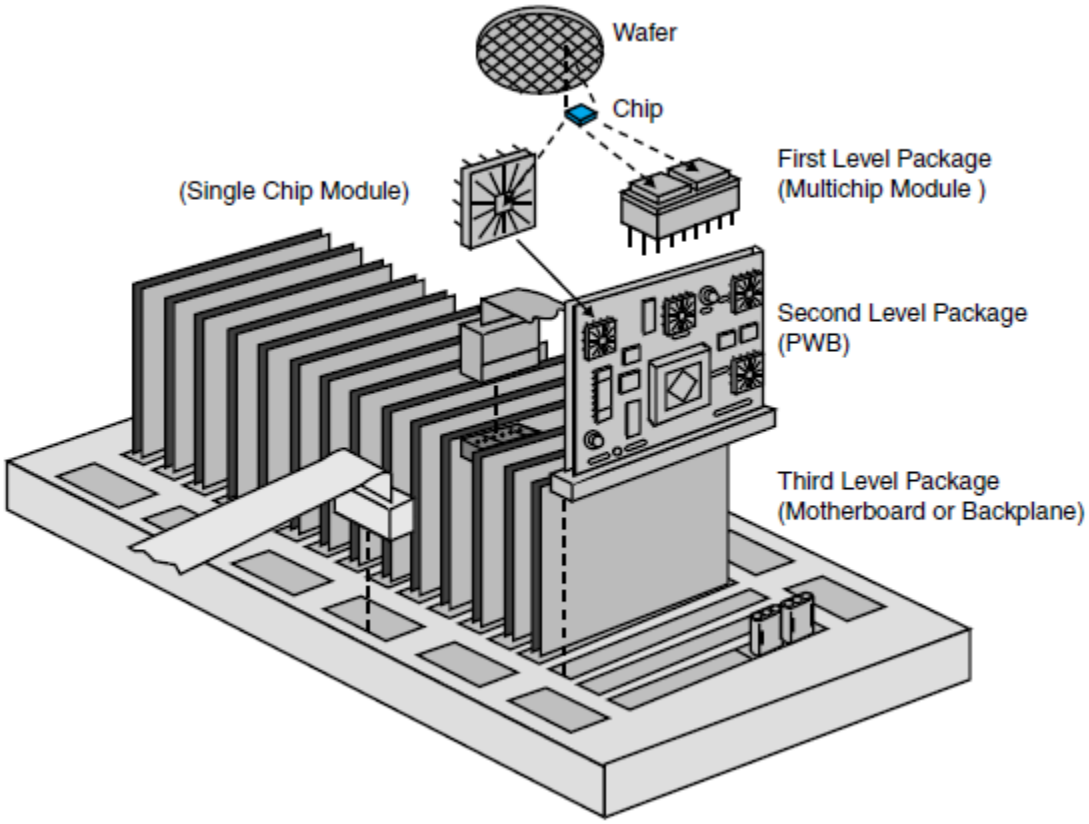

Fig. 2.1.b Packaging levels

In such a coordinated system, every level of packaging must perform certain functions:

- The package must provide electrical interconnections for the transfer of power and information bearing signal between semiconductor chip and the outside world.
- The package must mechanically support the small, fragile chip for subsequent processing, handling and performances.
- It must protect the sensitive chip from atmospheric variables such as moisture, dust and gases that adversely influence performance.
- Because the chip converts most of the electric power it consumes into heat, the package must dissipate the heat in order to prevent degradation in performance and concomitant reduction in operational lifetime.

In fulfilling these functions, however, the package imposes constraints on the chip. It typically degrades the electrical performance on the device, substantially increases the effective size and weight of the chip, encumbers testing and introduces reliability problems. The package also adds cost that often exceeds that of the chip itself. Hence packaging is a complex balance between provision of desired function and reduction of associated constraints. In response to the global world, new designs and materials of construction are evolving for IC's.

2.1.1 PACKAGE DESIGN CONSIDERATION:

The worldwide electronics industry continues to develop high density products. It has entered an era of packaging characteristics by faster, denser, thinner, lighter and lower cost package that can easily dissipate heat. Several technologies have been developed to address these needs. Thick film hybrids and high temperature co-fired ceramics are technologies used routinely by electronics industry that provide solution to high density packaging based on ceramics.

The art of mounting the chip on a substrate in such a way that they can be interconnected, cooled is called packaging.

Packaging problem are one of the severe limitation on the performance of modern high speed, integrated logic. There are many functions that must be taken into account in the design of a package and they are as follows:

- To provide mechanical support and attachment.
- To provide electrical connection to chip.
- Transform chip contact dimension to mechanically pluggable dimensions.
- Contain power distribution network.
- Protect the semiconductor from environment.

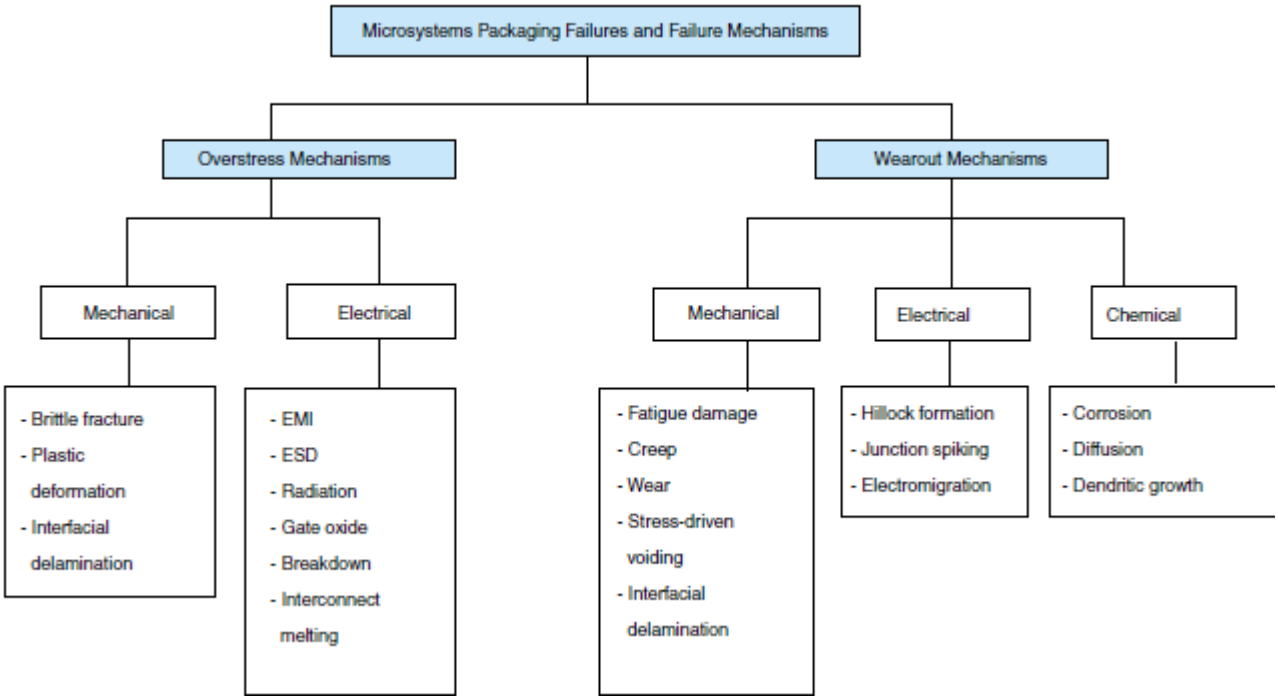

Fig. 2.1.1.a. Failure mechanism

2.1.1.1 PHYSICAL DESIGN:

The physical design starts with the determination of the form or shape of the package that is required to:

- Properly support and protect the semiconductor chip.
- Accommodate the adequate number of input pins for interconnection to the chip.
- Satisfy the space, weight and interconnection restriction imposed by higher level package.

The chip must be supported and protected from mechanical stresses due to handling, shocks, vibration, fatigue loading etc., and chemical stresses due to such things as moisture, particulate, ionic contamination, fluxes and so forth. In addition of two sets of pins, the packages must support multiple interconnections between the sets and if necessary between ground and power planes. Despite these items that consumes space, the shapes of the package should maximize the functional density of the device. Lastly, the selection of standardized package shape could provide an overall cost savings but this must be weighed against potential performance compromises.

2.1.1.2 THERMAL DESIGN:

The first consideration is the requirement that the package withstands the temperature cycles experienced during the chip assembly and board interconnection. Because the package contains dissimilar materials having different coefficient of thermal expansion, thermally induced stresses during temperature cycles and their deleterious effects must be minimized. The products of such reaction normally cause discontinuities in electrical and thermal transport across the interface and in extreme cases, mechanical failure.

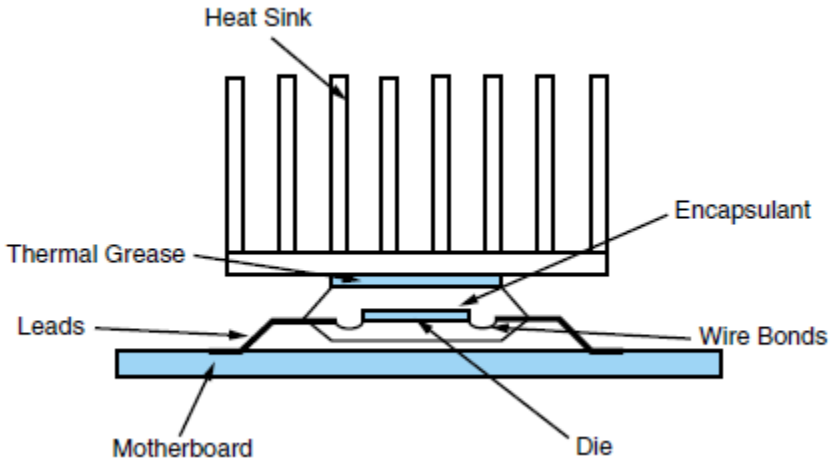

Fig. 2.1.1.2.a. Chip package with heat sink

The second phase of thermal design involves the dissipation of heat generated by semiconductor chip during use. A measure of ability of a package to dissipate the heat generated is its thermal resistance, given by:

$$Resistance\ of\ thermal\ path\ from\ junction\ to\ ambience = \frac{[Temp.\ of\ active\ junction\ in\ sink - Temp.\ of\ ambient\ junction]}{\text{heat dissipated}}$$

The thermal resistance comprises two additive terms:

- θ_{jc} – equivalent resistance of al heat conductive paths, internal to the package from active junction on the chip to the outer package shell. It is primarily controlled by package design through the use of high thermal conductivity materials along primary heat flow paths.
- Θ_{cn} – equivalent resistance of all convective, radiant and other heat flow paths from external shell to ambient. It is controlled by application conditions, which require an understanding of the thermal interactions with higher level packages.

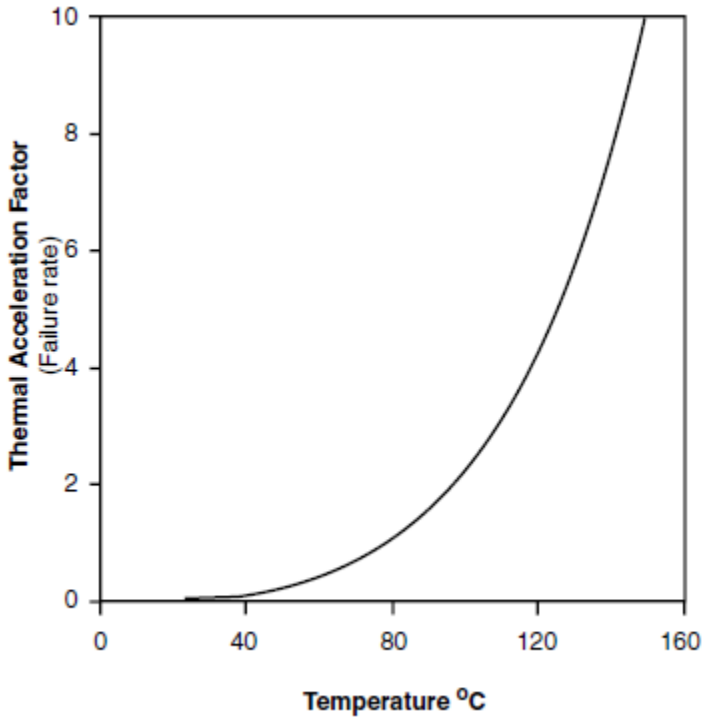

Fig. 2.1.1.2.b. Effect on temperature of failure rate

2.1.1.3 ELECTRICAL DESIGN:

The major issue for electrical design is to determine the impact of level 1 package on the transmission of power and signals through it. For a given package shape and design, a common approach is to convert the mechanical interconnection circuit of the package into an equivalent electrical circuit.

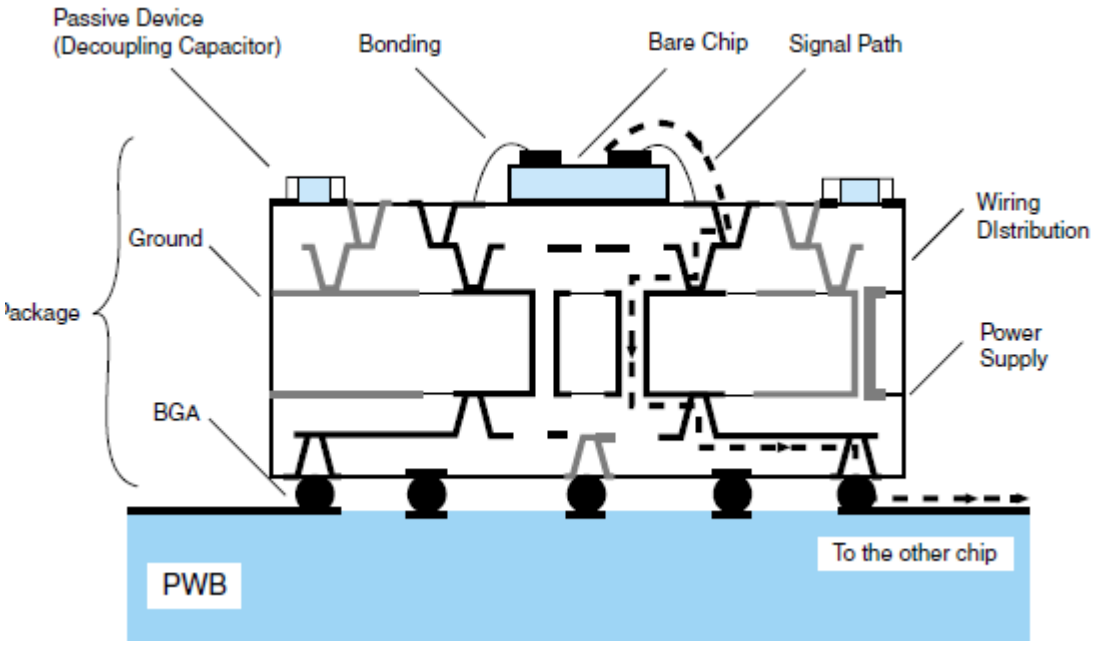

Fig. 2.1.1.3.a. Electrical design issues

2.1.1.4 MANUFACTURING:

Several issues must be addressed including:

- Purchase price or production cost of constituent parts.
- The number, variety and interchangeability of parts.
- Compatibility with existing manufacturing equipment and processes.
- Susceptibility to automation.

2.1.1.5 RELIABILITY:

Reliability is defined as the probability that a packaged device will perform a desired function under specific conditions for a specified time.

Table. 2.1.a. Distinguishing features of each of the families of packaging with the primary material.

PACKAGE AND MATERIAL	MAXIMUM PIN COUNT	MAXIMUM BOARD COUNT	MARKET SHARE
Transistor outline can			
• FN alloy	16	IM	0.6
SIP			
• Epoxy	24	IM	<0.1
DIP			
• Alumina	68	IM	8.7
• Epoxy	68	IM	63.5
Small outline IC			
• Epoxy	40	SM	6.1
Leadless chip carrier			
• Alumina	288	SM	2.4
• Epoxy	240	SM	0.5
Leaded chip carrier			
• Alumina	256	SM	0.6
• Epoxy	240	SM	14.5
Ceramic flat pack			
• Alumina	132	SM	0.3
Metal flat pack			
• FN alloy	64	SM	<0.1
Pin grid array			
• Alumina	386	IM	1.0
• Epoxy	400	IM	0.4
Chip on board			
• Epoxy silicon	400	SM	1.3

2.2 TECHNOLOGIES INVOLVED:

PACKAGE FABRICATION TECHNOLOGY

The following are the basic technologies used to fabricate primary package families:

- Ceramic Packages:
    a. Laminated
    b. Pressed
- Plastic Design:
    a. Laminated
    b. Molded

Not only do the technologies differ with respect to materials and method of construction but also the final products display vast differences in performance, reliability and cost.

Ceramics typically have a superior heat dissipation capability by virtue of their higher thermal conductivities, and a higher reliability as they provide hermetic environment for the chip. The epoxy base plastic packages tend to cost less and exhibit superior electrical performances because of their lower dielectric constant and use of copper interconnects.

Table.2.2. a. Comparison of Packaging Families and fabrication technologies.

FAMILY	SINGLE LAYER MOLDED PLASTIC	SINGLE LAYER PRESSED CERAMIC	MULTI LAYER LAMINATED CERAMIC	MULTI LAYER LAMINATED PLASTIC
Dual in line package	√	√	√	
Chip carrier leaded	√	√	√	
Chip carrier leadless	√		√	√
Grid array pin			√	√
Grid array pad			√	√

2.2.1 CERAMIC PACKAGES:

The ceramic packages are generally selected for applications requiring a higher degree of reliability that can be achieved with a plastic package. Although, ceramic packages can offer several other advantages, the major reason they are selected is because of the hermetic isolation of die. Hermetic packages use a cavity to house the microcircuit, which is then sealed to protect the device from outside ambient conditions. The most common methods for accomplishing hermeticity are with the use of a vitreous sealing gas, gold tin alloy or a kovar weld. Several new materials are being explored for high performance applications. The majority of ceramic packages continue to be manufactured from alumina. The selection of materials, body size and lead configuration can have a significant effect on the electric performance, heat dissipation, and mechanical integrity of the package.

2.2.1.1 GLASS SEALED (CERDIP PACKAGES):

The most common ceramic package is a CERDIP. The CERDIP package must consists of alumina base and lid glazed with a vitreous glass and an alloy 42 lead frame. The lead frame is embedded into the base glass prior to the wire bonding operation. The lead and base assembly are then sealed together and 420-460 leads can be provided with a tin plated or solder dipped finish. Gold plating after seal is also possible is not recommended because of chemical reaction with Pb content in the sealing glass.

These are used in applications requiring the higher reliability of the hermetic seal. Because the die in a CERDIP package is considered on the bottom surface only, it is often used for devices that are sensitive to the additional stress of a molding compound. Nearly all packages today use vitreous glasses, allowing for remitting of the glass without crystallization. Most of the glasses used consists of a base glass composition of about 80% PbO with the remainder mostly Diborane and other minor constituents. High level of capacitance are often encountered with packages using a glass seal and metal lead frame. Selecting a low dielectric glass, increasing the lead to lead separation, reducing the lead thickness.

CERPACKS and CERQUADS are low profile surface mount packages similar in body construction to the CERDIP package. The external leads of a CERPACK exit the body parallel to the sealing plane from two sides of the ceramic body. The leads are then formed into a gull wing configuration for surface mounting. CERQUADS are a version of the CERPACK with external leads existing on all four sides. The leads can be formed into a J-bend or gull wing configuration. The best way to enhance electrical performances to separate the power, ground and signal planes.

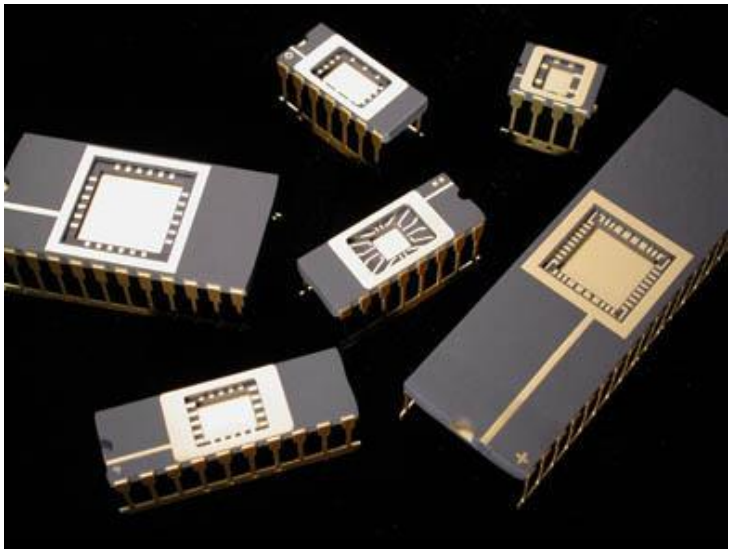

Fig. 2.2.1.1.a. Ceramic dual in line package

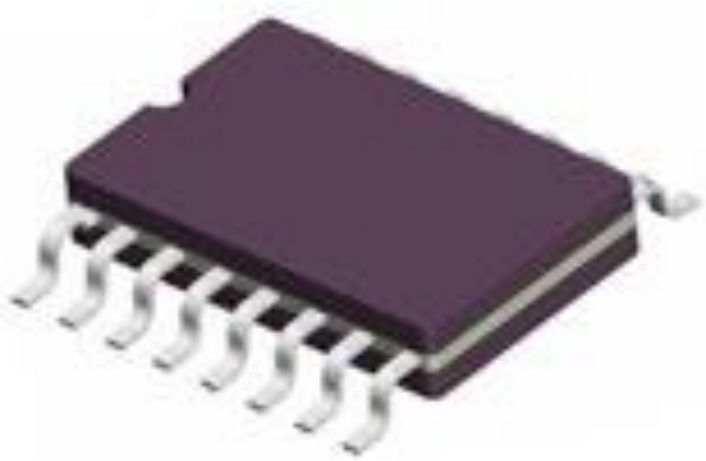

Fig. 2.2.1.1.b. CERPACK packaging type

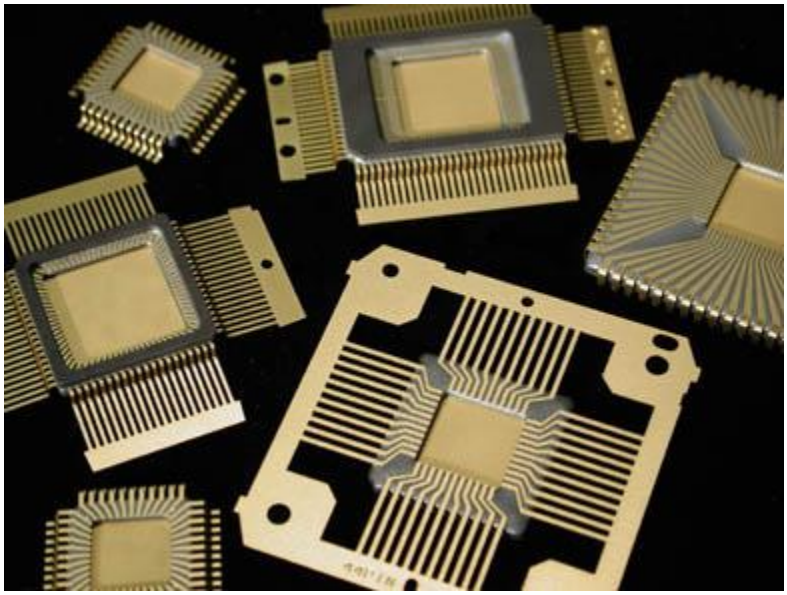

Fig. 2.2.1.1.c. CERQUAD package

2.2.1.2 MULTI LAYER CERAMIC PACKAGE:

These are manufactured from the stacking of several layers of ceramic green tape that have been screened with tungsten in the die attach, lead trace, seal ring and braze pad areas. This process is followed by nickel plating, brazing of leads and a second nickel plating and gold plating of the exposed metal surfaces. This type of package construction allows for considerable leeway in the layer thickness and trace metallization designs, while still meeting the overall package and lead footprint dimensions of equivalent lead count plastic and pressed ceramic packages.

Die attach options for the multilayer packages are the same as those for pressed ceramic packages using a metal lead frame embedded in a glass seal. Aluminum ultrasonic wedge bonding is the most common wire bonding of multi-layer ceramic packages, although gold ball bonding is also possible as long as aluminum gold diffusion and inner metallic growth is avoided. Lower capacitances, inductances and resistances are presently accomplished with multilayer packages through geometric changes rather than material changes.

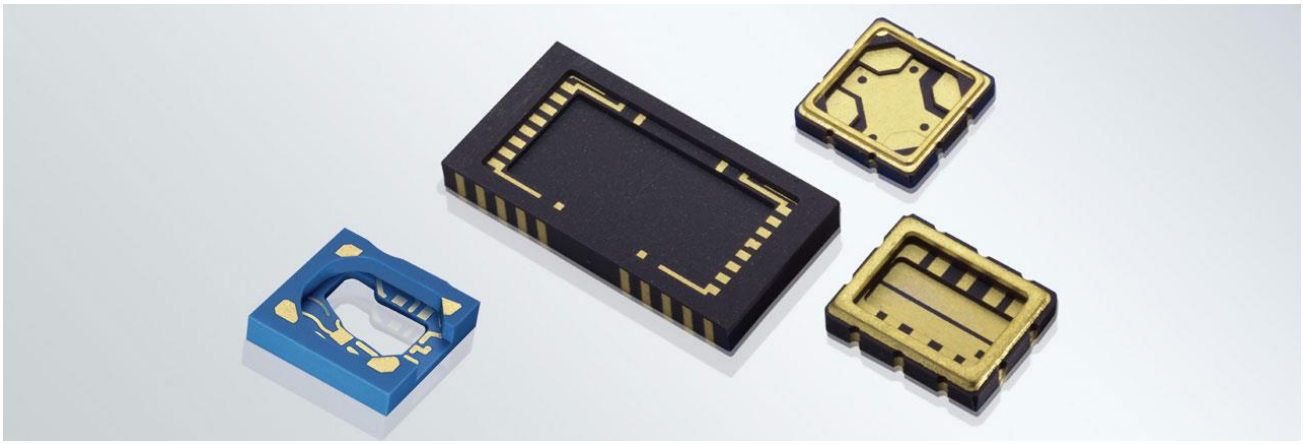

Fig. 2.2.1.2.a. Multilayer ceramic technology

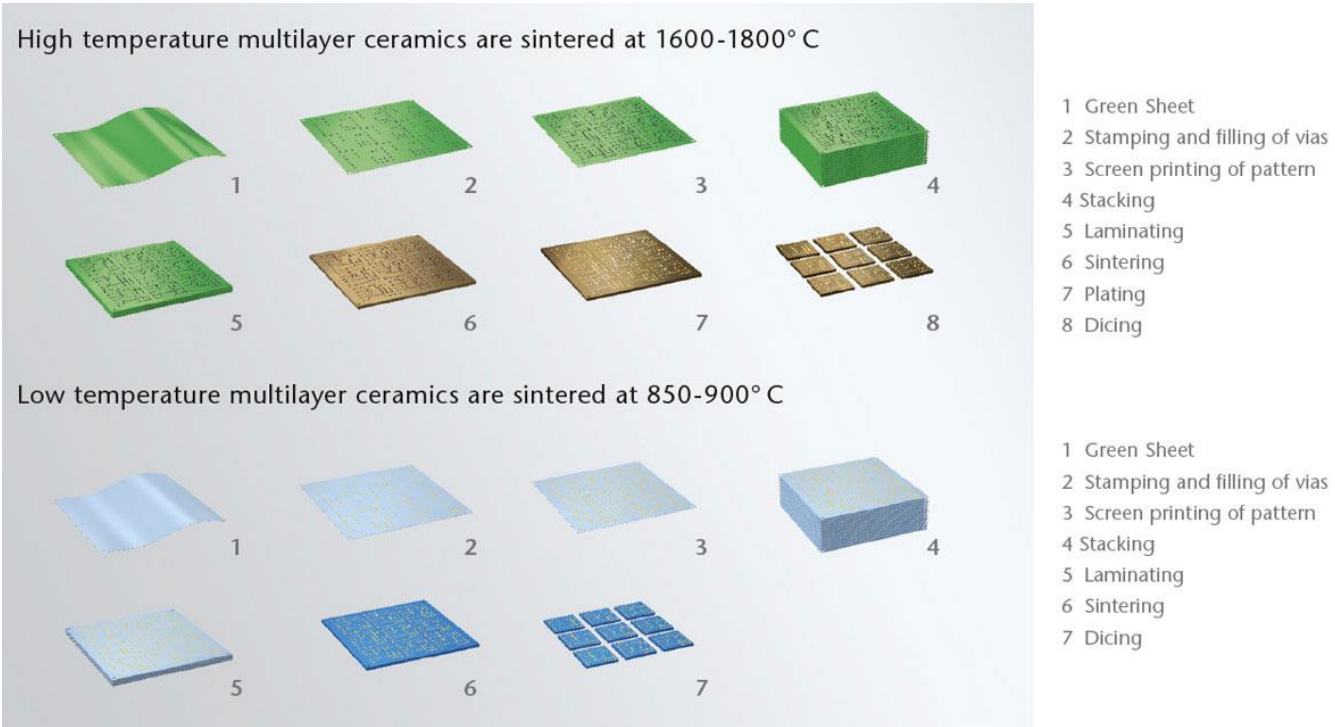

Fig. 2.2.1.2.b. Ceramics variation

2.2.1.2.1 LEADED CHIP CARRIERS:

These are confirmed low profile or rectangular packages that can be mounted directly to a printed board or to a socket. Instead of leads, the packages have interconnected pads around the periphery of the package. The leads of a leaded chip carrier are brazed to the top of the ceramic body prior to forming into a J bend configuration. The J bend leaded chip carrier is selected at higher cost over the J bend CERQUAD in application where there is greater concern about streets induced cracks in seal glass either during forming or subsequent handling operations.

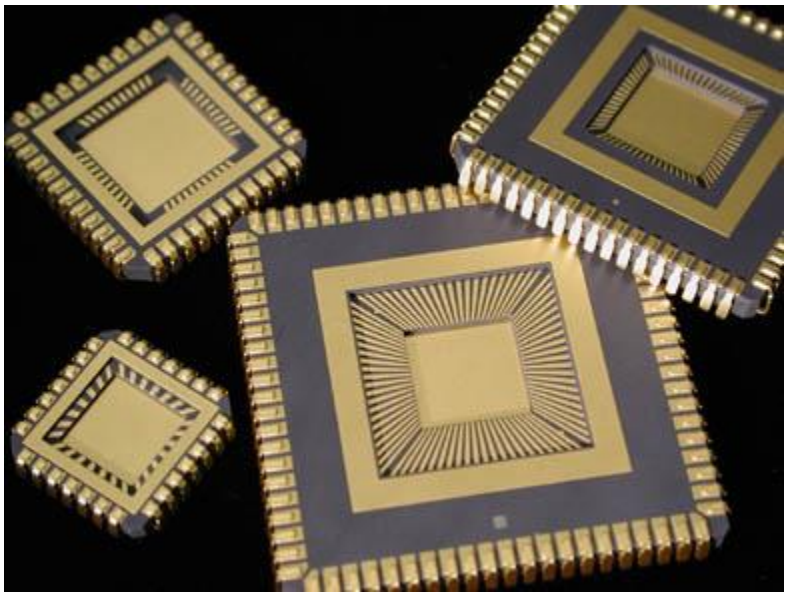

Fig. 2.2.1.2.1.a. Ceramic chip carrier packages

2.2.1.2.2 FLATPACKS:

These are generally thought of as the multilayer version of the CERPACK, although the terms are often used interchangeably. Its use is primarily limited to military applications. When the leads exit the body from all the four sides, the package is referred to as ceramic quad flat package. The leads of this package exit the body parallel to the seating plane. The terms leaded chip carrier and flat pack are often used to describe the same package.

All the packages within the flat pack family can be designed for either cavity up or cavity down use. CQFP with 300-400 leads for single chip are used today. Beyond this range multi-chip modules and chip on board technology appear to offer improvements in the electrical, thermal and mechanical problem areas with very high lead count QFP.

2.2.2 PLASTIC PACKAGES:

These are divided into surface mount and hole mount technique. The common families of surface mount plastic packages are small outline package (SOP), the plastic leaded chip carrier (PLCC) and the plastic quad flat pack (PQFP). Small outline packages are DIP's. Two body sizes are used, the narrow body, with a body width of 3.8mm and the wide body with a width of 7.5mm. Pin counts of 8-16 leads use the narrow body and pin counts of 14-28 use wide body. Package construction consists of a stamped metal lead frame of 0.20mm thickness for a narrow body or 0.25mm for a wide body with a central paddle for chip mounting and spider leads on both sides whose material is either Cu alloy or alloy 42, the paddle and lead tips are electroplated with Ag or Au. The chip is mounted onto the paddle with Ag filled epoxy compounds or it is soldered on with Au eutectic. The chip I/O pads are connected to the tips of lead frame using Au wire. The entire assembly is positioned in the mold and phenol based thermoplastic compound is injected to form the plastic body. External lead finish is accomplished by either solder plating or hot solder dipping and is done after the final shape is formed.

2.2.2.1 PLCC PACKAGES:

These are molded plastic packages with leads on all four sides configuration. Both square and rectangular bodies are used with lead counts of 18-124. Package construction consists of a lead frame spider with a central paddle and leads on all four sides. The package is either stamped or etched out of Cu alloy or alloy 42, 0.25mm thick. The rest of construction is same as that of SOP packages. The J-bend lead form protects the lead tips from mechanical damage.

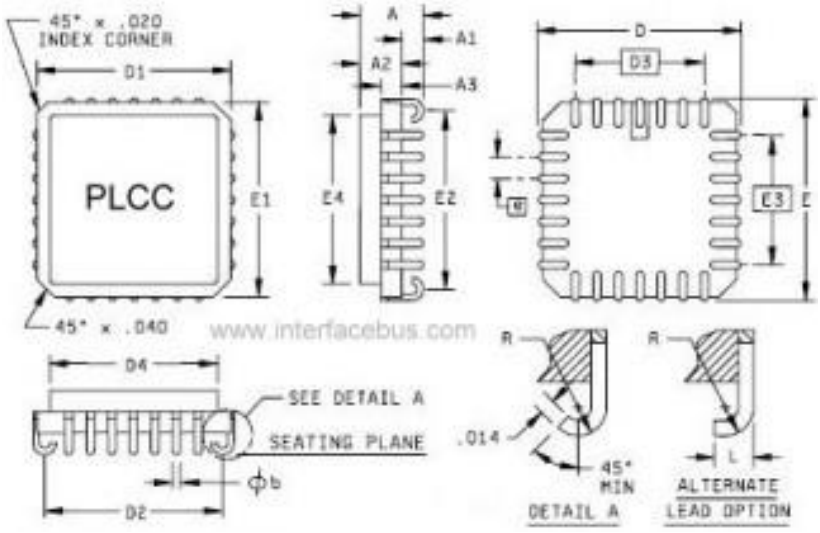

Fig. 2.2.2.1.a. J-lead IC package drawing