ASMA Ver.	0.2.1	TXFPER -	- Test P	ER Tracing of TXF	Transactions	10 Feb 2022 01:49:22 Page	1
LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
LOC	OBJECT CODE	ADDR1	ADDR2	2 ************************************	TXFPER. ********************** **gram performs a PER instruction fetch cludes two transactions. **t transaction, a construction being an unchained transaction nestensies are performed: the find find from Fetch (IF) and Even the actual transaction in the second test adds the IFetch ags to the mix. The second test traced, but in a and TEND instructions	******************************** truction trace of TXF transactions. h events for a range of instructions ained transaction, and a separate onstrained transaction with another d within it. rst test is performed with both the t-Suppression (ES) PER flags set. s except for the instructions that s themselves (i.e. the instructions ost TBEGIN/C instruction through the transaction, are NOT traced). Nullification (IFNUL) and TEND PER ond test should trace everything ddition, should also trace both the themselves too. This is controlled	
				25 * by speci 26 *	al Program Interrupt ha		
00000000		00000000 00000000	00000657		ART 0 SING TXFPER,R0		
00000000 0000008C	0000000	00000000	0000008C	33 PGMCODE DC 34 PGM_PER_EVE	F'0'	Program interrupt code Program interrupt code PER Event program interrupt code	
00000090 00000096 00000098	0000 00000000 00000000	00000090	00000096	35 37 OR 38 PERCODE DC 39 PERADDR DC	XL2'00'	PER interrupt fields PER interrupt code PER interrupt address	
		00000150	00000000	41 PGMOPSW EQ	QU TXFPER+X'150'	z Program Old PSW	
000000A0 000001A0 000001A8	00000001 80000000 00000000 00000200	000000A0	000001A0	43 OR 44 DC 45 DC	X'000000180000000'	z Restart New PSW	
000001A8 000001B0 000001D0 000001D8	00000000 00000200 000000001 80000000 00000000 00000394	000001B0	000001D0		G TXFPER+X'1D0' X'000000180000000'	z Program New PSW	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT					

				51 ** 52 *	******			*********	
					******	Start of actua: *******	*******	• • ***********	
000001E0		000001E0	00000200	55	ORG	TXFPER+X'200'			
				57 *:	******	*******	******	*********	
				58 *		Perform basic TXF	sanity chec	cks	
				59 *	******	*********	******	*********	
99999999	4100 001F		0000001F	61 G	O LA	R0,(L'FACLIST/8)-1		Store Facility List	
00000204	B2B0 0520		00000520	62		FACLIST		Score rucificy List	
	9120 0520 A784 020E		00000520 00000628	64 65	TM JZ	FACLIST+ZAFACBYT,ZAZAFAIL	AFACBIT	z/Arch mode?	
00000200	A/04 UZUE		200000028	65	J∠	LAFAIL			
	9140 0526		00000526	67	TM	FACLIST+PAFACBYT, PA	AFACBIT	PPA available?	
00000214	A784 020E		00000630	68	JZ	PAFAIL			
00000218	9140 0529		00000529	70	ТМ	FACLIST+TXFACBYT,TX	YEACRTT	TXF available?	
	A784 0212		00000323	71	JZ	TXFAIL	XI ACDI I	IXI available:	
	9120 0526		00000526	73 74	TM JZ	FACLIST+CTFACBYT,CTCTFAIL	TFACBIT	Constrained TXF?	
00000224	A784 020A		00000638	/4	JZ	CIFAIL			
				76 *	*********	*******	******	*********	
				77 *		Enable TXI			
				/8 [*]	* * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * *	*********	
00000228	EB00 0620 0025		00000620	80	STCTG	R0,R0,CTL0	Save CR0		
	E300 0620 0004		00000620	81	LG	RØ,CTLØ	Load_into		
00000234 00000238	A508 0080 E300 0620 0024		00000620	82 83	OIHH STG		Enable TXI Save GR0	F flag	
	EB00 0620 002F		00000620	84		R0,CTL0 R0,R0,CTL0	Load CR0		
					******			*********	
				87 * 88 *:	******	Begin tes [†] ********	LS ********	********	
	EB9B 04E0 002F		000004E0	90		R9,R11,PERCTL		CR11 PER Control Registers	
	8000 0518 45E0 0272		00000518 00000272	91 92	SSM BAL	ENPER R14,CTRANS		ogram Event Recording Constrained Transaction	
	45E0 028A		00000272 0000028A	93	BAL	R14,UTRANS		n Unconstrained Transaction	
						•			
	92F2 033C	00000454	0000033C	95 06	MVI	MSGCMD+14,C'2'	Test #2		
	D203 04E4 0648 EB9B 04E0 002F	000004E4	00000648 000004E0	96 97	MVC LCTLG	R9,R11,PERCTL		NUL+CR9_SUPPRESS+CR9_TEND) R11 PER Control Registers	
	45E0 0272		0000072	98	BAL	R14, CTRANS		Constrained Transaction	
0000026A	45E0 028A		0000028A	99	BAL	R14,UTRANS	Execute ar	n Unconstrained Transaction	
0000026E	A7F4 0135		000004D8	100	J	SUCCESS	Done!		

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				103 *		Dummy Transaction	<pre> *********************************</pre>	
		00000272	00000001	106 BEGRANGE	EQU	*	Begin of PER Range	
00000272 00000276	4111 1001 E561 0000 0000		00000001 00000000	108 CTRANS 109	LA TBEGII	R1,1(R1,R1) NC 0,0	Begin Constrained Transaction	
0000027C 00000280 00000284	4122 2002 B2F8 0000 4133 3003		00000002	110 111 112	LA TEND LA	R2,2(R2,R2) R3,3(R3,R3)	End of Transaction	
00000288	07FE		2000000	113	BR	R14	Return to caller	
0000028A 0000028E 00000290 00000296	A729 2000 1FFF E560 2000 FE00 A774 0012		00000000 000002BA	115 UTRANS 116 117 URETRY 118	JNZ	R2,X'2000' R15,R15 N 0(R2),X'FE00' UFAILED	R2> TDB R15 <== failure count = none yet unconstrained, WITH TDB, save R0-R13 CC != 0: aborted or can't be started	
0000029A 0000029E 000002A4 000002A8	4144 4004 E560 0000 0000 4155 5005 B2F8 0000		00000004 00000000 00000005	119 120 121 122	LA TBEGII LA TEND	R4,4(R4,R4) N 0,0 R5,5(R5,R5)	Begin Nested Transaction End of Nested Transaction	
000002AC 000002B0 000002B4	4166 6006 B2F8 0000 4177 7007		00000006 00000007	123 124 125 USKIP	LA TEND LA	Ŕ6,6(R6,R6) R7,7(R7,R7)	End of Outermost Transaction	
000002B8	07FE			126	BR	R14	Return to caller	
000002BA 000002BE	A744 000E A714 0010		000002D6 000002DE	128 UFAILED 129	BRC BRC	CC1,UFAILCC1 CC3,UFAILCC3	<pre>Indeterminate condition (unexpected) Persistent condition (unexpected)</pre>	
000002C2 000002C6	A7FA 0001 A7FE 0003		0000000	131 132	AHI CHI	R15,1 R15,3	Increment temporary failure count Have we reached our maximum retry?	
000002CA 000002CE	A7B4 FFF5 B2E8 10F0		000002B4	133 135	JNL PPA	USKIP R15,0,1	Yes, then do it the hard way Otherwise request assistance	
000002D2	A7F4 FFDF		00000290	136	j	URETRY	And try the transaction again	
000002D6	9206 0517		00000517	138 UFAILCC1		BADPSW+16-1,6	Unexpected CC1	
	A7F4 0101 9207 0517 A7F4 00FD		000004DC 00000517 000004DC	139 140 UFAILCC3 141	J MVI J	FAILURE BADPSW+16-1,7 FAILURE	FAIL test Unexpected CC3 FAIL test	
		000002E6	00000001	143 ENDRANGE	EQU	*	End of PER Range	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				146 *	Issue	Hercules MESSAGE poi	**************************************
000002E6 000002E8	1200 078F			149 MSG 150	LTR BZR	R0,R0 R15	Do we even HAVE a message? No, ignore
000002EA 000002EE 000002F2 000002F6	4900 0650		0000031C 00000650 000002FA 00000015	152 153 154 155	STM CH BNH LA	R0,R2,MSGSAVE R0,=AL2(L'MSGMSG) MSGOK R0,L'MSGMSG	Save registers Message length within limits? Yes, continue No, set to maximum
	1820 0620 4420 0328 4120 2012 4110 032E		00000328 00000012 0000032E	157 MSGOK 158 159 160 161	LR BCTR EX LA LA	R2,R0 R2,0 R2,MSGMVC R2,1+L'MSGCMD(,R2) R1,MSGCMD	Copy length to work register Minus-1 for execute Copy message to O/P buffer Calculate true command length Point to true command
0000030A 0000030E 00000312	83120008 4780 0314 0000		00000314	163 164 165	DC BZ DC	X'83',X'12',X'0008' MSGRET H'0'	<pre>Issue Hercules Diagnose X'008' Return if successful ** CRASH ** otherwise!</pre>
00000314 00000318	9802 031C 07FF		0000031C	167 MSGRET 168	LM BR	R0,R2,MSGSAVE R15	Restore registers Return to caller
0000031C 00000328 0000032E 0000033F	D200 033F 1000	0000033F	00000000	170 MSGSAVE 171 MSGMVC 173 MSGCMD 174 MSGMSG	DC MVC DC DC	3F'0' MSGMSG(0),0(R1) C'MSGNOH * Test 1: ' C'12345678 ==> 12345	Registers save area Executed instruction 6678',C' ' (extra byte for unpk)
				177 *	Trace	instructions that wa	**************************************
	F384 033F 009C 9240 0347 DC07 033F 0294	0000033F 0000033F	0000009C 00000347 00000294	180 ITRACE 181 182	UNPK MVI TR	MSGMSG(9),PERADDR+4(MSGMSG+8,C'' MSGMSG(8),HEXCHARS-X	(5) Address of instruction
	5810 009C F384 034C 1000 DC07 034C 0294		0000009C 00000000 00000294	184 185 186	L UNPK TR	R1,PERADDR+4 MSGMSG+13(9),0(5,R1) MSGMSG+13(8),HEXCHAR	
0000037A	4110 033F 4100 0015 45F0 02E6 07FE		0000033F 00000015 000002E6	188 189 190 191	LA LA BAL BR	R1,MSGMSG R0,L'MSGMSG R15,MSG R14	"Trace" the instruction
00000384	F0F1F2F3 F4F5F6F7			193 HEXCHARS	DC	CL16'0123456789ABCDE	F'

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				196 *		Program Interrupt Hand	**************************************
	9180 008F A784 0098		0000008F 000004C8	199 PGMRUPT 200	TM JZ	PGMCODE+3,PGM_PER_EVENT ABORT	Expected interrupt? No?! ** ABORT!! **
0000039C	EB0F 0448 0024		00000448	201	STMG	R0,R15,PGMREGS	Save caller's registers
000003A6 000003AA 000003AE	4700 03BA 9101 0096 4710 03B6 45E0 0356		000003BA 00000096 000003B6 00000356	203 TEST2BR 204 205 206	NOP TM BO BAL	PGMTEST2 PERCODE,X'01' BEGTEST2 R14,ITRACE	<pre>Branch ==> Test 2 logic CR9_IFNUL = Test 2 yet? Yes, Test 2 has begun Trace executed instruction</pre>
	47F0 043C		0000043C	207	В	PGMRET	(still Test 1)
000003BA 000003C0	92F0 03A3 E310 0098 0004 D501 1000 0652 4780 0408	00000000	000003A3 00000098 00000652 00000408	209 BEGTEST2 210 PGMTEST2 211 212		TEST2BR+1,X'F0' R1,PERADDR 0(2,R1),=XL2'E560' PGMTBEG	Activate Test 2 logic R1> instruction TBEGIN? Yes
000003CA 000003D0	D501 1000 0654 4780 0408	00000000	00000654 00000408	213 214	CLC BE	0(2,R1),=XL2'E561' PGMTBEG	TBEGINC? Yes
	9102 0096 4710 042C		00000096 0000042C	215 216	TM BO	PERCODE,X'02' PGMTEND	TEND PER event? Yes
000003E0	9101 0096 4780 03F8 45E0 0356		00000096 000003F8 00000356	218 219 220	TM BZ BAL	PERCODE,X'01' NOTIFNUL R14,ITRACE	CR9_IFNUL event? No, turn it back on Trace fetched instruction
000003EE	D203 04E4 064C EB9B 04E0 002F 47F0 043C	000004E4	0000064C 000004E0 0000043C	221 222 223	MVC	PERĆTL+4(4),=A(CR9_IF+CR9 R9,R11,PERCTL PGMRET	
000003FE	D203 04E4 0648 EB9B 04E0 002F 47F0 043C	000004E4	00000648 000004E0 0000043C	225 NOTIFNUL 226 227		PERCTL+4(4),=A(CR9_IF+CR9 R9,R11,PERCTL PGMRET	9_IFNUL+CR9_SUPPRESS+CR9_TEND) Turn Nullify back on again Go TRACE next instruction
	9101 0096		00000436		TM	PERCODE,X'01'	CR9 IFNUL event?
0000040C 00000410	4710 0418 9299 0517 A7F4 0064		0000033 00000418 00000517 000004DC	230 231 232	BO MVI J	PGMTBEG2 BADPSW+16-1,X'99' FAILURE	Yes, expected NO!? UNEXPECTED!!
00000418 0000041C 00000422	45E0 0356 D203 04E4 064C EB9B 04E0 002F	000004E4	00000356 0000064C 000004E0	233 PGMTBEG2 234 235	BAL MVC LCTLG	R14,ITRACE PERCTL+4(4),=A(CR9_IF+CR9 R9,R11,PERCTL	Switch to TXSUSPEND mode
	47F0 043C		0000043C	236	В	PGMRET	Go execute the transaction
00000430	45E0 0356 D203 04E4 0648 EB9B 04E0 002F	000004E4	00000356 00000648 000004E0	238 PGMTEND 239 240 241 *	BAL MVC LCTLG B	R14,ITRACE PERCTL+4(4),=A(CR9_IF+CR9 R9,R11,PERCTL PGMRET	Trace the TEND 9_IFNUL+CR9_SUPPRESS+CR9_TEND) Switch back to NULLIFY mode Go trace next instruction
	EB0F 0448 0004 B2B2 0150		00000448 00000150	243 PGMRET 244	LMG LPSWE	R0,R15,PGMREGS PGMOPSW	Restore caller's registers Return to caller
00000448	00000000 00000000			246 PGMREGS	DC	16D'0'	Saved GR registers 0 - 15

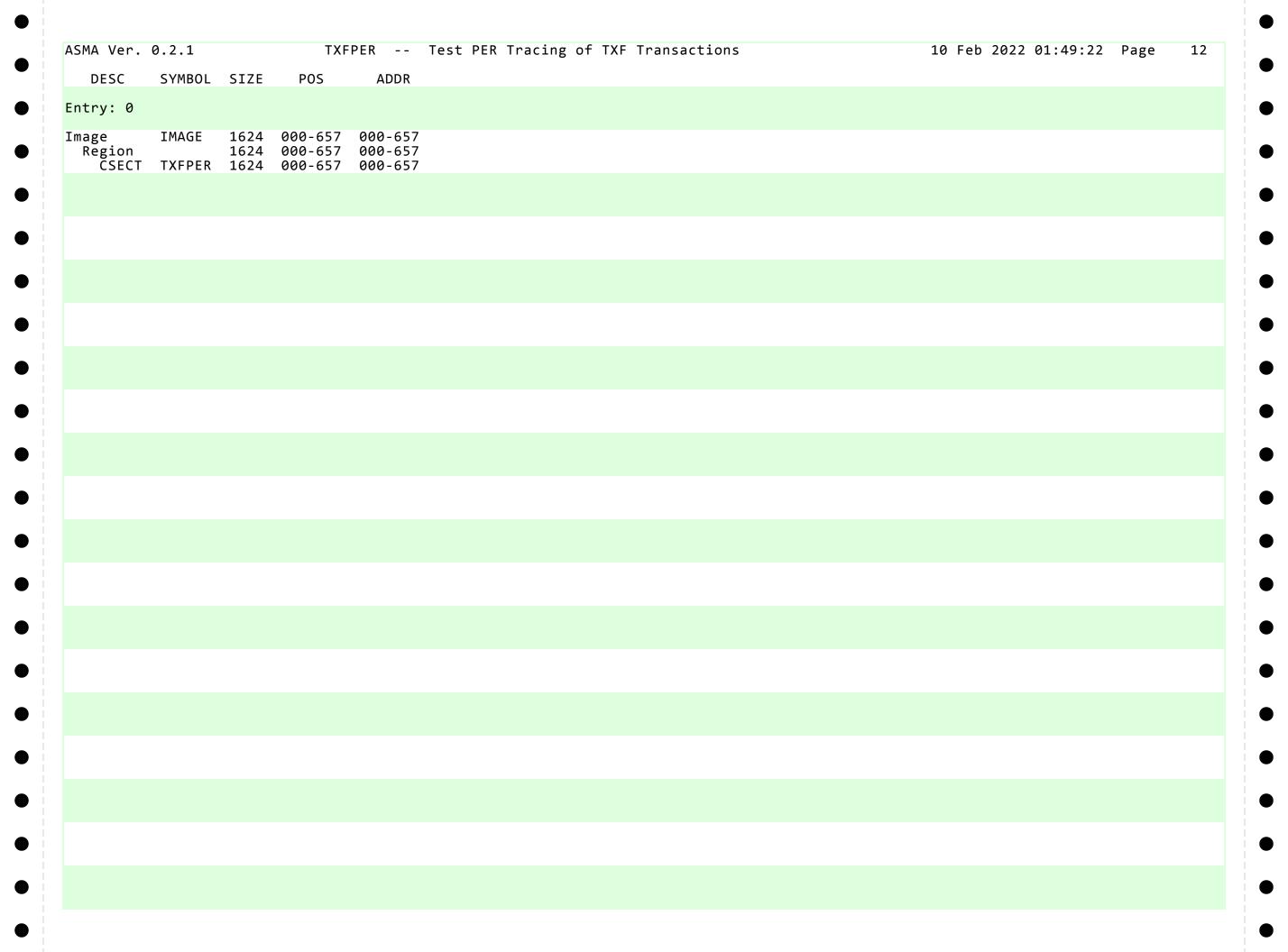
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LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				249 * AE	ORT test run due to unex	**************************************	
000004CE	D201 0512 0656 D203 0514 008C A7F4 0004	00000512 00000514	00000656 0000008C 000004DC	252 ABORT MVC 253 MVC 254 J			
				257 * Su	ccessful completion / Ab	**************************************	
	B2B2 04F8 B2B2 0508		000004F8 00000508	260 SUCCESS LPSW 261 FAILURE LPSW	IE GOODPSW Loa IE BADPSW Loa	nd test completed successfully PSW and the test FAILED somewhere!! PSW	
				264 *	WORKING STORAG	:*************************************	
		4000000 0200000 0100000 0040000		267 CR9_IF 268 CR9_TEND 269 CR9_IFNUL 270 CR9_SUPPRESS	EQU X'02000000' TEN EQU X'01000000' IF	struction Fetch PER event ID Instruction PER event etch Nullification PER event E Event-Suppression PER event	
000004E8	00000000 40400000 00000000 00000272 00000000 000002E6			272 PERCTL DC 273 DC 274 DC	AD(CR9_IF+CR9_SUPPRESS AD(BEGRANGE) AD(ENDRANGE)	CR10 = Range begining address CR11 = Range ending address	
	00020001 80000000 00000000 00000000			276 GOODPSW DC 277 DC	XL8'0002000180000000' XL4'00000000',A(X'0000	00000')	
	00020001 80000000 0000DEAD 000000FF			279 BADPSW DC 280 DC	XL8'0002000180000000' XL4'0000DEAD',A(X'0000	000FF') (FF = Reason for Failure)	
00000518	40			282 ENPER DC	B'01000000'	Enable PER bit in PSW	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				285 *		WORKING	**************************************	
00000520 00000520	00000000 00000000			288 289 FACLIST	DC DC	0D'0' XL256'00'	(doubleword boundary) Facility List	
00000620	00000000 00000000	00000080 00000004 00000001	00000001 00000001 00000001	291 CTL0 292 CR0TXF 293 CC1 294 CC3	DC EQU EQU EQU	D'0' X'0080' B'0100' B'0001'	Control Register 0 CRO bit 8: TXF Control Condition Code 1 Condition Code 3	
00000628 0000062C	9201 0517 A7F4 FF58	00000002 00000000 00000020	00000001 00000001 00000001 00000517 000004DC	296 ZAFACNUM 297 ZAFACBYT 298 ZAFACBIT 299 ZAFAIL 300	EQU	2 X'00' X'20' BADPSW+16-1,1 FAILURE	z/Arch mode	
	9202 0517 A7F4 FF54	00000031 00000006 00000040	00000001 00000001 00000001 00000517 000004DC	302 PAFACNUM 303 PAFACBYT 304 PAFACBIT 305 PAFAIL 306	EQU	49 X'06' X'40' BADPSW+16-1,2 FAILURE	PPA (Processor-Assist)	
00000638 0000063C	9203 0517 A7F4 FF50	00000032 00000006 00000020	00000001 00000001 00000001 00000517 000004DC	308 CTFACNUM 309 CTFACBYT 310 CTFACBIT 311 CTFAIL 312	EQU	50 X'06' X'20' BADPSW+16-1,3 FAILURE	Constrained TXF	
00000640 00000644	9204 0517	00000049 00000009 00000040	00000001 00000001 0000001 00000517 000004DC	314 TXFACNUM 315 TXFACBYT 316 TXFACBIT 317 TXFAIL 318	EQU	73 X'09' X'40' BADPSW+16-1,4 FAILURE	TXF	

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LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				321 *	Liter	rals Pool	**************************************	
				_				
0000648 0000648 000064C 0000650	43400000 42400000 0015			324 325 326 327	LTOR		UL+CR9_SUPPRESS+CR9_TEND) PRESS+CR9_TEND)	
0000652 0000654 0000656	E560 E561 DEAD			328 329 330		=XL2'E560' =XL2'E561' =XL2'DEAD'		
				337 ******	:*****	·****************	***********	
				333 *	Regis	ster equates	************	
		00000001 00000002 00000003 00000004 00000005 00000006 00000007 00000008 00000009	0000001 0000001 0000001 0000001 0000001 000000	336 R0 337 R1 338 R2 339 R3 340 R4 341 R5 342 R6 343 R7 344 R8 345 R9	EQU EQU EQU EQU EQU EQU EQU	0 1 2 3 4 5 6 7 8		
		0000000B 0000000C 0000000D 0000000E	00000001 00000001 00000001 00000001 000000	346 R10 347 R11 348 R12 349 R13 350 R14 351 R15	EQU EQU EQU EQU EQU	10 11 12 13 14 15		
				353	END			

CVADOL	T\/5=	TXFPER								-				_0		2022 (- 	Page	9
SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFE	RENCE	S													
BORT	I	000004C8	6	252	200															
ADPSW	Χ	00000508	8	279	138	140	231	252	253	261	299	305	311	317						
EGRANGE	U	00000272	1	106	273															
EGTEST2	I	000003B6	4	209	205															
CC1	U	00000004	1	293	128															
CC3	U	00000001	1	294	129															
ROTXF	U	00000080	1	292	82															
R9_IF	U	40000000	1	267	272	96	221													
R9_IFNUL	U	01000000	1	269	96															
R9_SUPPRESS	U	00400000	1	270	272	96	221													
R9_TEND	U	02000000	1	268	96	221														
CTFACBIT	U	00000020	1	310	73															
TFACBYT	U	00000006	1	309	73															
TFACNUM	U	00000032	1	308																
TFAIL	I	00000638	4	311	74															
TL0	D	00000620	8	291	80	81	83	84												
TRANS	I	00000272	4	108	92	98														
NDRANGE	U	000002E6	1	143	274															
NPER	В	00000518	1	282	91															
ACLIST	Χ	00000520	256	289	61	62	64	67	70	73										
AILURE	I	000004DC	4	261	139	141	232	254	300	306	312	318								
i0	I	00000200	4	61	45															
GOODPSW	Χ	000004F8	8	276	260															
IEXCHARS	С	00000384	16	193	182	186														
MAGE	1	00000000	1624	0																
TRACE	I	00000356	6	180	206	220	233	238												
1SG	I	000002E6	2	149	190															
1SGCMD	C	0000032E	17	173	95	160	161													
ISGMSG	C	0000033F	21	174	155	171	180	181	182	185	186	188	189	153						
ISGMVC	I	00000328	6	171	159															
1SG0K	I	000002FA	2	157	154															
ISGRET	I	00000314	4	167	164															
ISGSAVE	F	0000031C	4	170	152	167														
IOTIFNUL	I	000003F8	6	225	219															
PAFACBIT	U	00000040	1	304	67															
PAFACBYT	U	0000006	1	303	67															
PAFACNUM	U	00000031	1	302																
PAFAIL	I	00000630	4	305	68															
PERADDR	Α	00000098	8	39	180	184	210													
PERCODE	Χ	00000096	2	38	204	215	218	229												
PERCTL	Α	000004E0	8	272	90	96	97	221	222	225	226	234	235	239	240					
GMCODE	F	0000008C	4	33	199	253														
PGMOPSW	U	00000150	0	41	244															
GMREGS	D	00000448	8	246	201	243														
GMRET	I	0000043C	6	243	207	223	227	236												
PGMRUPT	I	00000394	4	199	49	_		-												
GMTBEG	I	00000408	4	229	212	214														
GMTBEG2	Ī	00000418	4	233	230															
PGMTEND	Ī	0000042C	4	238	216															
GMTEST2	Ī	000003BA	6	210	203															
OM PER EVENT	Ū	00000080	1	34	199															
10	Ü	00000000	1	336	30	61	80	81	82	83	84	149	152	153	155	157	167	189	201	
. •	3		_	230	50	0 1	30	31	52	33	5 -	± T/				± J ,	-0,	-07	201	

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No defined macros					



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STMT	FILE NAME	10 100 2022 01.43.22 rage	13
C. (0261.2 / F1211 / DC	ocuments\Visual Studio 2008\Projects\MyProjects\ASMA-0\TXFPER\TXFPER.asm		
** NO ERRORS FOUND **			