1. Description
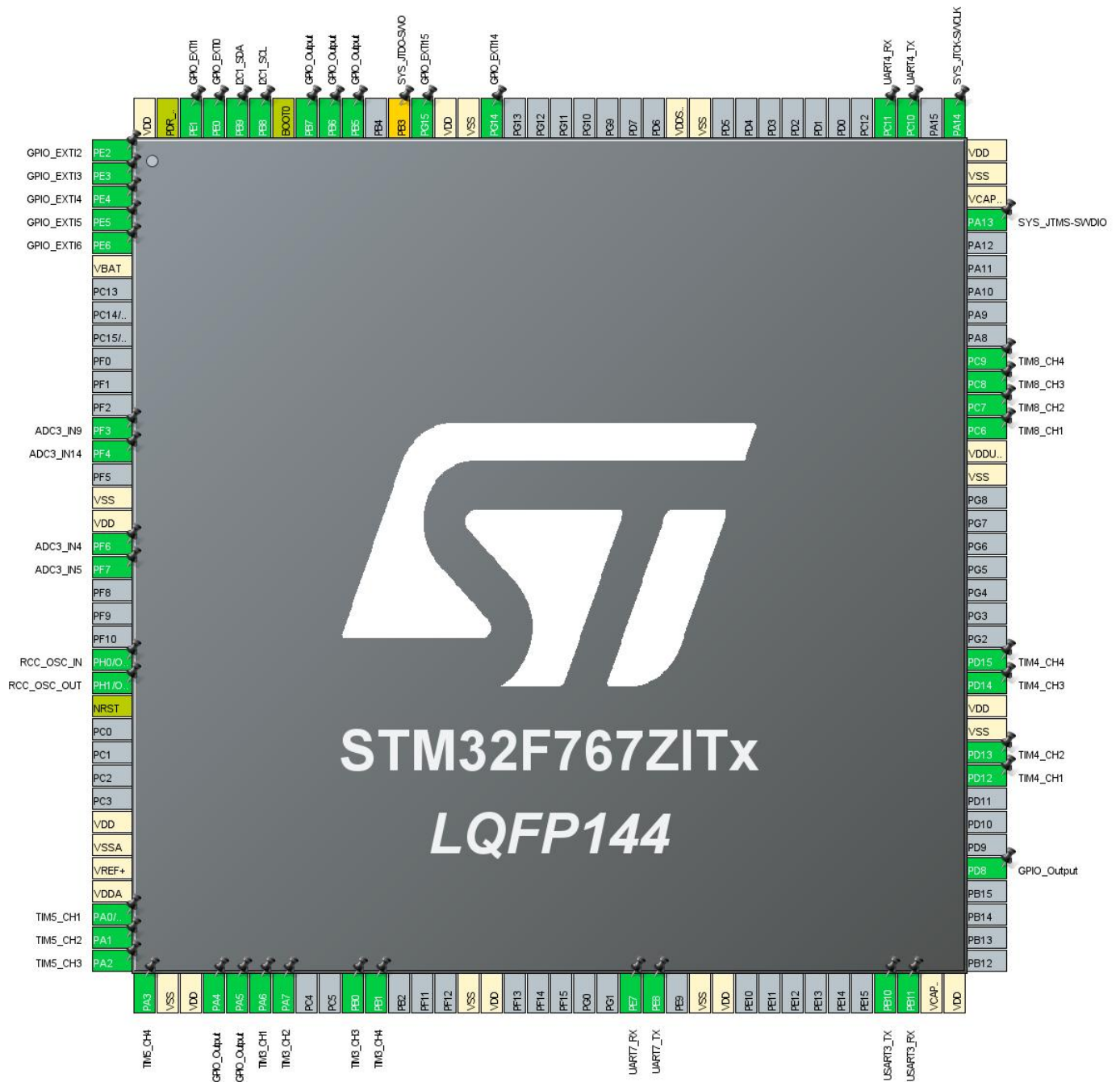
1.1. Project

Project Name	F767_codename_U
Board Name	custom
Generated with:	STM32CubeMX 5.5.0
Date	04/02/2025

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

3. Pins Configuration

| Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	GPIO_EXTI2	
2	PE3	I/O	GPIO_EXTI3	
3	PE4	I/O	GPIO_EXTI4	
4	PE5	I/O	GPIO_EXTI5	
5	PE6	I/O	GPIO_EXTI6	
6	VBAT	Power		
13	PF3	I/O	ADC3_IN9	
14	PF4	I/O	ADC3_IN14	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	ADC3_IN4	
19	PF7	I/O	ADC3_IN5	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM5_CH1	
35	PA1	I/O	TIM5_CH2	
36	PA2	I/O	TIM5_CH3	
37	PA3	I/O	TIM5_CH4	
38	VSS	Power		
39	VDD	Power		
40	PA4 *	I/O	GPIO_Output	
41	PA5 *	I/O	GPIO_Output	
42	PA6	I/O	TIM3_CH1	
43	PA7	I/O	TIM3_CH2	
46	PB0	I/O	TIM3_CH3	
47	PB1	I/O	TIM3_CH4	
51	VSS	Power		
52	VDD	Power		
58	PE7	I/O	UART7_RX	
59	PE8	I/O	UART7_TX	
61	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
62	VDD	Power		
69	PB10	I/O	USART3_TX	
70	PB11	I/O	USART3_RX	
71	VCAP_1	Power		
72	VDD	Power		
77	PD8 *	I/O	GPIO_Output	
81	PD12	I/O	TIM4_CH1	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	TIM4_CH3	
86	PD15	I/O	TIM4_CH4	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	TIM8_CH2	
98	PC8	I/O	TIM8_CH3	
99	PC9	I/O	TIM8_CH4	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
111	PC10	I/O	UART4_TX	
112	PC11	I/O	UART4_RX	
120	VSS	Power		
121	VDDSDMMC	Power		
129	PG14	I/O	GPIO_EXTI14	
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	GPIO_EXTI15	
133	PB3 **	I/O	SYS_JTDO-SWO	
135	PB5 *	I/O	GPIO_Output	
136	PB6 *	I/O	GPIO_Output	
137	PB7 *	I/O	GPIO_Output	
138	BOOT0	Boot		
139	PB8	I/O	I2C1_SCL	
140	PB9	I/O	I2C1_SDA	
141	PE0	I/O	GPIO_EXTI0	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
142	PE1	I/O	GPIO_EXTI1	
143	PDR_ON	Reset		
144	VDD	Power		

 * The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration
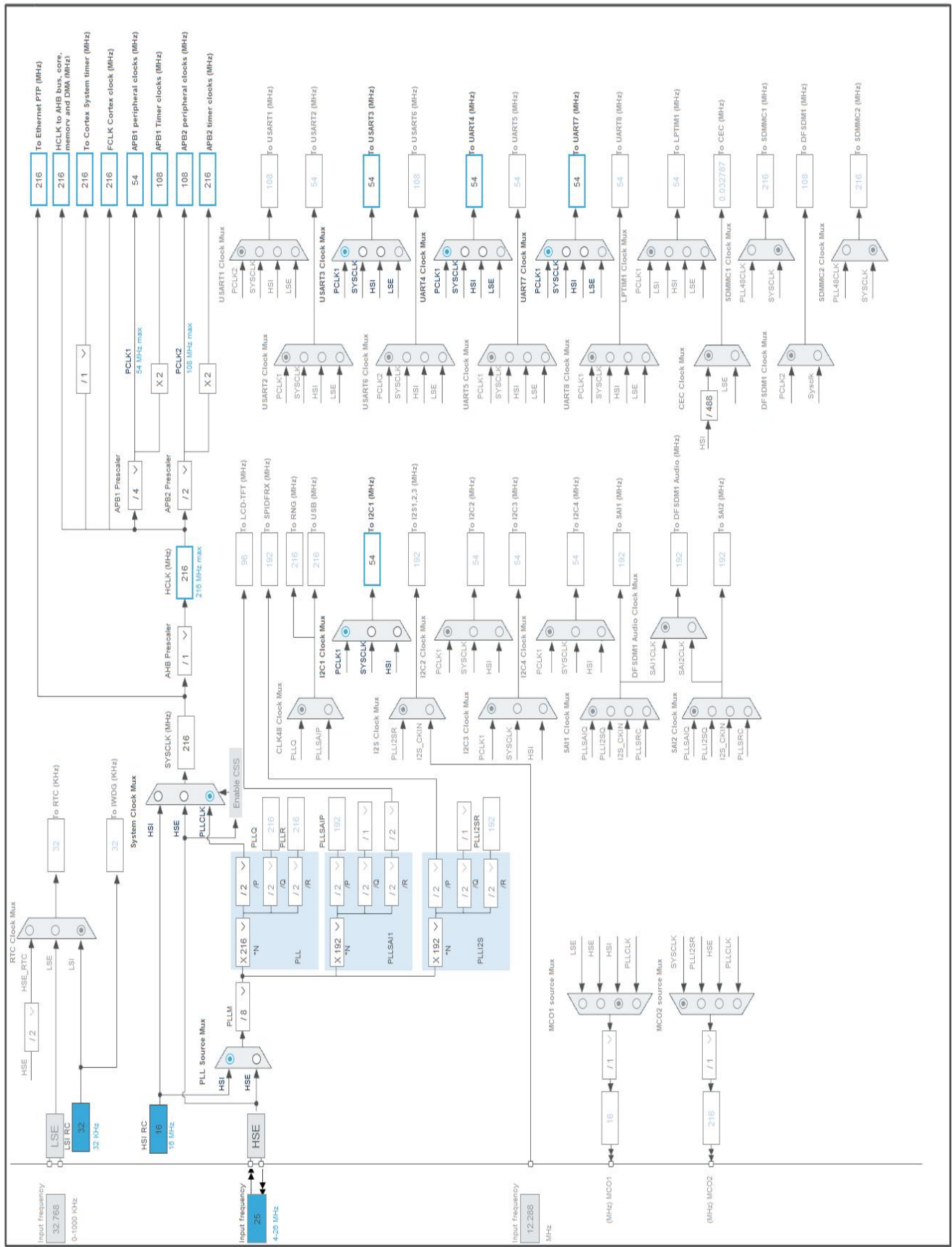
5. Software Project

5.1. Project Settings

Name	Value
Project Name	F767_codename_U
Project Folder	C:\Users\fukuj\STM32CubeIDE\workspace_1.2.0\F767_codename_U
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC3

mode: IN4

mode: IN5

mode: IN9

mode: IN14

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	**10 bits (13 ADC Clock cycles) ***
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 9 ***
Sampling Time	**56 Cycles ***
Rank	**2 ***
Channel	**Channel 14 ***
Sampling Time	**56 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. GPIO

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.5. SYS

Debug: Serial Wire
Timebase Source: SysTick

7.6. TIM3

Clock Source   : Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**80 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.7. TIM4

Clock Source   : Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2160-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable

CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM5

mode: Clock Source
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**80-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.9. TIM8

Clock Source   : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**4320-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.10. UART4

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. UART7

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. USART3

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC3	PF3	ADC3_IN9	Analog mode	No pull-up and no pull-down	n/a	
	PF4	ADC3_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PF6	ADC3_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PF7	ADC3_IN5	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0/WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
UART7	PE7	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PE8	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
GPIO	PE2	GPIO_EXTI2	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	
	PE3	GPIO_EXTI3	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	
	PE4	GPIO_EXTI4	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	
	PE5	GPIO_EXTI5	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	
	PE6	GPIO_EXTI6	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG14	GPIO_EXTI14	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	
	PG15	GPIO_EXTI15	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE0	GPIO_EXTI0			n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			External Interrupt Mode with Rising/Falling edge	**Pull-up ***		
	PE1	GPIO_EXTI1	**External Interrupt Mode with Rising/Falling edge**	**Pull-up ***	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC3	DMA2_Stream0	Peripheral To Memory	**Medium ***

ADC3: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	0	0
EXTI line1 interrupt	true	0	0
EXTI line2 interrupt	true	0	0
EXTI line3 interrupt	true	0	0
EXTI line4 interrupt	true	0	0
ADC1, ADC2 and ADC3 global interrupts	true	1	0
EXTI line[9:5] interrupts	true	0	0
EXTI line[15:10] interrupts	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
UART4 global interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		

* **User modified value**

9. Software Pack Report