

1. Description

1.1. Project

Project Name	F767_unit_1
Board Name	custom
Generated with:	STM32CubeMX 5.5.0
Date	08/13/2024

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

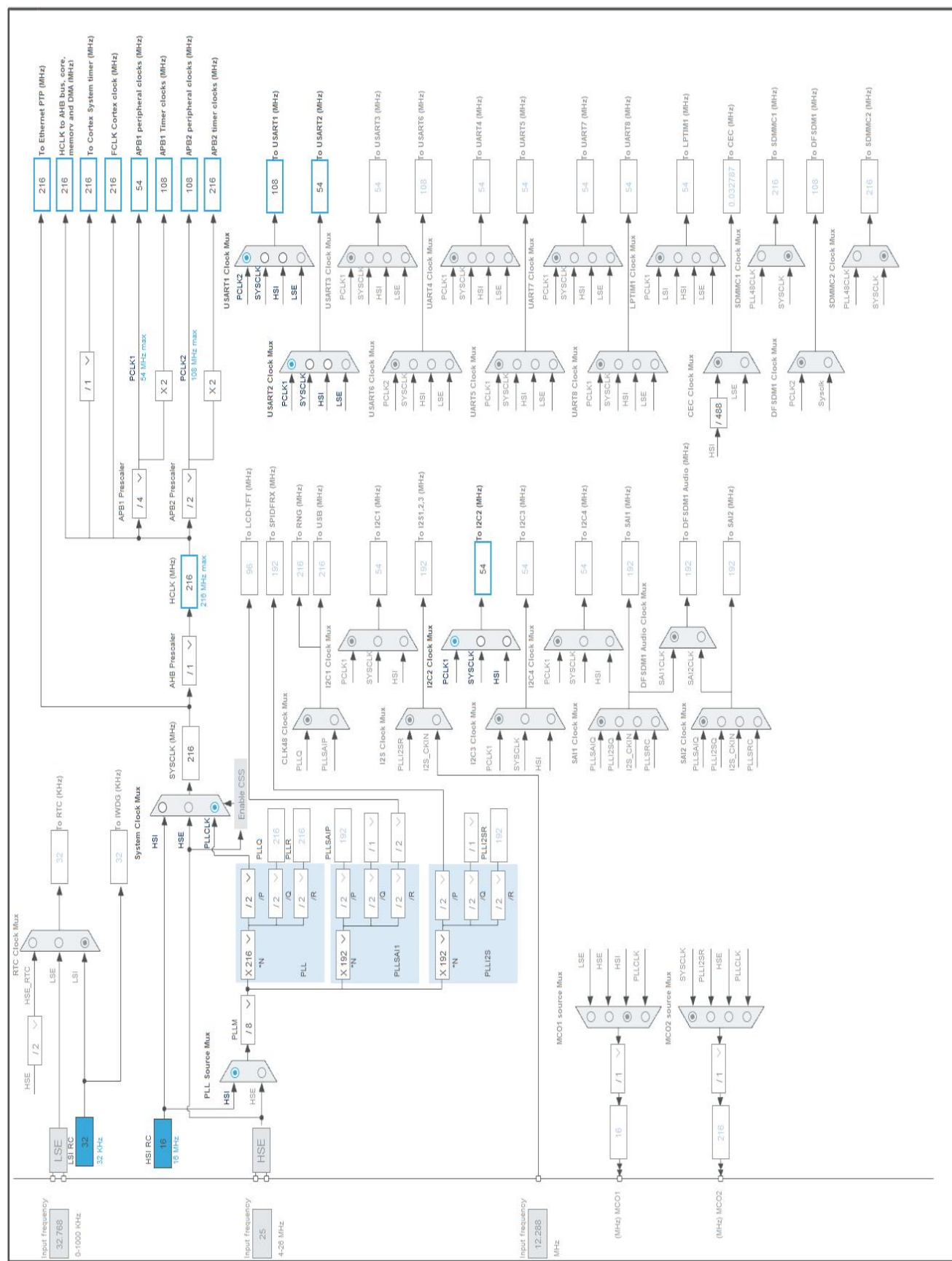
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
28	PC2 *	I/O	GPIO_Output	enable_7
29	PC3 *	I/O	GPIO_Output	enable_6
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM5_CH1	
35	PA1	I/O	TIM5_CH2	
36	PA2	I/O	TIM5_CH3	
37	PA3	I/O	TIM5_CH4	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	GPIO_EXTI4	
41	PA5	I/O	TIM2_CH1	
42	PA6	I/O	TIM3_CH1	
46	PB0 *	I/O	GPIO_Output	
47	PB1	I/O	TIM3_CH4	
48	PB2	I/O	GPIO_EXTI2	Botton_Black
49	PF11	I/O	GPIO_EXTI11	Botton_Red
50	PF12	I/O	GPIO_EXTI12	Botton_Blue
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	GPIO_EXTI13	
54	PF14	I/O	GPIO_EXTI14	
55	PF15	I/O	GPIO_EXTI15	
56	PG0 *	I/O	GPIO_Output	Enable_1
57	PG1 *	I/O	GPIO_Output	Enable_2
58	PE7 *	I/O	GPIO_Output	Enable_4
59	PE8 *	I/O	GPIO_Output	Enable_3_5
60	PE9	I/O	TIM1_CH1	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
61	VSS	Power		
62	VDD	Power		
63	PE10 *	I/O	GPIO_Output	LED_White
64	PE11 *	I/O	GPIO_Output	LED_Green
65	PE12 *	I/O	GPIO_Output	LED_Red
66	PE13 *	I/O	GPIO_Output	LED_Yellow
67	PE14	I/O	TIM1_CH4	
69	PB10	I/O	TIM2_CH3	
70	PB11	I/O	TIM2_CH4	
71	VCAP_1	Power		
72	VDD	Power		
75	PB14	I/O	USART1_TX	
76	PB15	I/O	USART1_RX	
79	PD10	I/O	GPIO_EXTI10	
81	PD12	I/O	TIM4_CH1	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	TIM4_CH3	
86	PD15	I/O	TIM4_CH4	
88	PG3	I/O	GPIO_EXTI3	
90	PG5	I/O	GPIO_EXTI5	
91	PG6 *	I/O	GPIO_Output	
92	PG7 *	I/O	GPIO_Output	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	TIM8_CH2	
98	PC8	I/O	TIM3_CH3	
99	PC9	I/O	TIM8_CH4	
101	PA9	I/O	TIM1_CH2	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
114	PD0	I/O	GPIO_EXTI0	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6	I/O	USART2_RX	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	TIM2_CH2	
135	PB5	I/O	TIM3_CH2	
138	BOOT0	Boot		
139	PB8	I/O	TIM10_CH1	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	F767_unit_1
Project Folder	C:\Users\fukuj\STM32CubeIDE\workspace_1.2.0\F767_unit_1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCELERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED
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7.2. GPIO

7.3. I2C2

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x20404768 *

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. RCC

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.5. SYS

Timebase Source: SysTick

7.6. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel4: PWM Generation CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	4320-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.7. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	216-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	216-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable

CH Polarity	High
PWM Generation Channel 4:	
Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.9. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	216-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.10. TIM5

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	216-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.11. TIM6

mode: Activated

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	10800-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	50000-1 *
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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7.12. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel4: PWM Generation CH4

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	4320-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable

CH Polarity	High
CH Idle State	Reset
PWM Generation Channel 4:	
Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.13. TIM9

mode: Clock Source

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	216-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

7.14. TIM10

mode: Activated

Channel1: PWM Generation CH1

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	4320-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	1000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High

7.15. USART1

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. USART2

Mode: Asynchronous

7.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
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Over Sampling	16 Samples
Single Sample	Disable
Advanced Features:	
Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Enable *
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	Very High *	
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	Very High *	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0/WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM10	PB8	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB14	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
GPIO	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	enable_7
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	enable_6
	PA4	GPIO_EXTI4	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_EXTI2	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	Botton_Black
	PF11	GPIO_EXTI11	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	Botton_Red
	PF12	GPIO_EXTI12	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	Botton_Blue
	PF13	GPIO_EXTI13	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	
	PF14	GPIO_EXTI14	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	
	PF15	GPIO_EXTI15	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Enable_1
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Enable_2
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Enable_4
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Enable_3_5
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_White
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_Green
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_Red
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_Yellow
	PD10	GPIO_EXTI10	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	
	PG3	GPIO_EXTI3	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	
	PG5	GPIO_EXTI5		No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			External Interrupt Mode with Rising/Falling edge			
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD0	GPIO_EXTI0	External Interrupt Mode with Rising/Falling edge	No pull-up and no pull-down	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA2_Stream2	Peripheral To Memory	High *
USART2_RX	DMA1_Stream5	Peripheral To Memory	Very High *

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	0	0
EXTI line2 interrupt	true	0	0
EXTI line3 interrupt	true	0	0
EXTI line4 interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
DMA2 stream2 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM8 capture compare interrupt		unused	
TIM5 global interrupt		unused	
FPU global interrupt		unused	

* User modified value

9. Software Pack Report