ⓘ Dashed red lines indicate isolation barriers between TS and LV.

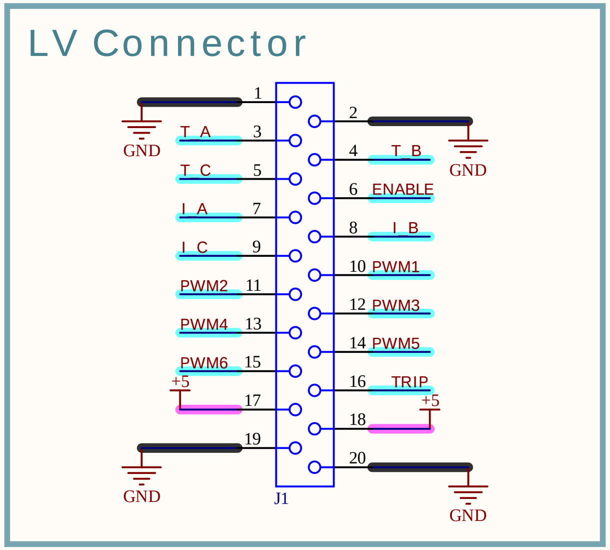
ⓘ Cyan areas indicate GLVS and cyan nets indicate signals from/to GLVS.

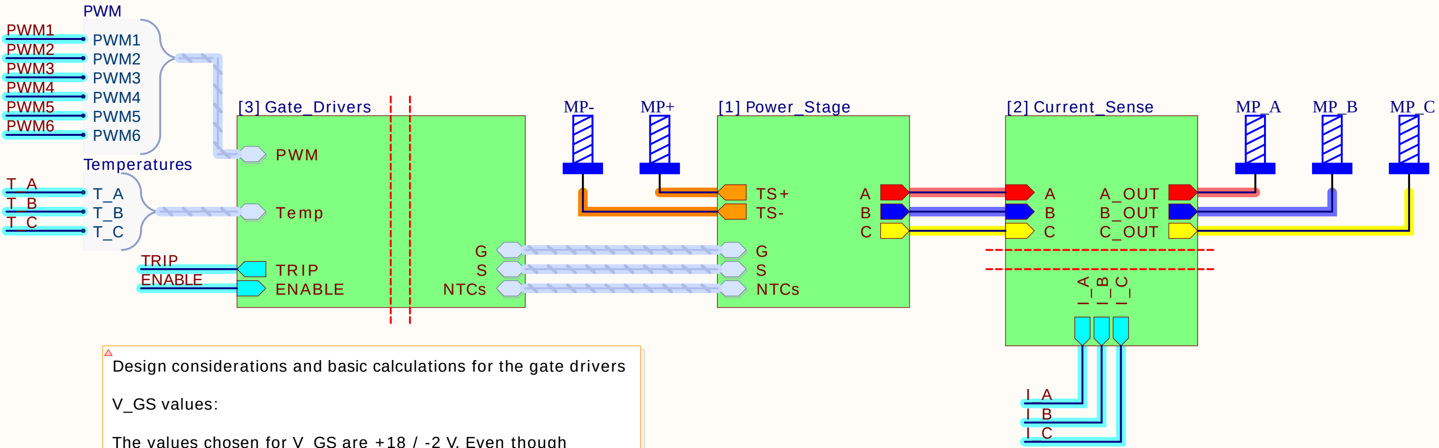
ⓘ Orange areas indicate TS and orange nets indicate high power TS.

Specifications:

$V_{in,\,max}$ = 600 VDC
$V_{out,\,max}$ = 245 VRMS (SVPWM)
f_{sw} = 50 kHz
P_{out_max} = 40kW
I_{out_max} = 80 ARMS

Liquid cooled with water at 50ºC max





Design considerations and basic calculations for the gate drivers

V_{GS} values:

The values chosen for V_{GS} are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum $V_{GS(th)}$. A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
$I_{GD(min)} = f_{sw} \cdot Q_G = 50\text{ kHz} \cdot 520\text{ nC} = 26\text{ mA}$
$P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20\text{ V} \cdot 26\text{ mA} = 0.52\text{ W} \rightarrow 1\text{ W}$

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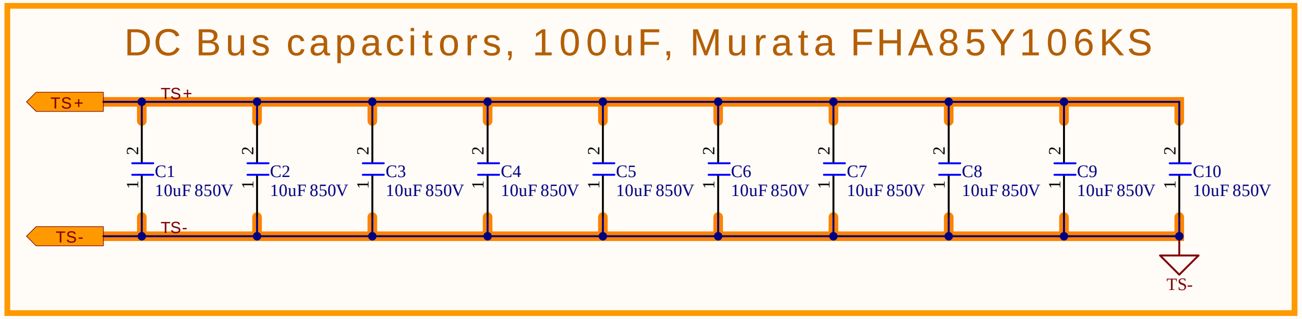


DC Link design considerations:

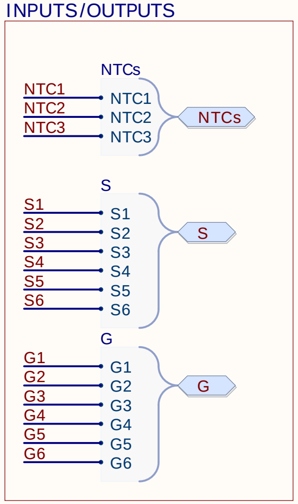
$V_C > 1.1 \cdot V_{max} = 1.1 \cdot 600\ V = 660\ V \rightarrow 850\ V$

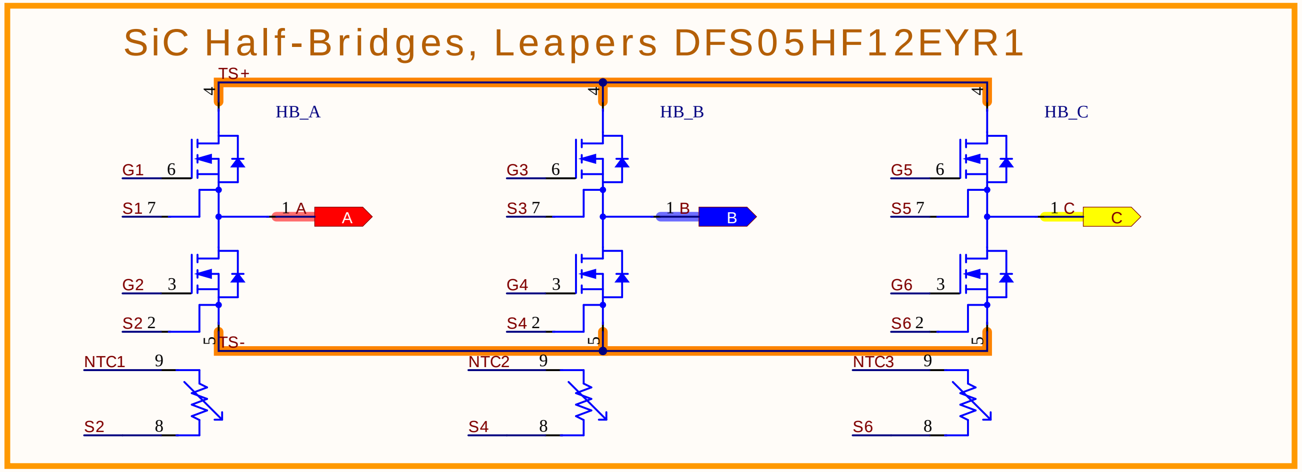
$I_{C,RMS} \approx 0.65 \cdot I_{phase,RMS} = 0.65 \cdot 80\ A_{RMS} = 52\ A_{RMS} \rightarrow 10 \times 5\ A_{RMS}$ ($\Delta T = 10$ ºC)

$C > I_{C,RMS} / (V_{ripple} \cdot f_{sw}) = 52\ A_{RMS} / (15V \cdot 50\ kHz) \approx 79\ \mu F \rightarrow 10 \times 10\ \mu F$

Check:
https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter

INPUTS/OUTPUTS





Semiconductor details:

$V_{DSS(breakdown)} = 1200$ V
Ron = 5.5 .. 13 mΩ
$V_{f\_D} = 3.3$ .. 4 V
$T_{rr} = 41.5$ .. 45 ns
$Q_{rr} = 2.19$ .. 3.94 µC
$R_{th\_jc} = 0.12$ .. 0.15 K/W
Q_G (600V, 150A, V_{GS} = +15/0V) = 520 nC
$C_{in} = 14.5$ nF
$R_{G(int)} = 1.9$ Ω
$V_{GS(th)} = 2.8$ .. 4.8 V

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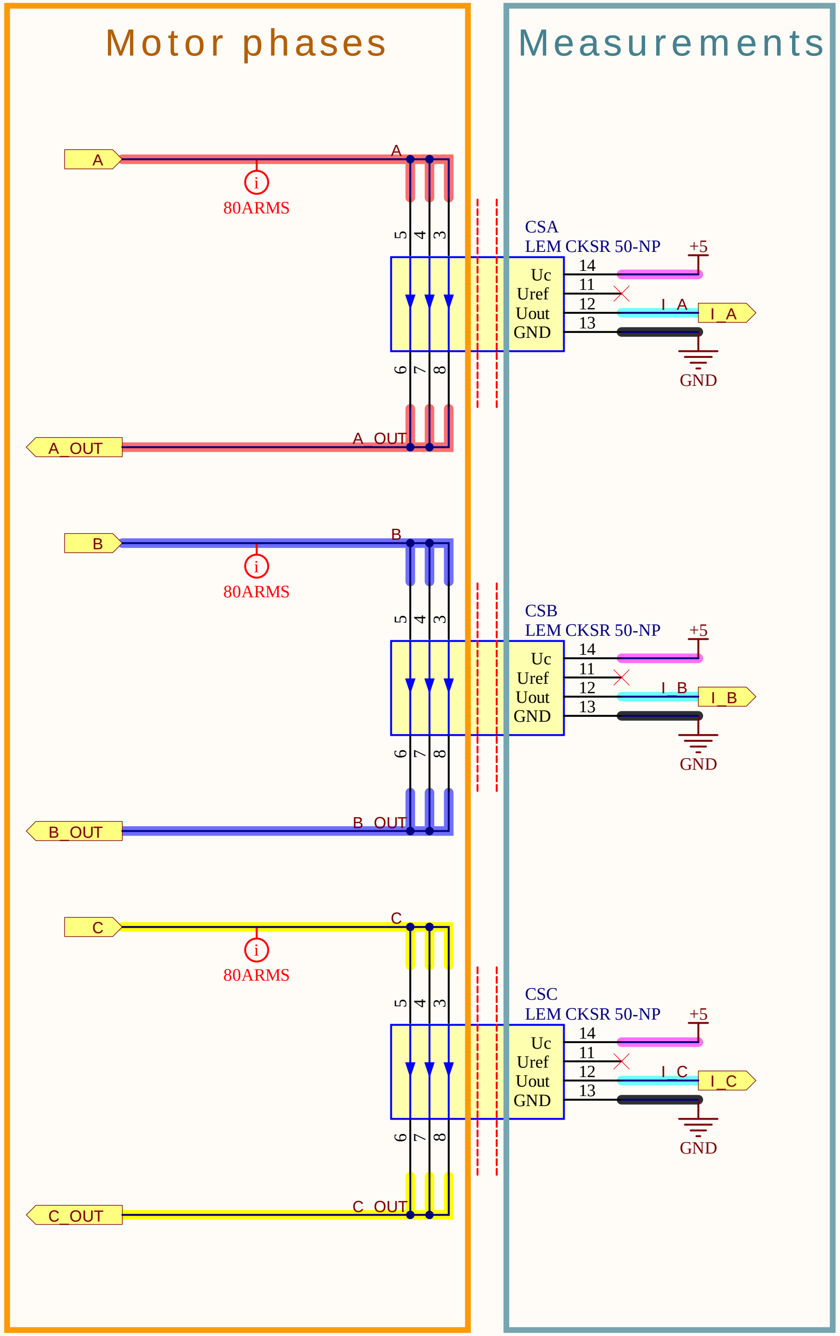
CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)

CSA , CSB , CSC

AC insulation test
RMS voltage, 50 Hz,
1 min:

Ud = 4.3 kV >
3*V_max = 1.8 kV



CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values

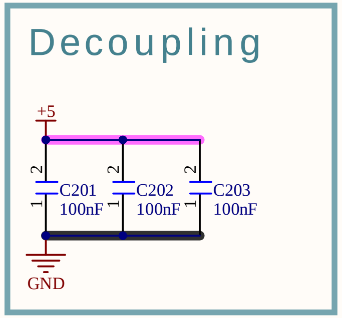
I_A , I_B , I_C

U_meas = (12.5mV/A · I_meas + 2.5V)

For ±150Apk:
U_meas_pk+ = 4.375V
U_meas_pk- = 0.625V

C201 , C202 , C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).



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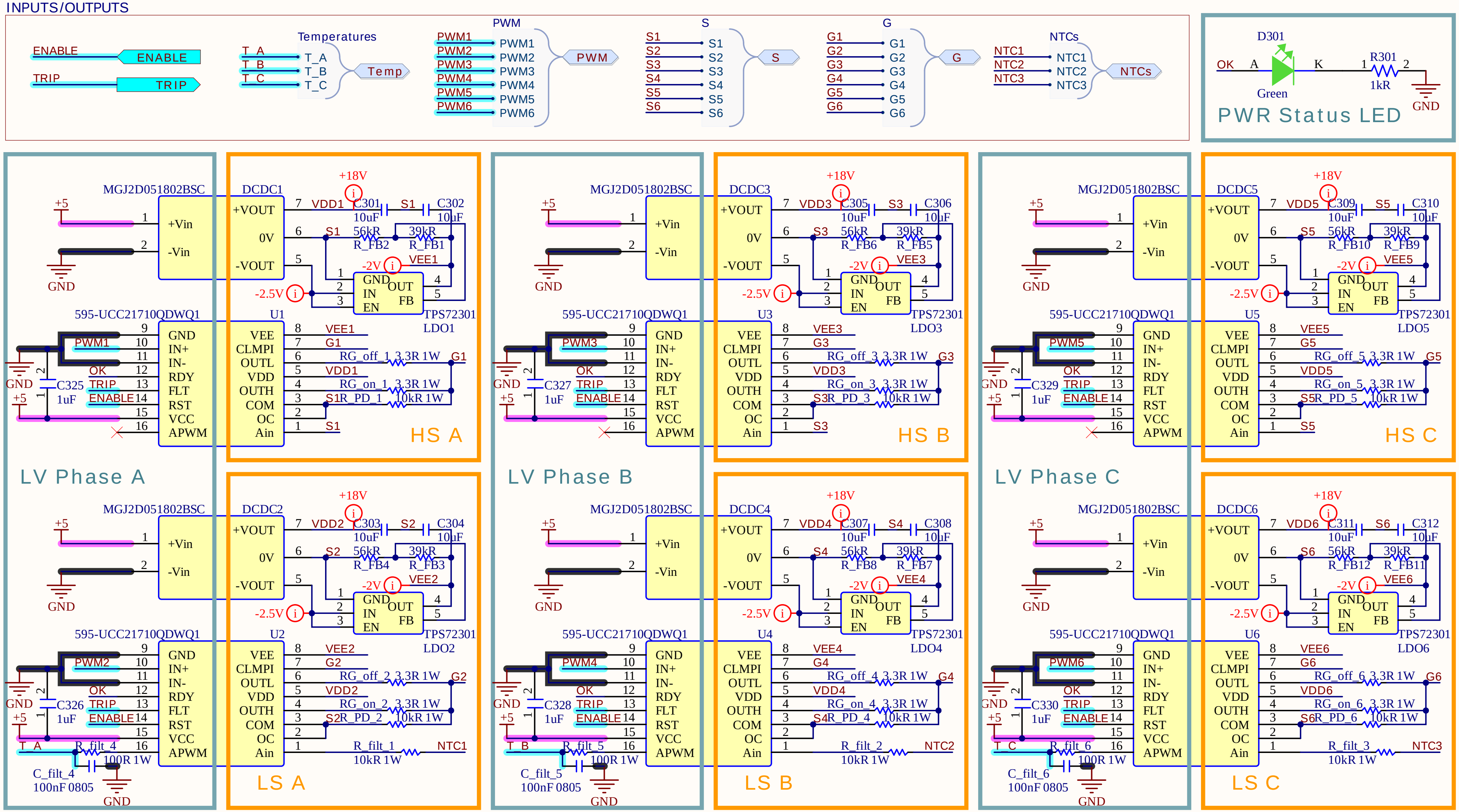

U1, U2, U3, U4, U5, U6

1. TRIP and OK signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to GND.
3. ENABLE to be given by MCU in active-high mode. When set to low for more than 1us, TRIP is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200uA. SPICE simulation in parent directory. PWM to analog using a RC filter, to be fed directly to MCU ADC.
5. Miller clamp protection is used.
6. R_PD_1, R_PD_2, R_PD_3, R_PD_4, R_PD_5, R_PD_6: External gate pull-down is implemented.
7. Overcurrent detection is not implemented.

LDO1, LDO2, LDO3, LDO4, LDO5, LDO6

Feedback voltage divider adjusted to -2V, providing
V_GS = +18 V / -2 V

Adjust feedback if needed.

DCDC1, DCDC2, DCDC3, DCDC4, DCDC5, DCDC6
Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U1, U2, U3, U4, U5, U6
VIOTM (t = 60 s (qualification test)): 8000 VPK

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