ⓘ Dashed red lines indicate isolation barriers between TS and LV.

ⓘ Cyan areas indicate GLVS and cyan nets indicate signals from/to GLVS.

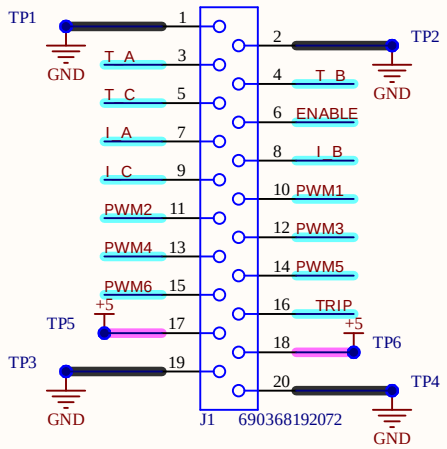
ⓘ Orange areas indicate TS and orange nets indicate high power TS.

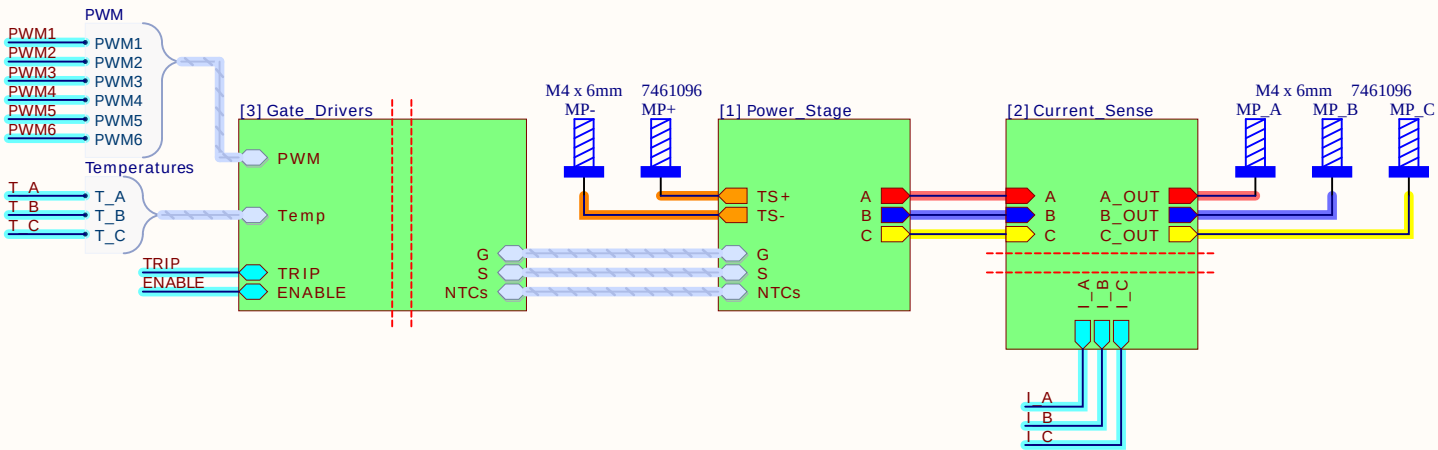
Specifications:

V_in, max = 600 VDC
V_out, max = 245 VRMS (SVPWM)
f_sw = 50 kHz
P_out_max = 40kW
I_out_max = 80 ARMS

Liquid cooled with water at 50ºC max

LV Connector





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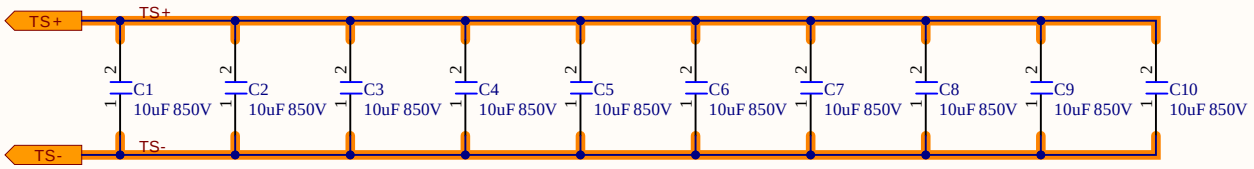
DC Bus capacitors, 100uF, Murata FHA85Y106KS



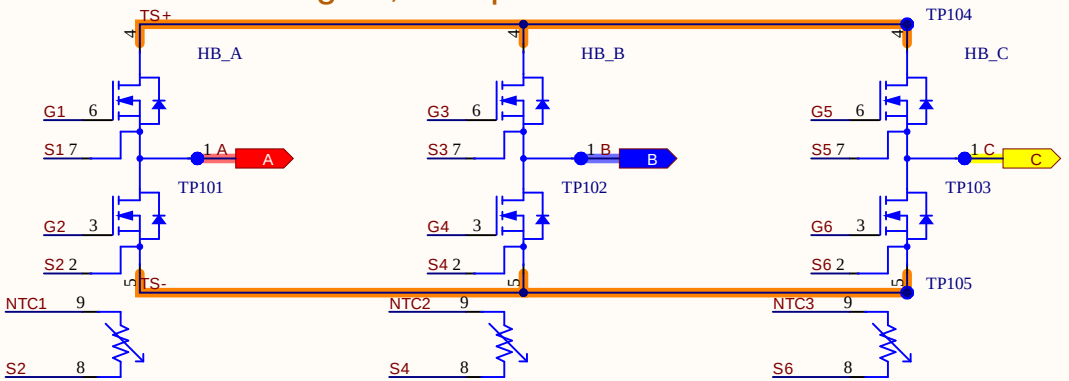
DC Link design considerations:

$V_C > 1.1 \cdot V_{max} = 1.1 \cdot 600\ V = 660\ V \rightarrow 850\ V$

$I_{C,RMS} \approx 0.65 \cdot I_{phase,RMS} = 0.65 \cdot 80\ A,RMS = 52\ A,RMS \rightarrow 10 \times 5\ A,RMS\ (\Delta T = 10\ ^oC)$
$C > I_{C,RMS} / (V_{ripple} \cdot f_{sw}) = 52\ A,RMS / (15V \cdot 50\ kHz) \approx 79\ \mu F \rightarrow 10 \times 10\ \mu F$

Lowering the switching frequency will proportionally lower the current rating for the same voltage ripple or proportionally increase the voltage ripple for the same output current. Check: https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter

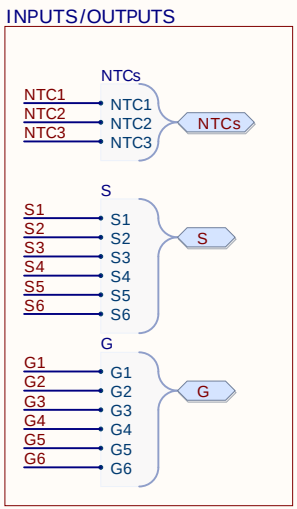
SiC Half-Bridges, Leapers DFS05HF12EYR1



Semiconductor details:

$V_{DSS(breakdown)} = 1200\ V$
$R_{on} = 5.5\ ..\ 13\ m\Omega$
$V_{f\_D} = 3.3\ ..\ 4\ V$
$T_{rr} = 41.5\ ..\ 45\ ns$
$Q_{rr} = 2.19\ ..\ 3.94\ \mu C$
$R_{th\_jc} = 0.12\ ..\ 0.15\ K/W$
$Q_G\ (600V, 150A, V_{GS} = +15/0V) = 520\ nC$
$C_{in} = 14.5\ nF$
$R_{G(int)} = 1.9\ \Omega$
$V_{GS(th)} = 2.8\ ..\ 4.8\ V$

INPUTS/OUTPUTS



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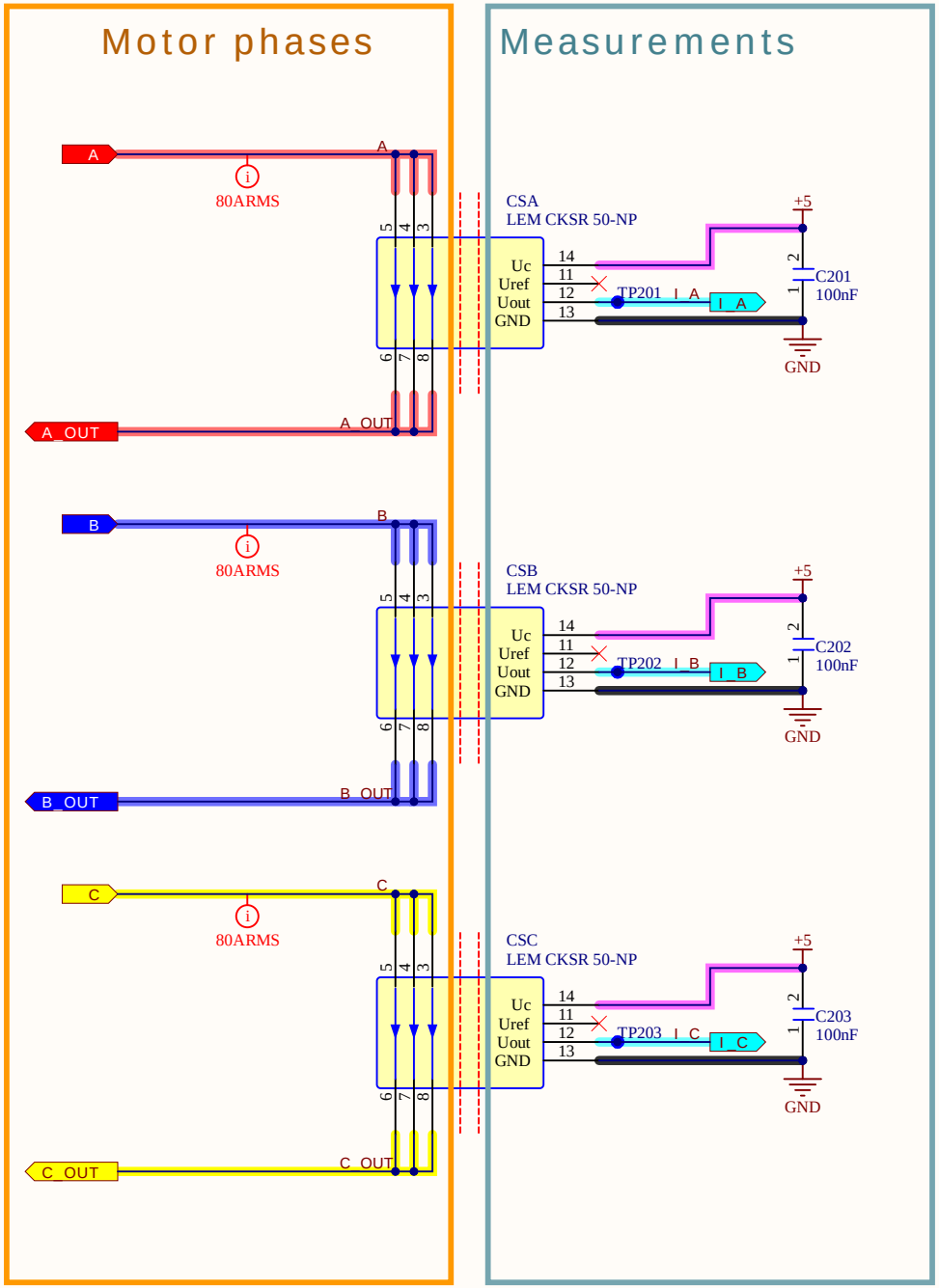
CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)



CSA , CSB , CSC

AC insulation test
RMS voltage, 50 Hz,
1 min:

Ud = 4.3 kV >
3*V_max = 1.8 kV

CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values

I_A, I_B, I_C

U_meas = (12.5mV/A · I_meas + 2.5V)

For ±150Apk:
V_meas_pk+ = 4.375V
V_meas_pk- = 0.625V

C201, C202, C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

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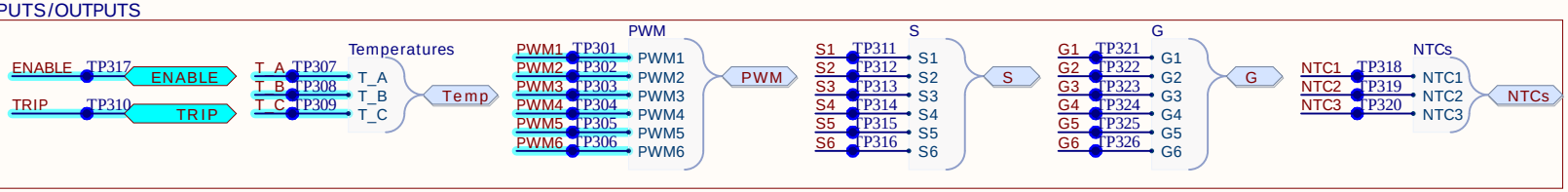
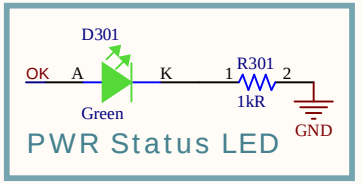
INPUTS/OUTPUTS

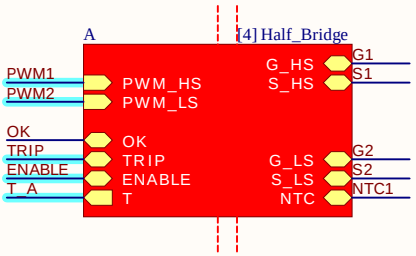


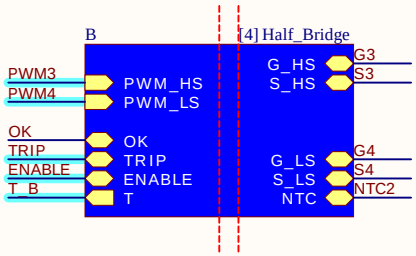


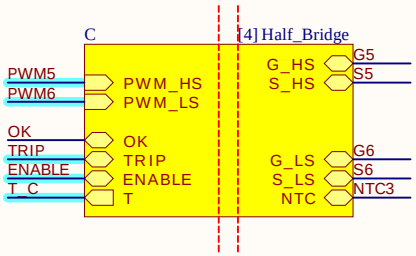
T_A, T_B, T_C

Look-up table obtained with MATLAB script.

For different temperatures:
V_meas(0ºC) = 0.246V
V_meas(25ºC) = 2V
V_meas(50ºC) = 2.578V
V_meas(90ºC) = 2.864V







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U_HS, U_LS

1. TRIP and OK signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to GND.
3. ENABLE to be given by MCU in active-high mode. When set to low for more than 1 µs, TRIP is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200 µA. PWM to analog using a RC filter, to be fed directly to MCU ADC. R405, R406 and C413 from SPICE simulation.
5. Miller clamp protection is used.
6. RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent/Shoot-through detection is not implemented.

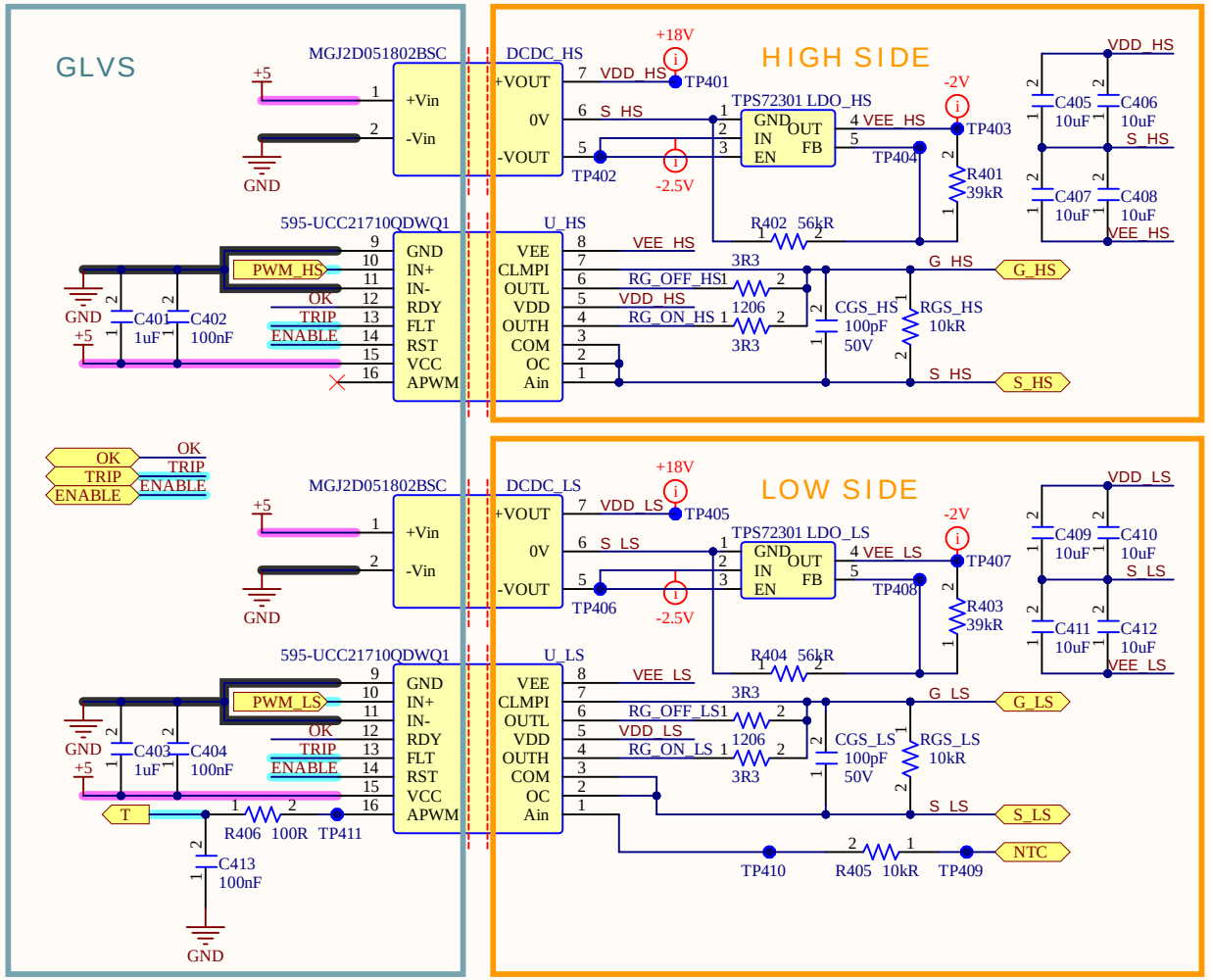
LDO_HS, LDO_LS

An LDO is implemented to trim VEE_LS_A and VEE_LS_A when testing the inverter. if a higher value is needed, DCDC_HS and DCDC_LS must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing
V_GS = +18 V / -2 V
VEE = - 1.186 · (1 + R1/R2)
R1 + R2 ≈ 100 kΩ

DCDC_HS, DCDC_LS
Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS
VIOTM (t = 60 s (qualification test)): 8000 VPK



V_GS values:

The values chosen for V_GS are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum V_GS(th). A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
I_GD(min) = f_sw · Q_G = 50 kHz · 520 nC = 26 mA
P_min = ΔV_GS · I_GD(min) = 20 V · 26 mA = 0.52 W → 2 W

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the manufacturer in the datasheet.

CGS_HS, CGS_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could result in further issues with the power limit for DCDC_HS and DCDC_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

CGS_max = 2 · P_DCDC / (ΔV_GS ^2 · f_sw) = 2 · 2 W / ((20 V)^2) · 50 kHz) = 200 nF

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