ⓘ Dashed red lines indicate isolation barriers between TS and LV.

ⓘ Cyan areas indicate GLVS and cyan nets indicate signals from/to GLVS.

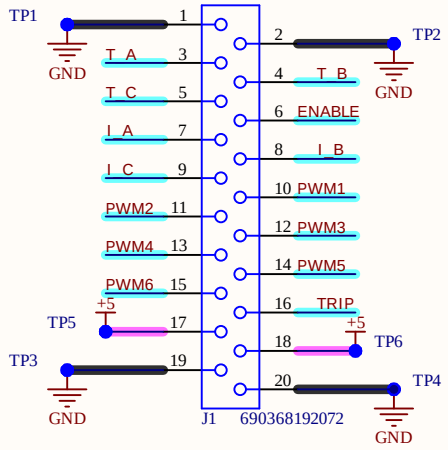
ⓘ Orange areas indicate TS and orange nets indicate high power TS.

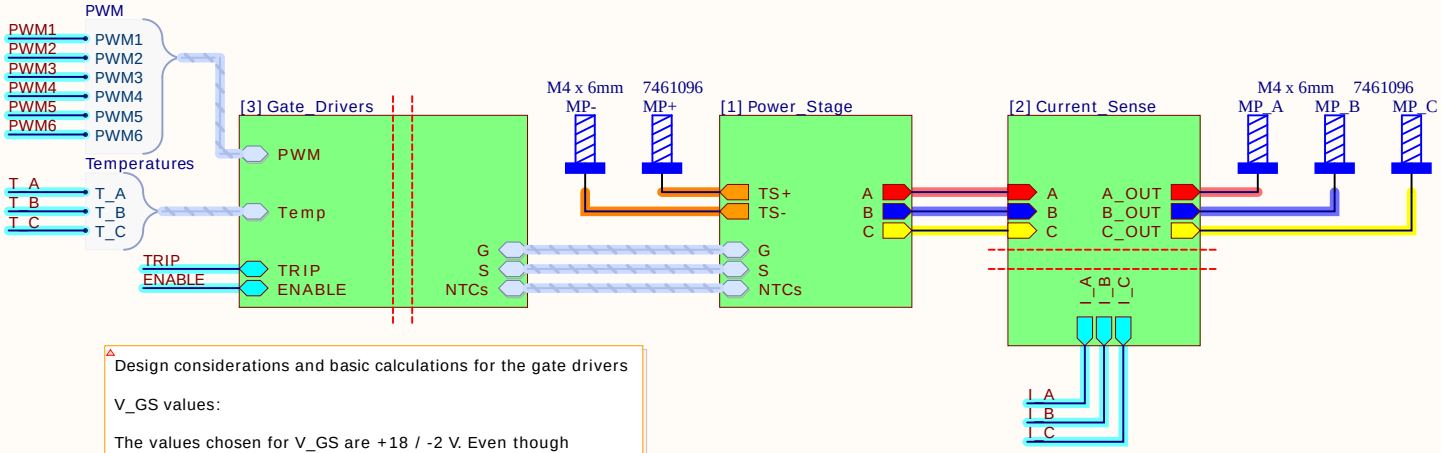
Specifications:

V_in, max = 600 VDC
V_out, max = 245 VRMS (SVPWM)
f_sw = 50 kHz
P_out_max = 40kW
I_out_max = 80 ARMS

Liquid cooled with water at 50ºC max

LV Connector





Design considerations and basic calculations for the gate drivers

V_GS values:

The values chosen for V_GS are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum V_GS(th). A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
$I_{GD(min)} = f_{sw} \cdot Q_G = 50\ kHz \cdot 520\ nC = 26\ mA$
$P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20\ V \cdot 26\ mA = 0.52\ W \rightarrow 1\ W$

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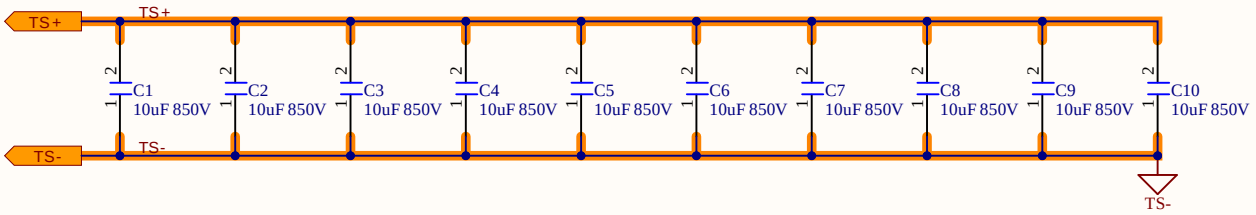
DC Bus capacitors, 100uF, Murata FHA85Y106KS



DC Link design considerations:

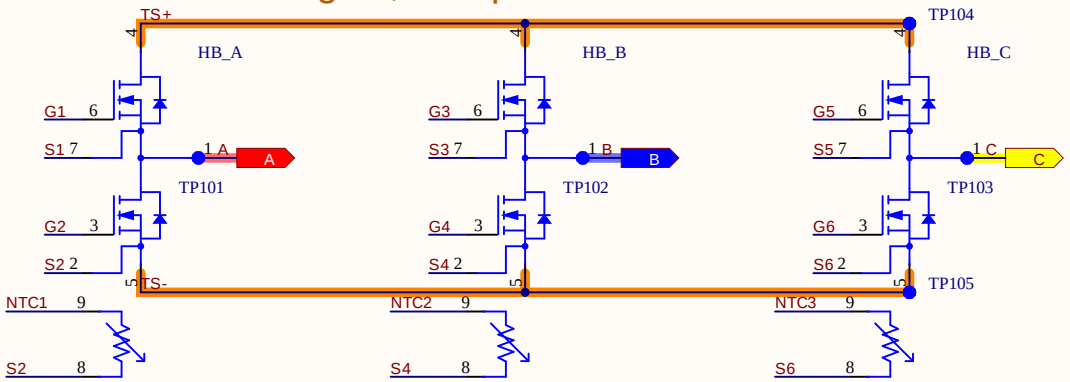
V_C > 1.1 · Vmax = 1.1 · 600 V = 660 V → 850 V

I_C,RMS ≈ 0.65 · I_phase,RMS = 0.65 · 80 A,RMS = 52 A,RMS → 10 x 5 A,RMS (ΔT = 10 ºC)

C > I_C,RMS / (V_ripple · f_sw) = 52 A,RMS / (15V · 50 kHz) ≈ 79 µF → 10 x 10 µF

Check:
https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter

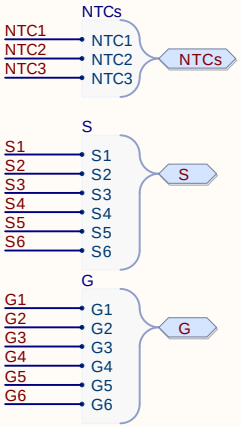
SiC Half-Bridges, Leapers DFS05HF12EYR1



Semiconductor details:

V_DSS(breakdown) = 1200 V
Ron = 5.5 .. 13 mΩ
Vf_D = 3.3 .. 4 V
T_rr = 41.5 .. 45 ns
Q_rr = 2.19 .. 3.94 µC
R_th_jc = 0.12 .. 0.15 K/W
Q_G (600V, 150A, V_GS = +15/0V) = 520 nC
C_in = 14.5 nF
R_G(int) = 1.9 Ω
V_GS(th) = 2.8 .. 4.8 V

INPUTS/OUTPUTS



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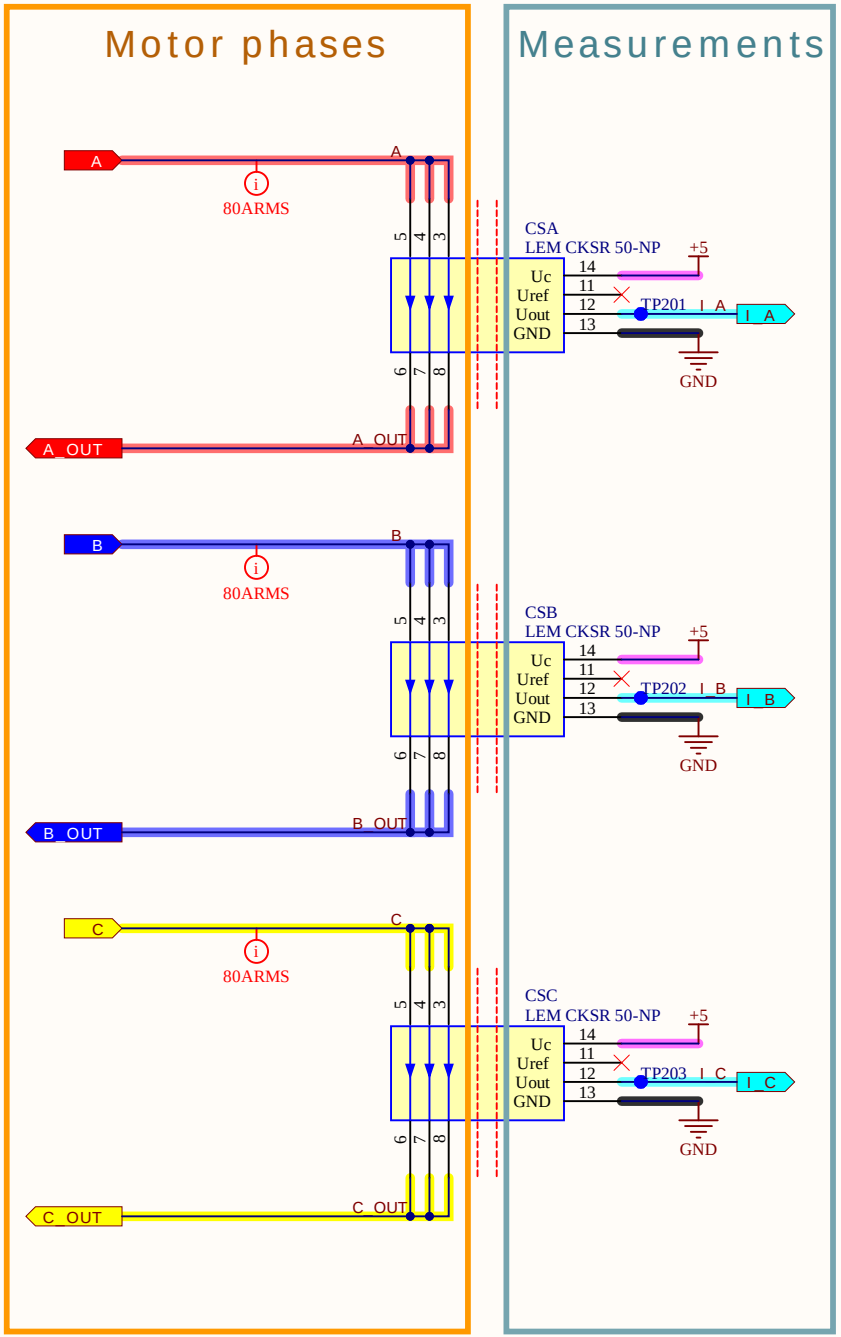
CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)

Motor phases

Measurements



CSA , CSB , CSC

AC insulation test RMS voltage, 50 Hz, 1 min:

Ud = 4.3 kV > 3*V_max = 1.8 kV

CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values

I_A , I_B , I_C

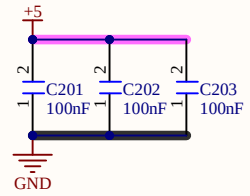
U_meas = (12.5mV/A · I_meas + 2.5V)

For ±150Apk:
U_meas_pk+ = 4.375V
U_meas_pk- = 0.625V

C201 , C202 , C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

Decoupling



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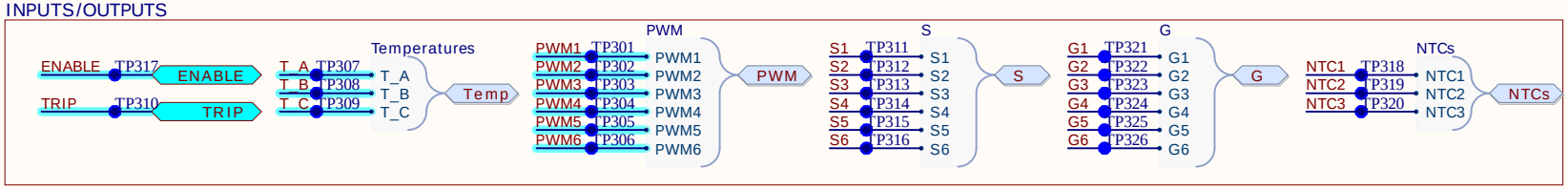
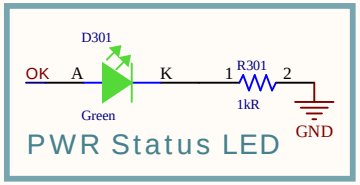
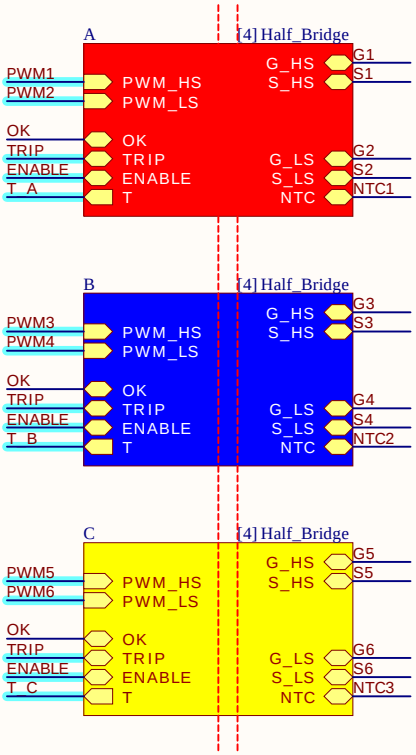
INPUTS/OUTPUTS







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U_HS, U_LS

1. TRIP and OK signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to GND.
3. ENABLE to be given by MCU in active-high mode. When set to low for more than 1us, TRIP is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200uA. An OrCAD SPICE simulation and a MATLAB file to compute LUT can be found in the parent directory. PWM to analog using a RC filter, to be fed directly to MCU ADC.
5. Miller clamp protection is used.
6. RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.

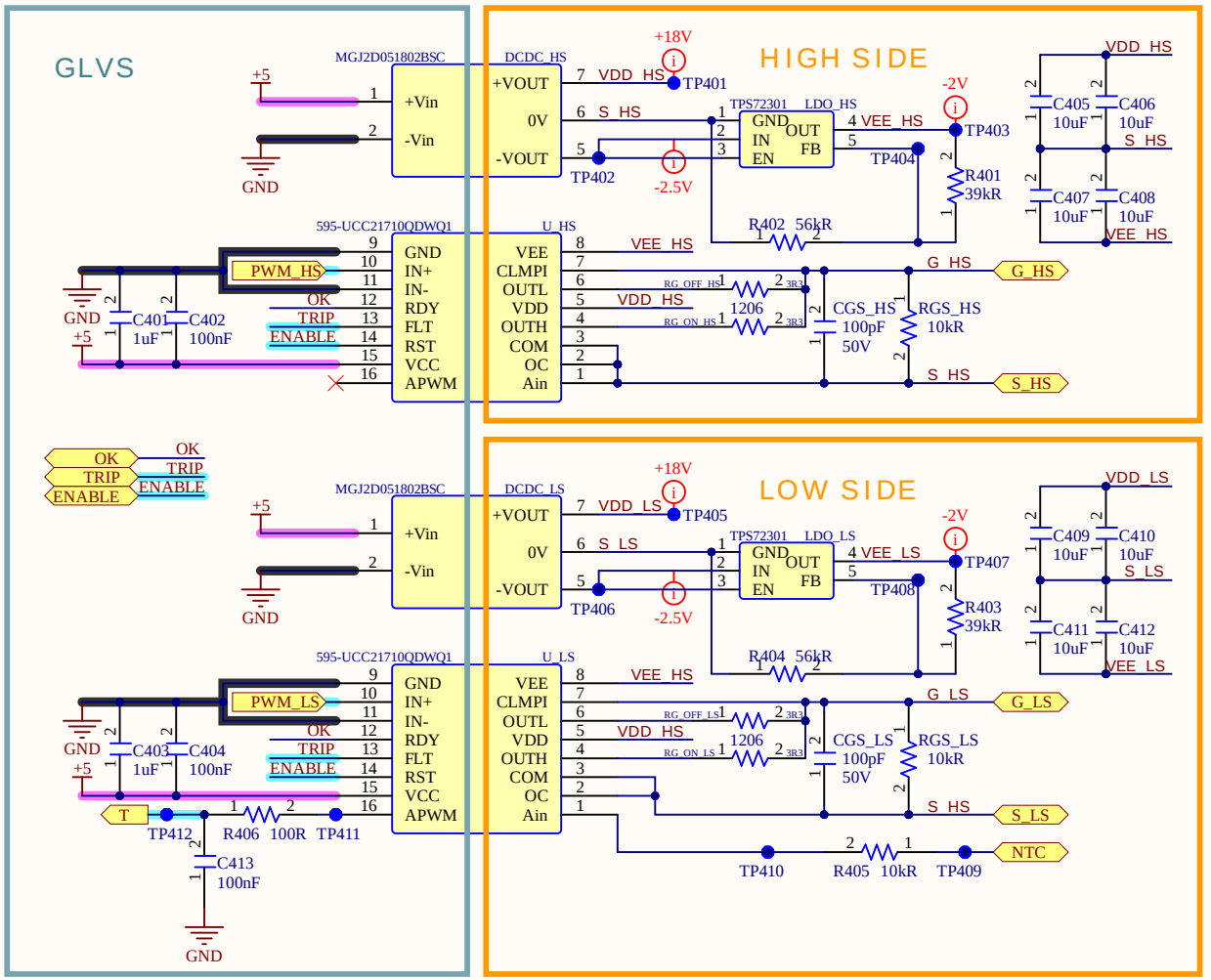
LDO_HS, LDO_LS

An LDO is implemented to trim VEE_HS_A and VEE_LS_A when testing the inverter. if a higher value is needed, DCDC_HS and DCDC_LS must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing
V_GS = +18 V / -2 V
V_out = - 1.186 * (1 + R1/R2), R1 + R2 ~= 100kOhm

DCDC_HS, DCDC_LS
Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS
VIOTM (t = 60 s (qualification test)): 8000 VPK



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