AB158x Series EVK Layout Guide

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Document revision history

Revision	Date	Description
1.0	15 Feb 2022	Initial Version. (C782/C804/C805)

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Lists of tables and figures

1. Introduction

The AB1585/8 is an advanced single-chip solution which integrates baseband and radio for intensive stereo/mono audio applications. Here is EVK daughterboard for layout guideline example, Figure 1, Figure 2, and the layout guide separated four function:

- PCB Specifications
- RF Layout Guidelines
- Power/GND Layout Guidelines
- Audio Layout Guidelines

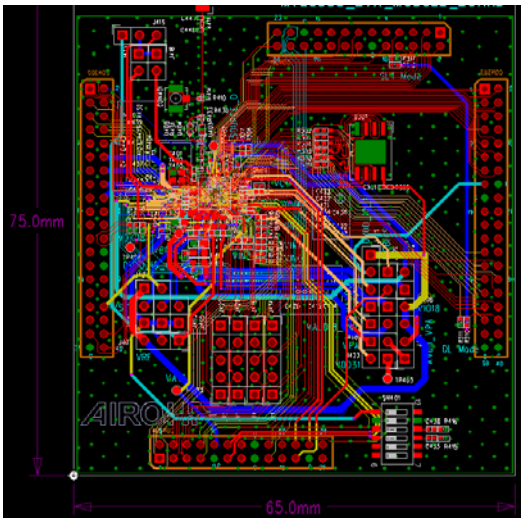

Figure 1. Top view of AB1588 EVK daughter board

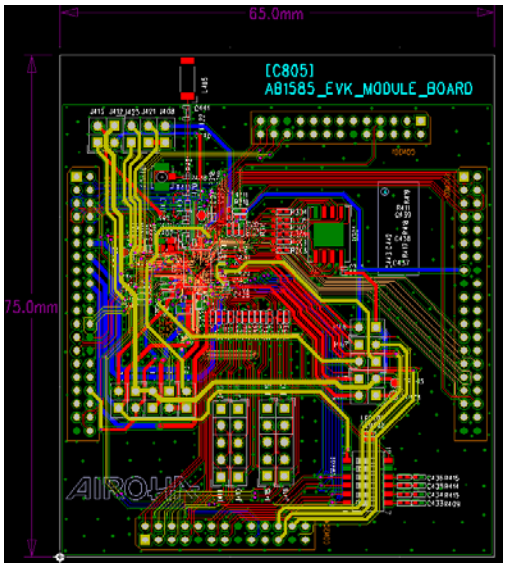

Figure 2. Top view of AB1585 EVK daughter board

2. PCB Specifications

The AB1588 EVK daughter board has six different layers, as shown in a stack-up layout in Table 1. and the AB1585 EVK daughter board has four different layers as shown in a stack-up layout in

Table **2**. Developers can make changes to the stack-up layers based on requirements and the impedance must be calculated wire-wide and with a separation. Please refer to

Table **3** and

Table **4** for more details.

Table 1. Stack-up table of the AB1588 EVK daughter board

Top side solder mask				0.7	mils
L1	**TOP**	**Differential and Signal**	**copper and plating**	1.2	mils
			prepreg	2.5	mils
L2			**copper**	0.8	mils
			prepreg	2.4	mils
L3			**copper**	1.1	mils
			core	46.0	mils
L4		**GND**	**copper**	1.1	mils
			prepreg	2.4	mils
L5			**copper**	0.8	mils
			prepreg	2.5	mils
L6	**Bottom**	**Differential and Signal**	**copper and plating**	1.2	mils
Bottom side solder mask				0.7	mils
TOTAL				63.2	mils
				1.606	mm

Total thickness: 1.6mm

Table 2. Stack-up table of the AB1585 EVK daughter board

Top side solder mask				0.80	mils
L1	**TOP**	**Differential and Signal**	**copper and plating**	1.40	mils
			prepreg	3.17	mils
L2		**GND**	**copper**	1.25	mils
			core	48.5	mils
L3			**copper**	1.25	mils
			prepreg	3.17	mils

Top side solder mask				0.80	mils
L4	**Bottom**	**Differential and Signal**	**copper and plating**	1.40	mils
Bottom side solder mask				0.80	mils
TOTAL				61.74	mils
				1.57	mm

Total thickness: 1.57mm

Table 3. PCB design rules of the AB1588 EVK daughter board

Parameter	Value	Comments
Number of layers	6	HDI 2+2+2
Thickness	1.6 mm	N/A
Dielectric	Er=4.4	Er@1 GHz
Minimum trace width	2.36 mils	Minimum track width can be reduced but the cost would be higher.
Minimum spacing	2.36 mils	Minimum spacing can be reduced but the cost would be higher.
Laser drill diameter	Top layer :3.54/8.27 mils Inner layer : 3.54/8.66 mils	N/A
Middle drill diameter	9.84/19.69 mils	N/A
Copper thickness	1 oz	N/A
RF Impedance	Trace wide: 3.8 mil Gnd gap: 6 mil	50 ohm impedance Gnd reference L2
USB Impedance	Trace wide: 3.9 mil Trace gap: 6 mil Gnd gap: 6 mil	90 ohm impedance Gnd reference L2

Table 4. PCB design rules of the AB1585 EVK daughter board

Parameter	Value	Comments
Number of layers	4	HDI 1+2+1
Thickness	1.6 mm	N/A
Dielectric	Er=4.4	Er@2.45GHz
Minimum trace width	2.36 mils	Minimum track width can be reduced but the cost would be higher.
Minimum spacing	2.36 mils	Minimum spacing can be reduced but the cost would be higher.
Laser drill diameter	3.94/8.66 mils	N/A
Middle drill diameter	9.84/17.72 mils	N/A

Parameter	Value	Comments
Copper thickness	1 oz	N/A
RF Impedance	Trace wide:5 mil Gnd gap: 8 mil	50 ohm impedance Gnd reference L2
USB Impedance	Trace wide:5 mil Trace gap:6 mil Gnd gap: 8 mil	90 ohm impedance Gnd reference L2

3. RF Layout Guidelines

3.1. RF trace

It is essential to provide a correct layout for the RF section (as shown in Figure 3) for the wireless device in order to achieve optimum device performance. A poor layout can cause performance degradation for the output power, the DEVM, the harmonic emission, the sensitivity, and the spectral mask. There is need to add BPF/LPF to BT_TRX for Tx harmonic rejection, and other PI network for Antenna matching should be put close to the antenna.

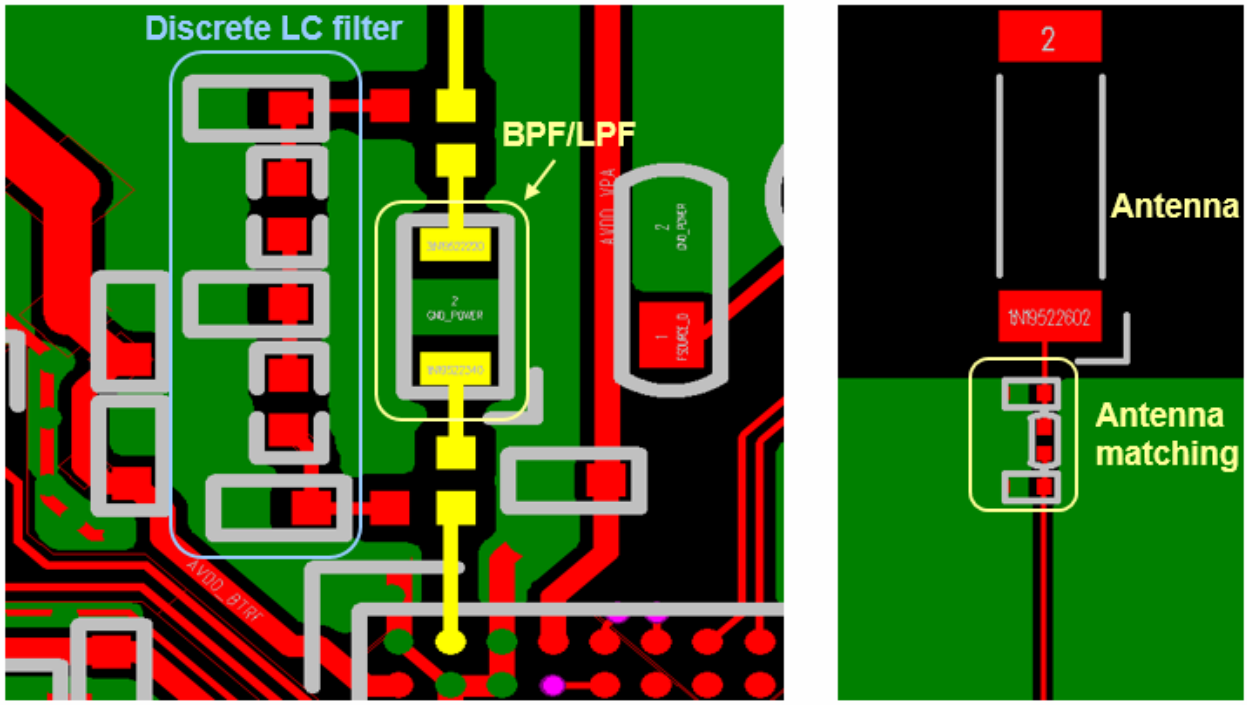

Figure 3. RF trace of the AB1585/AB1588 EVK daughter board

- Make sure RF path impedance is 50 ohm
- RF trace to antenna should be the top layer and do not let it go through by vias.
- Make sure that the ground plane under the RF trace is solid and increase the vias around the RF trace.
- BPF/LPF/discrete LC filter should be placed as close as possible to IC BT_TRX.
- Make sure the return path is solid and good, and the reference layer should be checked also. Refer Figure 4 for more information.

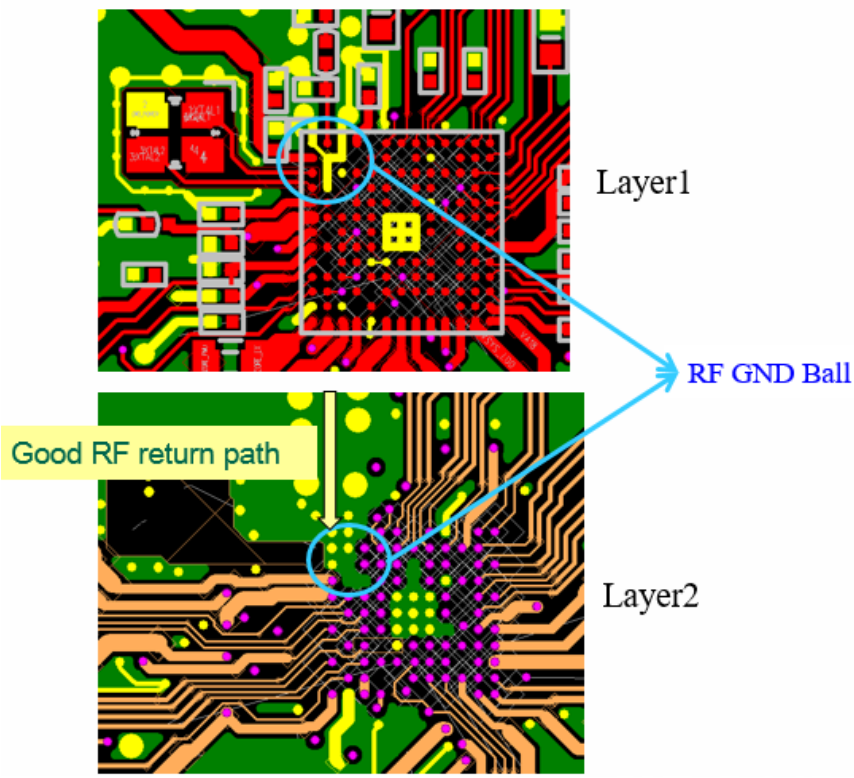

Figure 4. Gnd Via around RF trace and return RF trace of the AB1585/AB1588 EVK daughter board

3.2. RF circuit decupling Cap

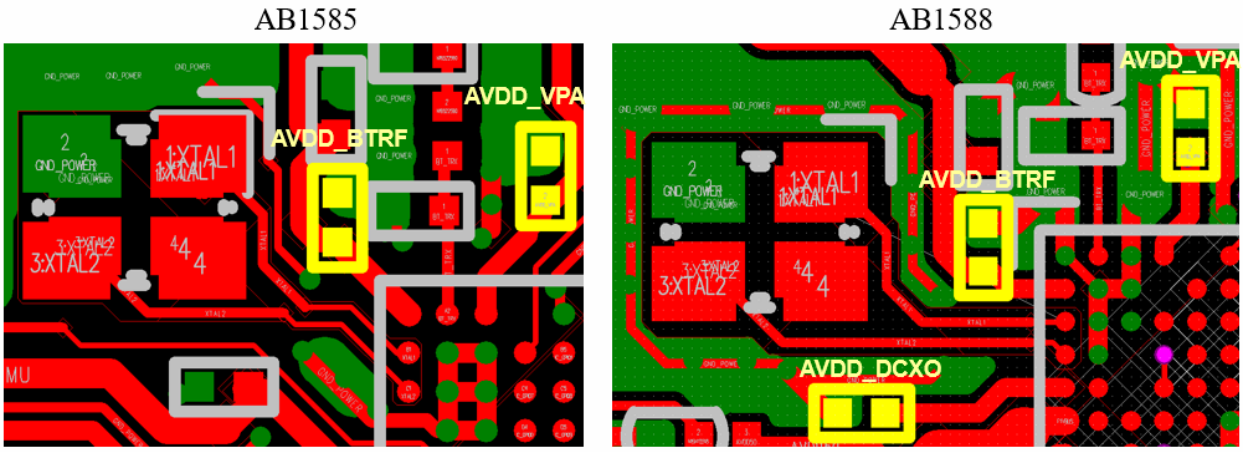

Figure 5. RF circuit decupling Cap of the AB1585/AB1588 EVK daughter board

All decoupling caps for AVDD_VBT (0.1uF), AVDD_BTRF (1uF), and AVDD_DCXO (1uF) should be placed as close as possible to the pins and with enough GND via for better return path.

3.3. Crystal 26M

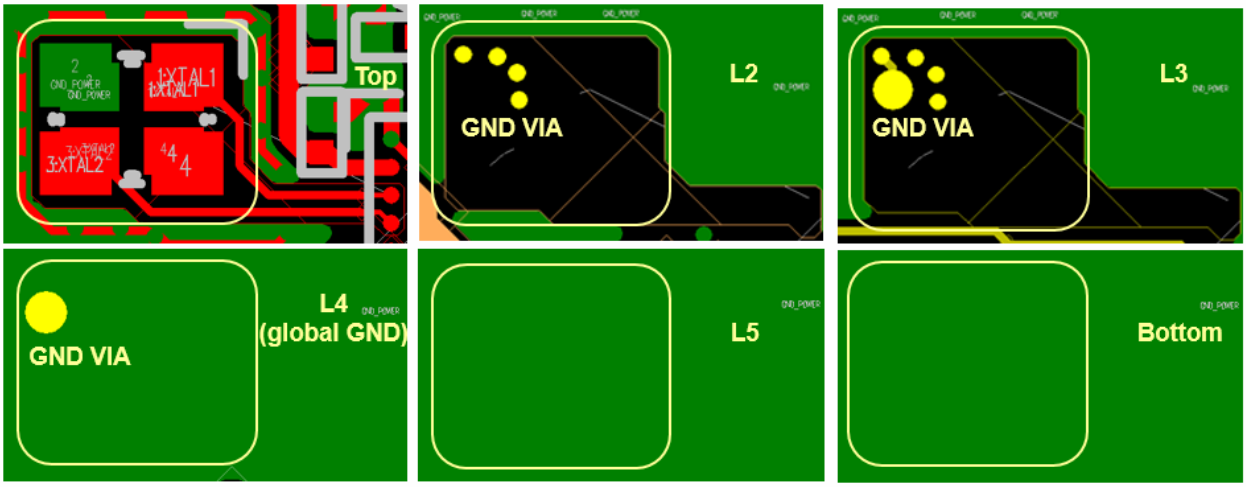

Figure 6. Crystal 26M of the AB1585/AB1588 EVK daughter board

- The crystal and its trace directly refer to the global ground, please refer to Figure 6 (Keep out L1&L2&L3 ground).
- XTAL pins must be put at the top layer if possible. If it is not possible, put them at the bottom layer with the shortest trace to crystal.
- XTAL ground pad directly connects to the global ground. Do not connect to GND on a different layer.
- Add more GND vias around crystal for good isolation, please refer to Figure 7.

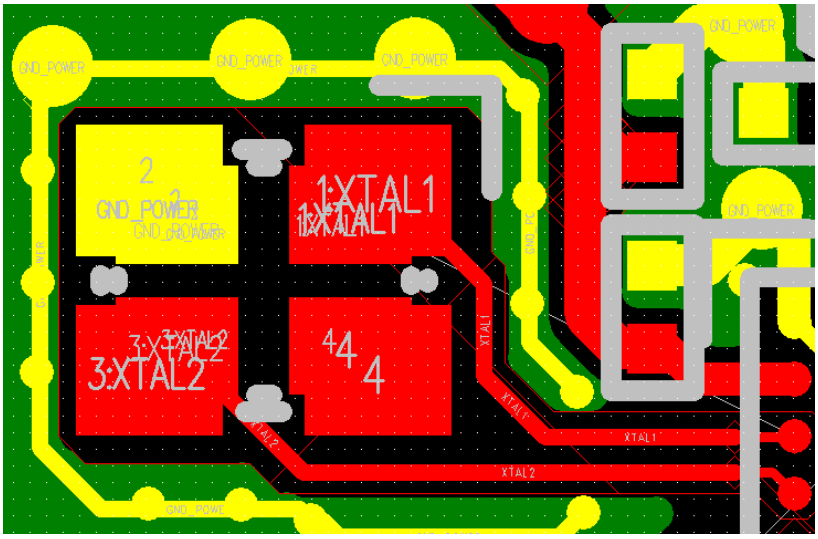

Figure 7. Crystal 26M ground vias of the AB1585/AB1588 EVK daughter board

4. Power Layout Guidelines

4.1. Power Trace

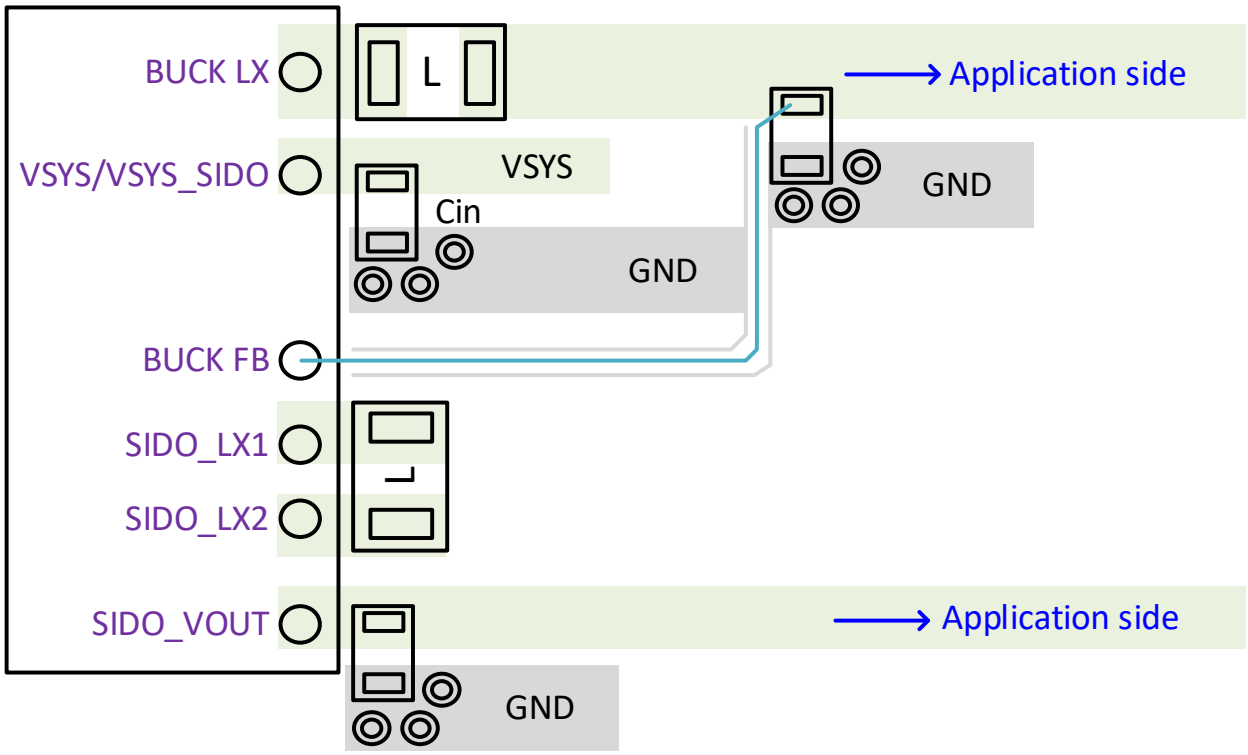

Figure 8. Buck and SIDO layout guide

- The BUCK/SIDO input cap must as close to VSYS, VSYS_BUCK and VSYS_SIDO pins as possible.
- The BUCK/SIDO inductor must as close to BUCK_LX, SIDO_LX1, SIDO_LX2 pins as possible.
- The BUCK/SIDO input cap GND connects directly to the main ground as shown in the figure below.
- The BUCK/SIDO input cap must be the closest, then the BUCK/SIDO inductor.
- The sensing point of the BUCK_FB path must be located at the maximum output capacitor.
- BUCK_FB must be shielded with GND and no noise above or below.
- The SIDO output cap must very close to SIDO_VOUT.
- SIDO cap GND connect with main ground directly and separated with another SIDO GND.
- Avoid putting the inductor close to the antenna, microphone or speaker.

4.2. Buck Trace

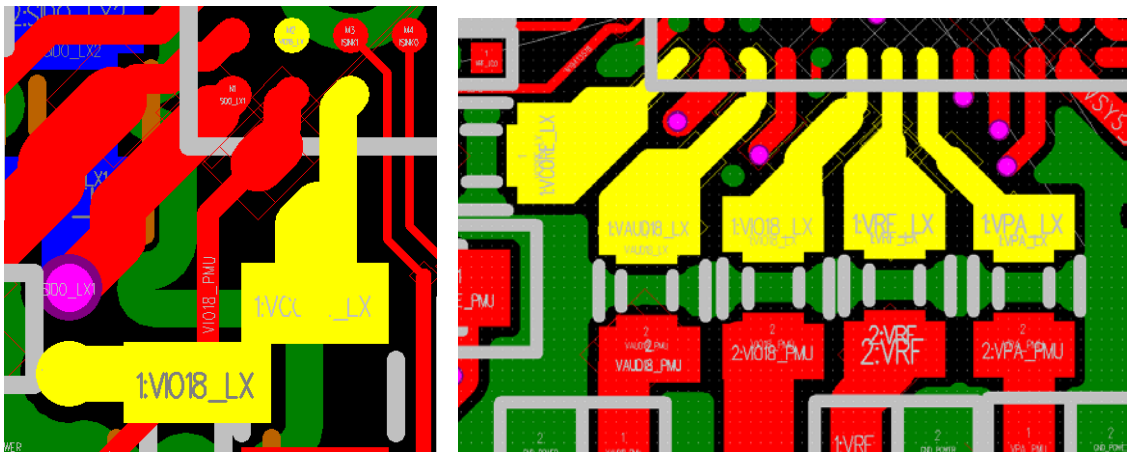

Figure 9. LX Trace of theAB1585 and AB1588 EVK daughter board

The VIO18, VCORE, VAUD18, VPA must be kept as wide as possible. Please refer to Table 5.

Table 5. BUCK/SIDO trace wide of the AB1585 and AB1588 EVK daughter board

Parameter	Trace Width (mil)	GND shielding
VCORE_LX	12	
VCORE_FB	6	Yes
VIO18_LX	12	
VIO18_FB, AVDD18_AUD	6	Yes
VAUD18_LX, SIDO_VAUD18	10	
VAUD18_FB	min width	Yes
VRF_LX, SIDO_VRF	6	
VRF_FB	min width	Yes
VPA_LX	10	
VPA_FB	min width	Yes
SIDO_LX1, SIDO_LX2	10	

4.3. LDO Trace

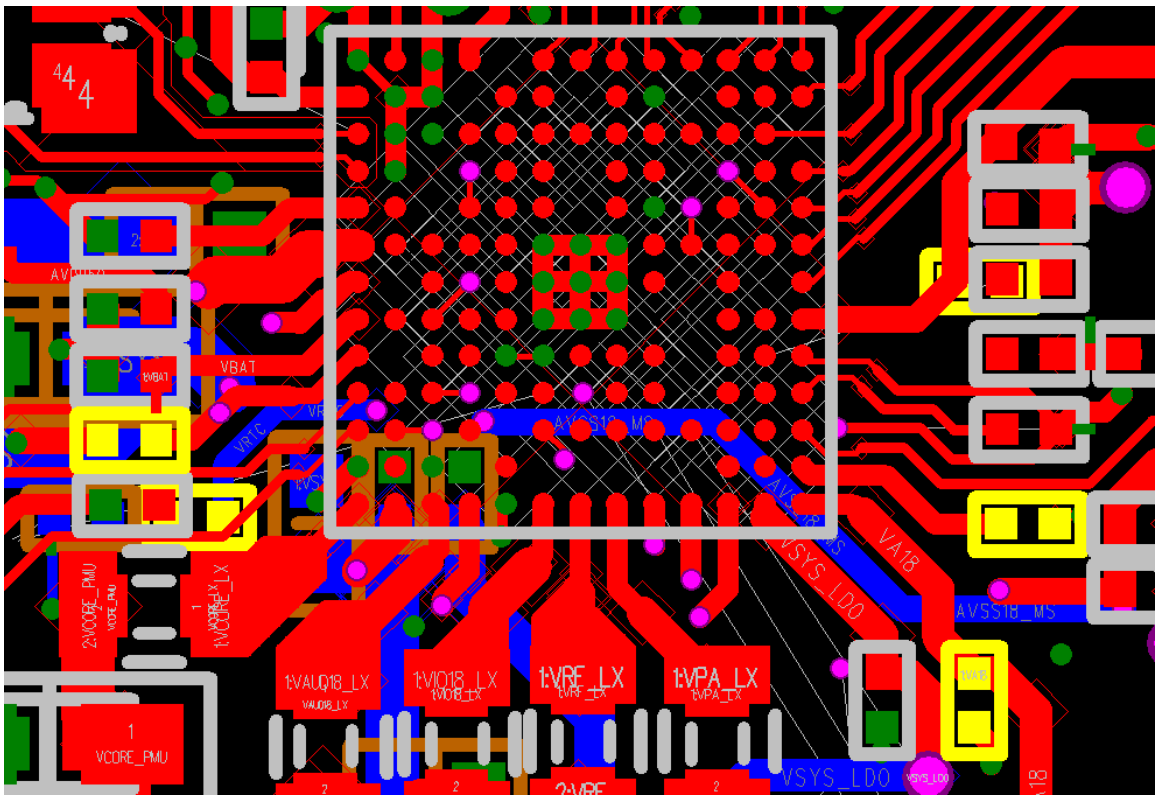

Figure 10. LDO decoupling capacitor of the AB1588 EVK daughter board

- The distance between the decoupling capacitor and IC pin must be as short as possible.
- Traces must be routed through the decoupling capacitor pin before the IC pin.
- The LDO trace must be kept as wide as possible. Please refer Table 6.
- The LDO output pin and the farthest cap must less than 200mΩ.

Table 6.BUCK trace wide of theAB1585 and AB1588 EVK daughter board

Parameter	Trace Width (mil)	GND shielding
VDIG18	4	
VDD31	6	
VRF	6	
VSRAM	6	
VA18	4	Nice to have
VRTC	4	
ISINK0	6	
ISINK1	6	

4.4. Charger trace

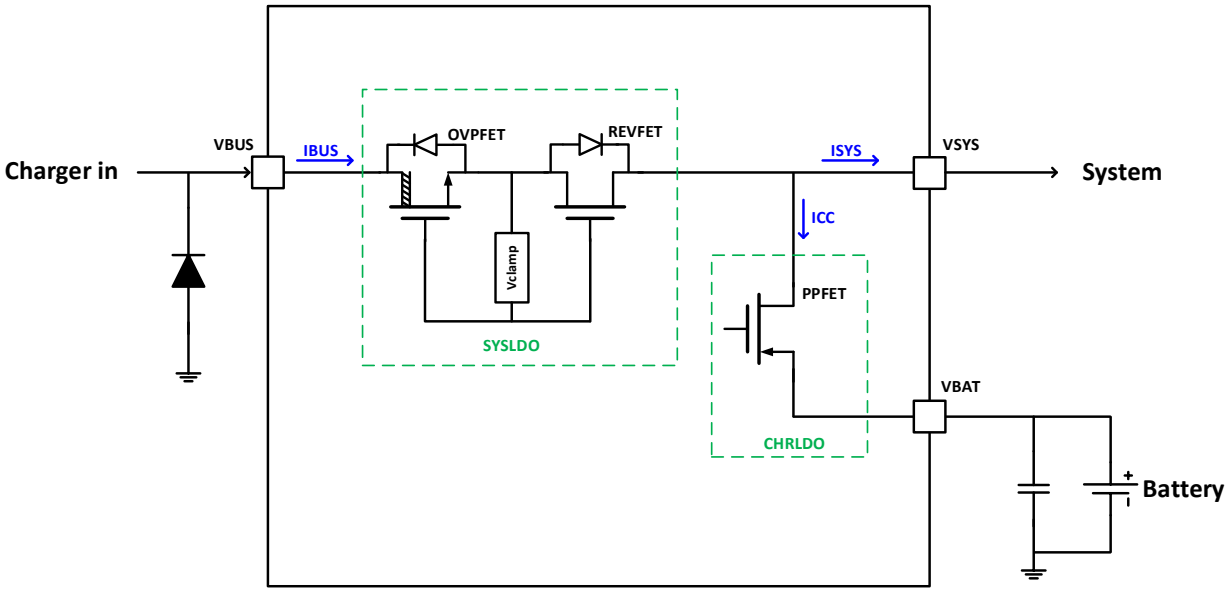

Figure 11. Charger path

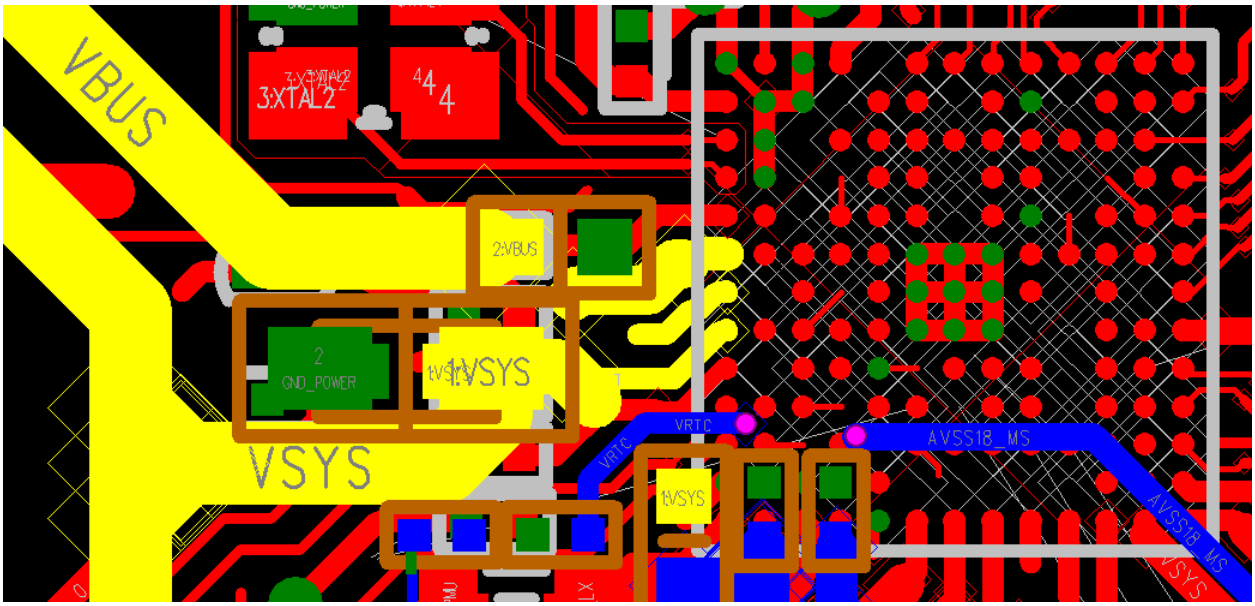

Figure 12. Charger path of the AB1588 EVK daughter board

- The charger trace must be kept as wide as possible.
- VBUS, VBAT and VSYS decoupling capacitor and IC pin must be as short as possible.
- The LDO trace must be kept as wide as possible. Please refer Table 7.

Table 7.Charger trace wide of the AB1588 EVK daughter board

Parameter	Trace Width (mil)	GND shielding
VSYS	20	
VBAT	20	
VBUS	20	ESD and schottky protection is recommended
VBUS_UART	12	ESD and schottky protection is recommended

5. Audio Layout Guidelines

For better audio performance and to avoid interference or path loss, you must obey the following rules:

1) The length of microphone path (AU_VIN0_P, AU_VIN0_N, AU_VIN1_P and AU_VIN1_N, AU_VIN2_P and AU_VIN2_N, AU_VIN3_P and AU_VIN3_N) and speaker path (AU_HPRP, AU_HPRN, AU_HPLP and AU_HPLN) must be as short as possible.
2) Increase the width of the speaker trace to reduce the parasitic resistance that occurs when the speaker trace is too long.
3) The microphone path and speaker path are routed with a solid ground on both sides and the shield is formed by having the ground on the PCB layers above and below the signals. The surrounding ground planes must be firmly connected with vias to make sure there is a good connection between the ground layers and to the main ground in the PCB.
4) For Class D amp applications, the SPK traces must be isolated to all MIC traces to avoid interference by the PWM wave.

5.1. SPK out trace

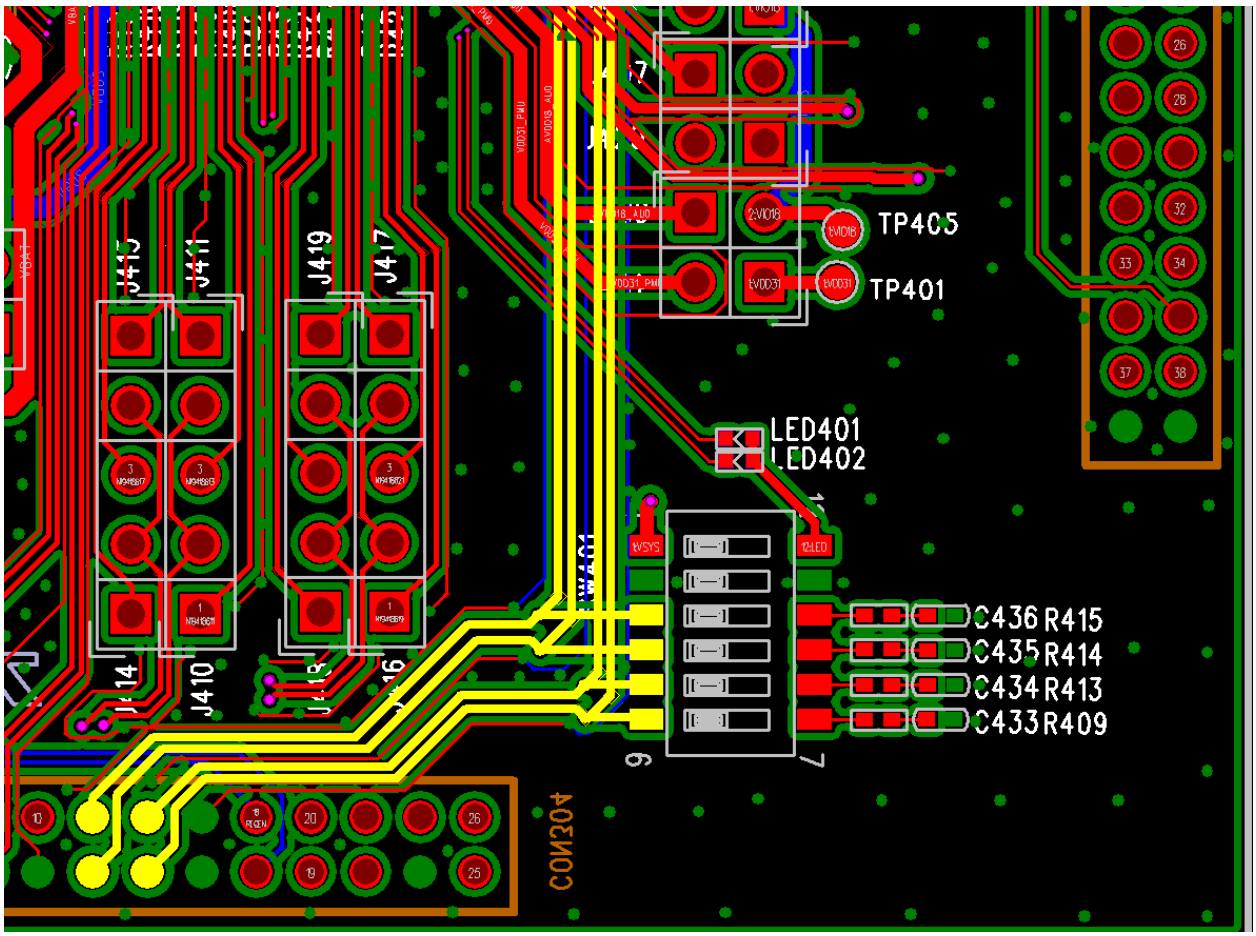

Figure 13. SPK out trace of the AB1585/1588 EVK daughter board

- The SPK trace should be well shielded by the ground traces and not overlap other traces in the layers in the middle.
- The trace width must be at least 12 mil wide.

5.2. Mic out trace

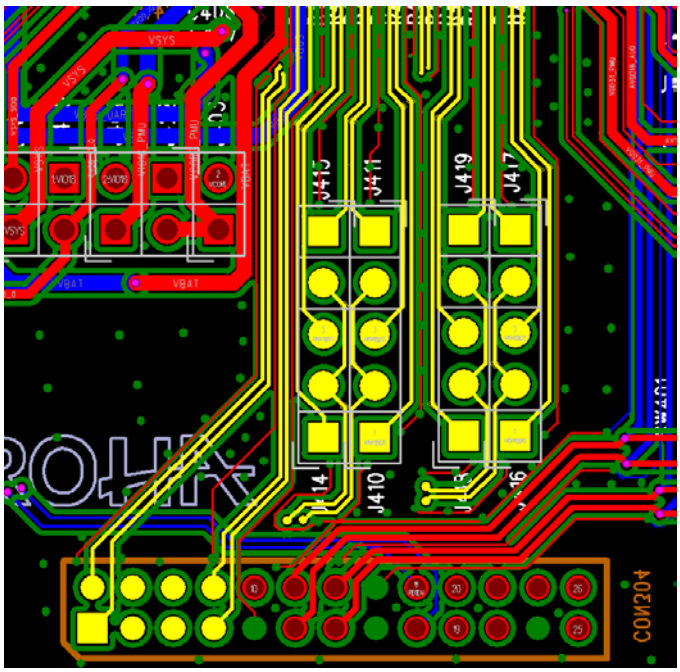

Figure 14. Mic out trace of the AB1585/1588 EVK daughter board

- The width of MIC traces should be at least 6 mil wide and the length of MIC pairs should be as similar as possible and shielded by a ground trace.

5.3. Mic_bias trace

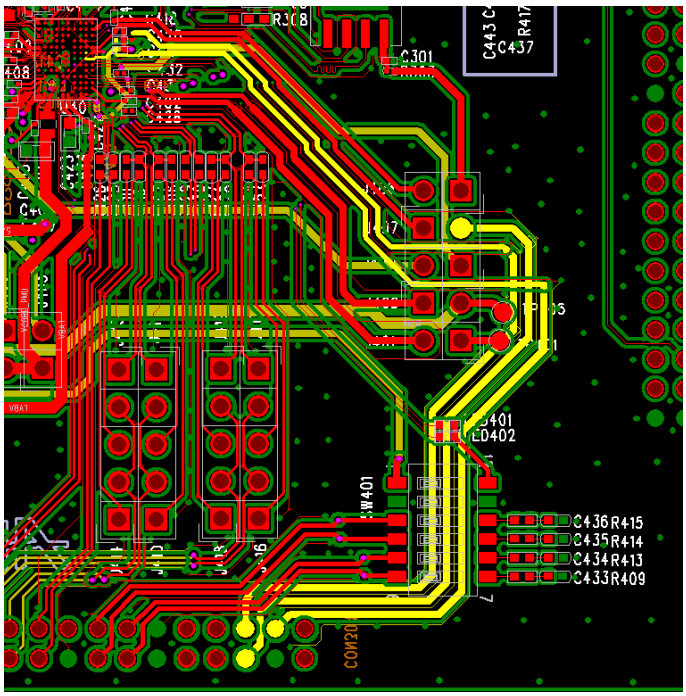

Figure 15. Mic_bias trace of the AB1585/1588 EVK daughter board

- The width of Mic_bias traces should be at least 6 mil and shielded well by the ground trace.

5.4. Touch Pad

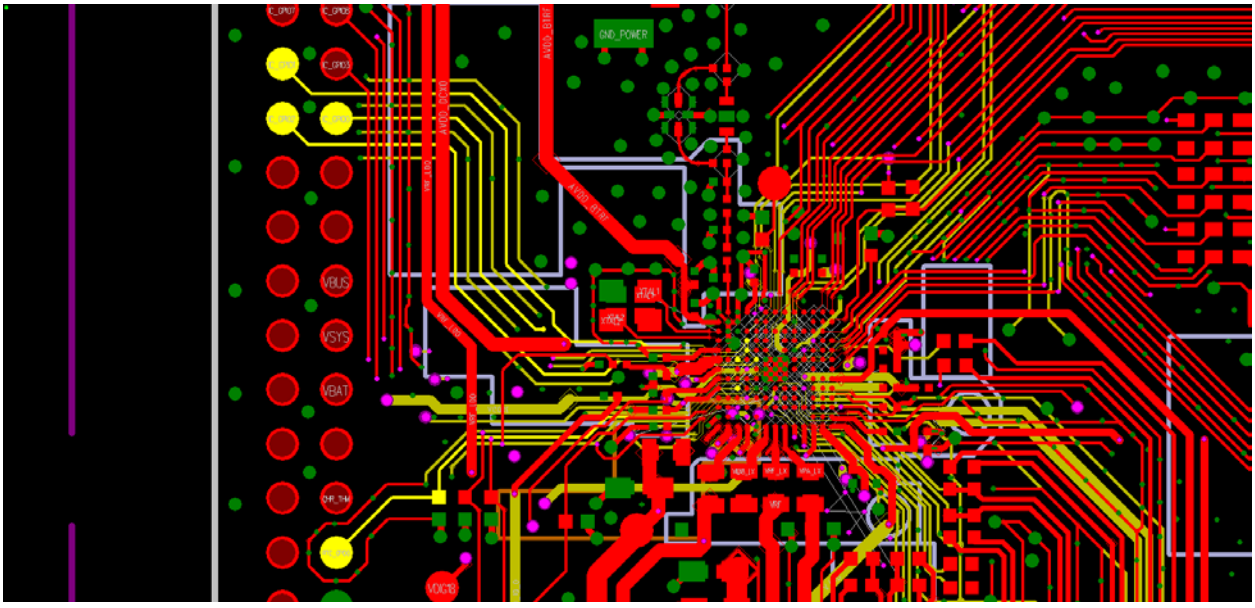

Figure 16. Touch Pad of the AB1588 EVK daughter board

- Trace/pad of the touch should be shielded by ground as much as possible. We suggest adding a GND area for the shielding to surround the touch trace. We also suggest putting the trace layout on bottom layer and the touch sensor on the top layer. It is better if the middle layer empty, with no signal, and no GND

layer. If there is high speed signal cross touch trace, it is better to add a GND layer (Grip GND is best) between the touch trace and signals. Avoid using the via. If a via is necessary, do not add the via over the touch trace and signals.

- We strongly suggest that the width between the touch trace is at least 5 times the width of the trace; a larger gap is always better. The distance from the trace to the other signals (ex: I²C, SPI, Clock, Power, GND) should be three times the trace width; it is always better to put them further apart. If the touch trace cannot be away from the signal line, put them in a vertical layout, not parallel. Otherwise, add a GND line between them.
- We strongly suggest that the distance from the touch trace to other signals (ex: I²C, SPI, Clock, Power, GND) be three times the width of the trace; It is always better to put them further apart.
- Bigger sensors are more sensitive but do not let the capacitance value of the sensor with trace be more than 40pF. We suggest adding a GND grid for shielding to surround the touch sensor and to cover components on the top & bottom and over the touch area. The material overlay on the touch sensor should not be conductive or contain any metal.
- The trace from the sensor pad to IC pin should be short and thin (i.e. between 3mil and 6mil).
- When the touch function are enabled, let the touch channels (GPIO0 / 1 / 2, RTC_GPIO0) be a critical line.
- If there are the branches on GPIO0 / 1 / 2, RTC_GPIO0, keep the branches short to avoid increasing the parasitic cap. value.
- The total cap value on every channel should be less than 40pF (Sensors + Traces)
- If more than two shared pin function on the GPIO0/1/2 and RTC_GPIO0, reserve a 0ohm as close as possible to the touch trace to avoid increasing the parasitic cap. value. The total cap value should be less than 40pF (Sensors + Traces).